Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1154agc-gad-ax

(2) Non-port functions (1/3)

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Digital input port	P20 to P27
ANO0	Output	D/A converter analog output	Input port	P110
ANO1	Output	D/A converter analog output	Input port	P111
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P50
INTP2				P51
INTP3				P30/RTC1HZ
INTP4				P31/TI03/TO03
INTP5				P16/TI01/TO01
INTP6				P140/PCLBUZ0
INTP7				P141/PCLBUZ1
INTP8				P74/KR4 to P77/KR7
INTP9				
INTP10				
INTP11				
KR0 to KR3	Input	Key interrupt input	Input port	P70 to P73
KR4 to KR7				P74/INTP8 to P77/INTP11
PCLBUZ0	Output	Clock output/buzzer output	Input port	P140/INTP6
PCLBUZ1				P141/INTP7
REGC	–	Connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF).	–	–
RTCDIV	Output	Real-time counter clock (32 kHz divided frequency) output	Input port	P15/RTCCL
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P15/RTCDIV
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Input port	P30/INTP3
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD0	Input	Serial data input to UART0	Input port	P11/SI00
RxD1	Input	Serial data input to UART1	Input port	P03/SI10/SDA10
RxD2	Input	Serial data input to UART2	Input port	P143/SI20/SDA20
RxD3	Input	Serial data input to UART3	Input port	P14
$\overline{\text{SCK00}}$	I/O	Clock input/output for CSI00, CSI01, CSI10, and CSI20	Input port	P10
$\overline{\text{SCK01}}$				P43
$\overline{\text{SCK10}}$				P04/SCL10
$\overline{\text{SCK20}}$				P142/SCL20

(2) Non-port functions (3/3)

Function Name	I/O	Function	After Reset	Alternate Function
V_{DD}	–	Positive power supply (P121 to P124 and other than ports (excluding $\overline{RESET}$ and FLMD0 pins))	–	–
EV_{DD}	–	Positive power supply for ports (other than P20 to P27, P110, P111 and P121 to P124) and $\overline{RESET}$ and FLMD0 pins	–	–
AV_{REF0}	–	• A/D converter reference voltage input • Positive power supply for P20 to P27 and A/D converter	–	–
AV_{REF1}	–	• D/A converter reference voltage input • Positive power supply for P110, P111, and D/A converter	–	–
V_{SS}	–	Ground potential (P121 to P124 and other than ports (excluding $\overline{RESET}$ and FLMD0 pins))	–	–
EV_{SS}	–	Ground potential for ports (other than P20 to P27, P110, P111 and P121 to P124) and $\overline{RESET}$ and FLMD0 pins	–	–
AV_{SS}	–	Ground potential for A/D converter, D/A converter, P20 to P27, P110, and P111	–	–
FLMD0	–	Flash memory programming mode setting	–	–
TOOL0	I/O	Data I/O for flash memory programmer/debugger	Input port	P40
TOOL1	Output	Clock output for debugger	Input port	P41

3.4.9 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents. This addressing is automatically employed when the PUSH, POP, subroutine call, and return instructions are executed or the register is saved/restored upon generation of an interrupt request.

Stack addressing is applied only to the internal RAM area.

[Operand format]

Identifier	Description
–	PUSH AX/BC/DE/HL POP AX/BC/DE/HL CALL/CALLT RET BRK RETB (Interrupt request generated) RETI

Table 5-5. Changing CPU Clock (2/2)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
Subsystem clock[Note]	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator and selection of internal high-speed oscillation clock as main system clock • HIOSTOP = 0, MCS = 0	XT1 oscillation can be stopped (XTSTOP = 1)
	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	Enabling input of external clock from EXCLK pin and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 1, MSTOP = 0 • MCS = 1	

Note When changing the subsystem clock to another clock, the clock must be set back to the clock before setting the subsystem clock. For example, when changing the clock to the X1 clock after having changed the internal high-speed oscillation clock to the subsystem clock, the clock is changed in the order of the subsystem clock, the internal high-speed oscillation clock, and the X1 clock.

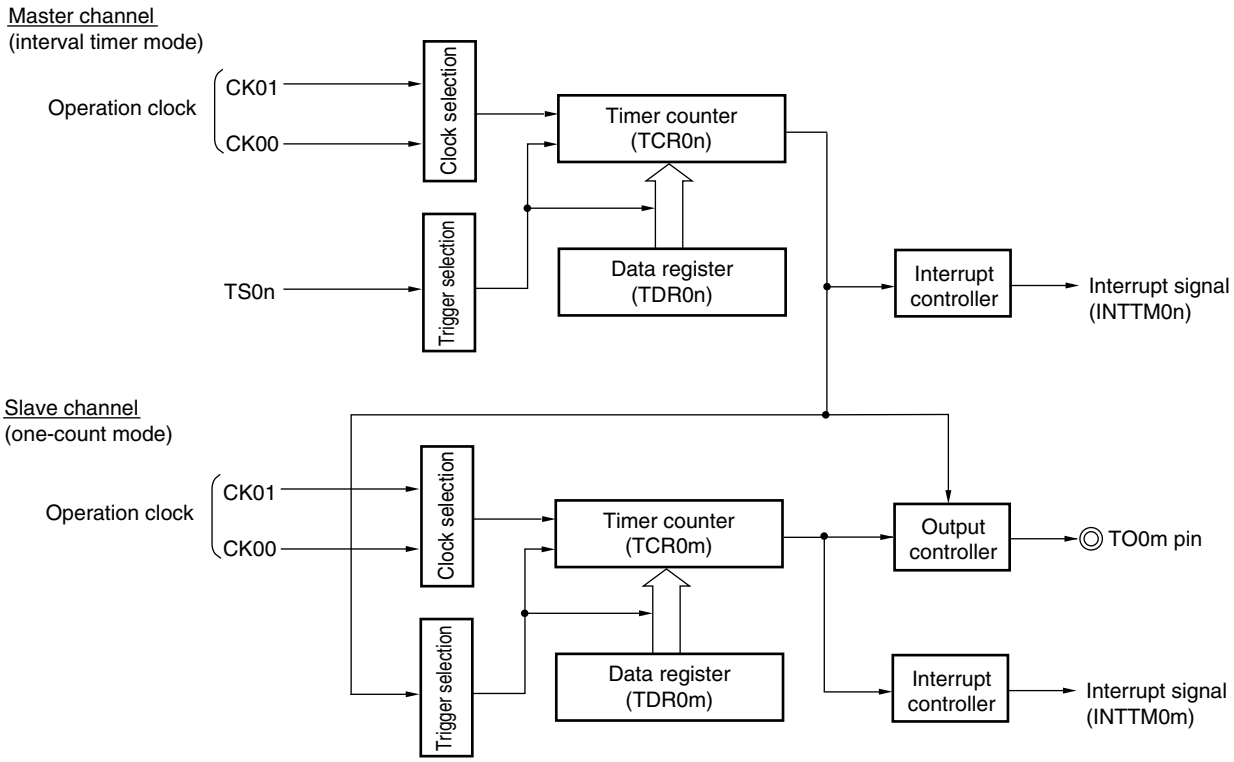
Figure 6-50. Operation Procedure When Input Pulse Interval Measurement Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN bit of the PER0 register to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets the TPS0 register. Determines clock frequencies of CK00 and CK01.	
Channel default setting	Sets the TMR0n register (determines operation mode of channel).	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets TS0n bit to 1. → The TS0n bit automatically returns to 0 because it is a trigger bit.	TE0n = 1, and count operation starts. TCR0n is cleared to 0000H at the count clock input. When the MD0n0 bit of the TMR0n register is 1, INTTM0n is generated.
During operation	Set values of only the CIS0n1 and CIS0n0 bits of the TMR0n register can be changed. The TDR0n register can always be read. The TCR0n register can always be read. The TSR0n register can always be read. Set values of TOM0n, TOL0n, TO0n, and TOE0n bits cannot be changed.	Counter (TCRn) counts up from 0000H. When the TI0n pin input valid edge is detected, the count value is transferred (captured) to TDR0n. At the same time, TCR0n is cleared to 0000H, and the INTTM0n signal is generated. If an overflow occurs at this time, the OVF bit of the TSR0n register is set; if an overflow does not occur, the OVF bit is cleared. After that, the above operation is repeated.
Operation stop	The TT0n bit is set to 1. → The TT0n bit automatically returns to 0 because it is a trigger bit.	TE0n = 0, and count operation stops. TCR0n holds count value and stops. The OVF bit of the TSR0n register is also held.
TAU stop	The TAU0EN bit of the PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

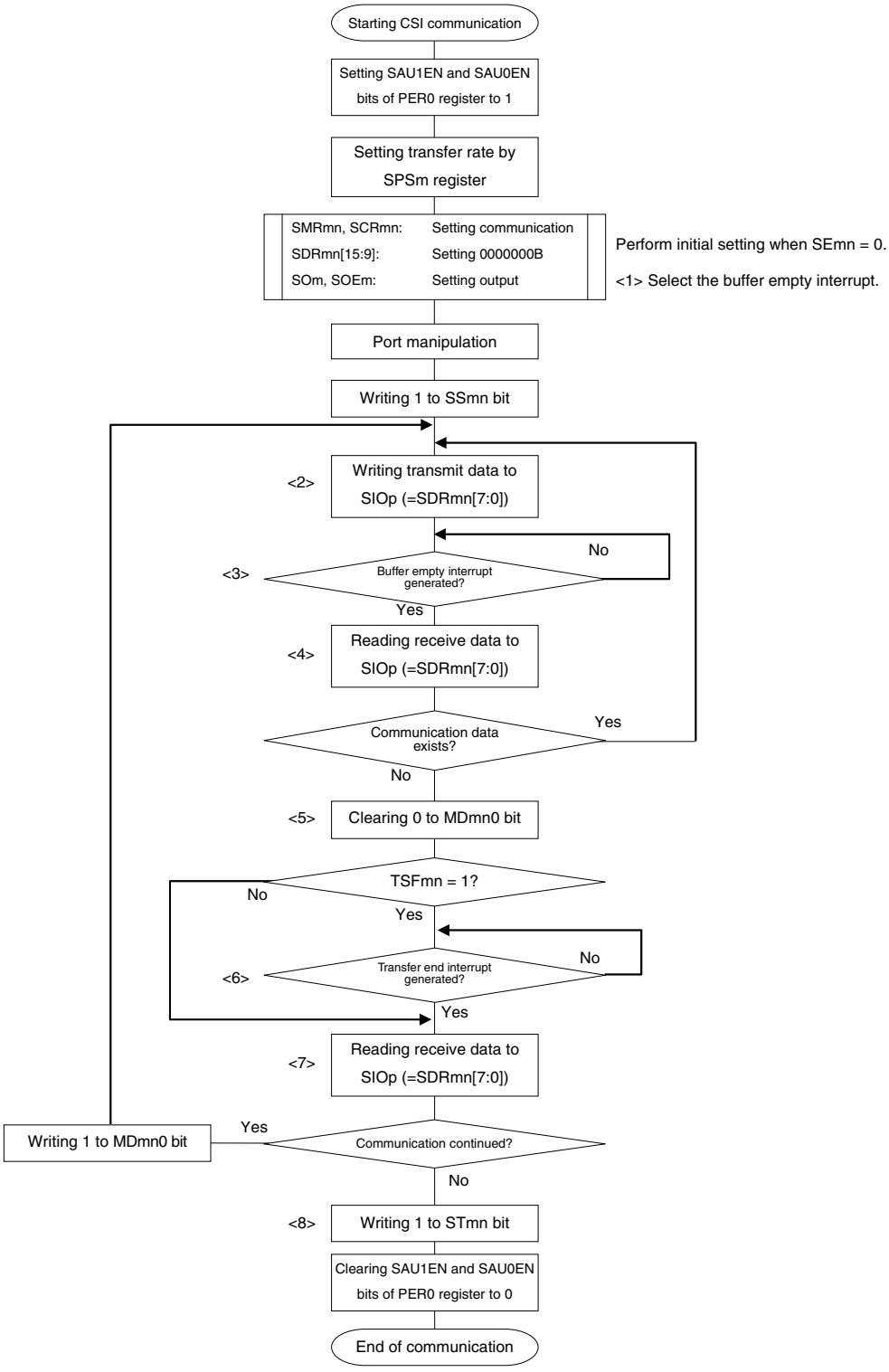
Remark n = 0 to 7

Figure 6-55. Block Diagram of Operation as PWM Function



Remark n = 0, 2, 4, 6
m = n + 1

Figure 12-69. Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)



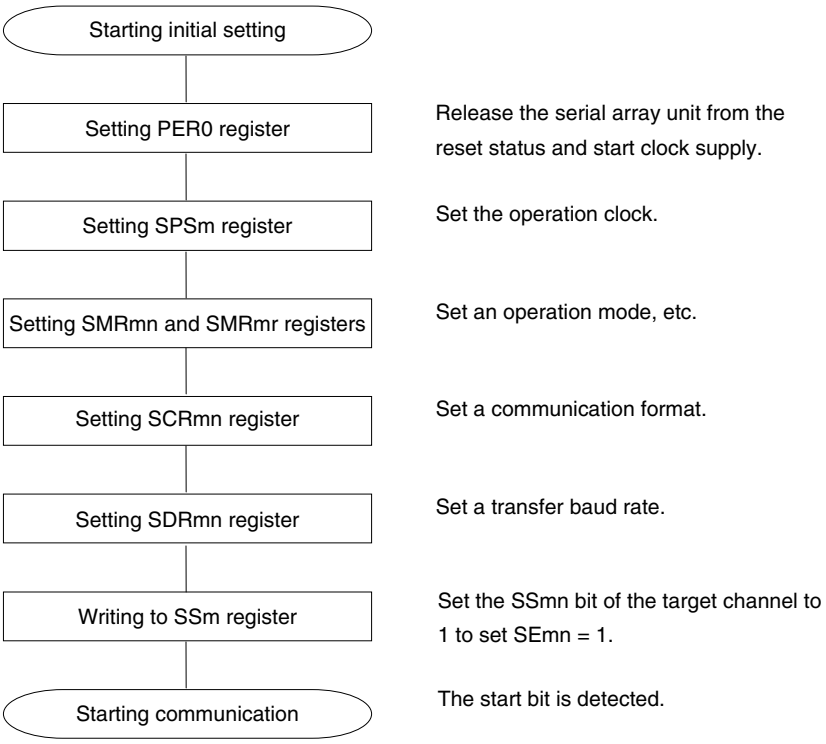
Cautions 1. After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

2. Be sure to set transmit data to the SIOp register before the clock from the master is started.

Remark <1> to <8> in the figure correspond to <1> to <8> in **Figure 12-68 Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)**.

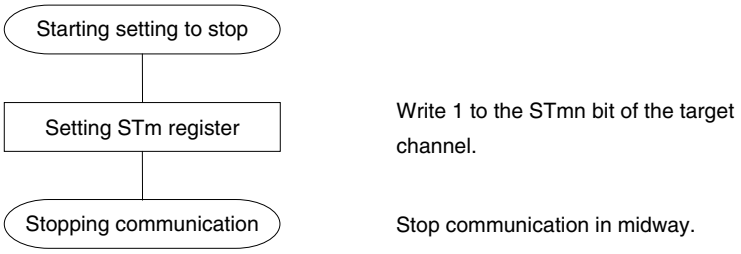
(2) Operation procedure

Figure 12-80. Initial Setting Procedure for UART Reception



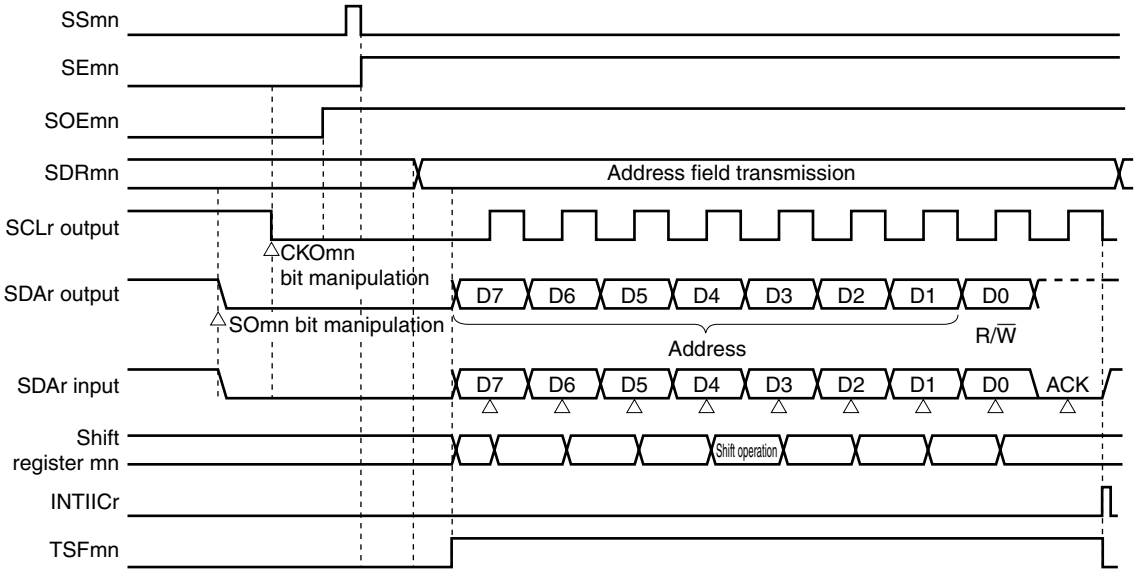
Caution After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

Figure 12-81. Procedure for Stopping UART Reception



(3) Processing flow

Figure 12-95. Timing Chart of Address Field Transmission



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)

Here is an example of setting an IIC transfer rate where MCK = f_{CLK} = 20 MHz.

IIC Transfer Mode (Desired Transfer Rate)	f_{CLK} = 20 MHz			
	Operation Clock (MCK)	SDRmn[15:9]	Calculated Transfer Rate	Error from Desired Transfer Rate
100 kHz	f_{CLK}	99	100 kHz	0.0%
400 kHz	f_{CLK}	24	400 kHz	0.0%

CHAPTER 14 MULTIPLIER

14.1 Functions of Multiplier

The multiplier has the following functions.

- Can execute calculation of 16 bits × 16 bits = 32 bits.

Figure 14-1 shows the block diagram of the multiplier.

Figure 14-1. Block Diagram of Multiplier

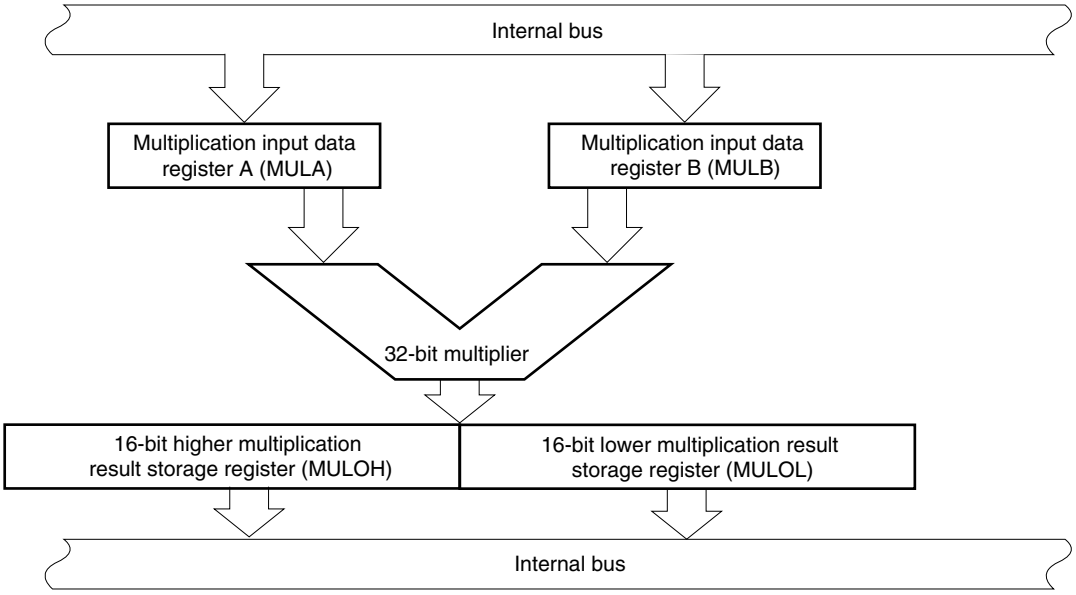


Figure 23-3. Format of Option Byte (000C2H/010C2H)

Address: 000C2H/010C2H[Note]

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1

Note Be sure to set FFH to 000C2H, as these addresses are reserved areas. Also set FFH to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

23.3 Format of On-chip Debug Option Byte

The format of on-chip debug option byte is shown below.

Figure 23-4. Format of On-chip Debug Option Byte (000C3H/010C3H)

Address: 000C3H/010C3H[Note]

7	6	5	4	3	2	1	0
OCDENSET	0	0	0	0	1	0	OCDERSD

OCDENSET	OCDERSD	Control of on-chip debug operation
0	0	Disables on-chip debug operation.
0	1	Setting prohibited
1	0	Enables on-chip debugging. Erases data of flash memory in case of failures in authenticating on-chip debug security ID.
1	1	Enables on-chip debugging. Does not erases data of flash memory in case of failures in authenticating on-chip debug security ID.

Note Set the same value as 000C3H to 010C3H when the boot swap operation is used because 000C3H is replaced by 010C3H.

Caution Bits 7 and 0 (OCDENSET and OCDERSD) can only be specified a value.
Be sure to set 000010B to bits 6 to 1.

Remark The value on bits 3 to 1 will be written over when the on-chip debug function is in use and thus it will become unstable after the setting.
However, be sure to set the default values (0, 1, and 0) to bits 3 to 1 at setting.

Table 27-5. Operation List (2/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit data transfer	MOV	A, [HL + byte]	2	1	4	A ← (HL + byte)	
		[HL + byte], A	2	1	–	(HL + byte) ← A	
		A, [HL + B]	2	1	4	A ← (HL + B)	
		[HL + B], A	2	1	–	(HL + B) ← A	
		A, [HL + C]	2	1	4	A ← (HL + C)	
		[HL + C], A	2	1	–	(HL + C) ← A	
		word[B], #byte	4	1	–	(B + word) ← byte	
		A, word[B]	3	1	4	A ← (B + word)	
		word[B], A	3	1	–	(B + word) ← A	
		word[C], #byte	4	1	–	(C + word) ← byte	
		A, word[C]	3	1	4	A ← (C + word)	
		word[C], A	3	1	–	(C + word) ← A	
		word[BC], #byte	4	1	–	(BC + word) ← byte	
		A, word[BC]	3	1	4	A ← (BC + word)	
		word[BC], A	3	1	–	(BC + word) ← A	
		[SP + byte], #byte	3	1	–	(SP + byte) ← byte	
		A, [SP + byte]	2	1	–	A ← (SP + byte)	
		[SP + byte], A	2	1	–	(SP + byte) ← A	
		B, saddr	2	1	–	B ← (saddr)	
		B, !addr16	3	1	4	B ← (addr16)	
		C, saddr	2	1	–	C ← (saddr)	
		C, !addr16	3	1	4	C ← (addr16)	
		X, saddr	2	1	–	X ← (saddr)	
		X, !addr16	3	1	4	X ← (addr16)	
		ES:!addr16, #byte	5	2	–	(ES, addr16) ← byte	
		A, ES:!addr16	4	2	5	A ← (ES, addr16)	
		ES:!addr16, A	4	2	–	(ES, addr16) ← A	
		A, ES:[DE]	2	2	5	A ← (ES, DE)	
		ES:[DE], A	2	2	–	(ES, DE) ← A	
		ES:[DE + byte],#byte	4	2	–	((ES, DE) + byte) ← byte	
		A, ES:[DE + byte]	3	2	5	A ← ((ES, DE) + byte)	
		ES:[DE + byte], A	3	2	–	((ES, DE) + byte) ← A	

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

(3) X1 oscillation: Ceramic resonator (AMPH = 1, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants		Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Manufacturing Co., Ltd.	CSTCE12M0G55-R0	SMD	12.0	Internal (33)	Internal (33)	1.8	5.5
	CSTCE16M0V53-R0	SMD	16.0	Internal (15)	Internal (15)	1.8	
	CSTLS16M0X51-B0	Lead		Internal (5)	Internal (5)	1.8	
	CSTCE20M0V53-R0	SMD	20.0	Internal (15)	Internal (15)	1.9	
	CSTCG20M0V53-R0	Small SMD		Internal (15)	Internal (15)	2.0	
	CSTLS20M0X51-B0	Lead		Internal (5)	Internal (5)	1.9	
TOKO, Inc.	DCRHYC(P)12.00A	Lead	12.0	Internal (22)	Internal (22)	1.8	5.5
	DCRHZ(P)16.00A-15	Lead	16.0	Internal (15)	Internal (15)		
	DCRHZ(P)20.00A-15	Lead	20.0	Internal (15)	Internal (15)	2.0	
	DECRHZ20.00	SMD		Internal (10)	Internal (10)	1.8	

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

<R> **When doing so, check the conditions for using the AMPH bit, RMC register, and whether to enter or exit the STOP mode.**

The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KF3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

<R> **(4) X1 oscillation: Crystal resonator (AMPH = 1, RMC = 00H, T_A = –40 to +85°C)**

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants		Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
KYOCERA KINSEKI Co., Ltd.	HC49SFWB16000D0PPTZZ	Lead	16.0	10	10	1.8	5.5
	CX49GFWB16000D0PPTZZ						
	CX1255GB16000D0PPTZZ	SMD					
	CX8045GB16000D0PPTZZ						
	CX5032GB16000D0PPTZZ						
	CX5032SB16000D0PPTZZ						
	CX3225GB16000D0PPTZZ						
	CX3225SB16000D0PPTZZ						
	CX2520SB16000D0PPTZZ						
	HC49SFWB20000D0PPTZZ	Lead	20.0	10	10	2.3	
	CX49GFWB20000D0PPTZZ						
	CX1255GB20000D0PPTZZ	SMD					
	CX8045GB20000D0PPTZZ						
	CX5032GB20000D0PPTZZ						
	CX5032SB20000D0PPTZZ						
	CX3225GB20000D0PPTZZ						
	CX3225SB20000D0PPTZZ						
	CX2520SB20000D0PPTZZ						
	CX2016SB20000D0PPTZZ						

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

When doing so, check the conditions for using the AMPH bit, RMC register, and whether to enter or exit the STOP mode.

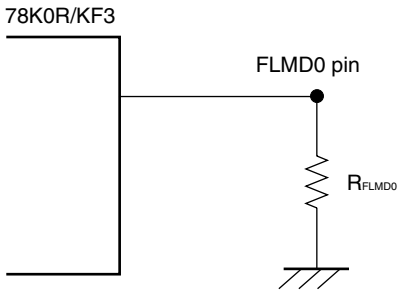
The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KF3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

DC Characteristics (7/12)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF0} ≤ V_{DD}, 1.8 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
On-chip pull-up resistance	R_U	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P55, P64 to P67, P70 to P77, P90, P120, P140 to P145	V_I = V_{SS}, In input port	10	20	100	kΩ
FLMD0 pin external pull-down resistance [Note]	R_{FLMD0}	When enabling the self-programming mode setting with software		100			kΩ

Note It is recommended to leave the FLMD0 pin open. If the pin is required to be pulled down externally, set R_{FLMD0} to 100 kΩ or more.

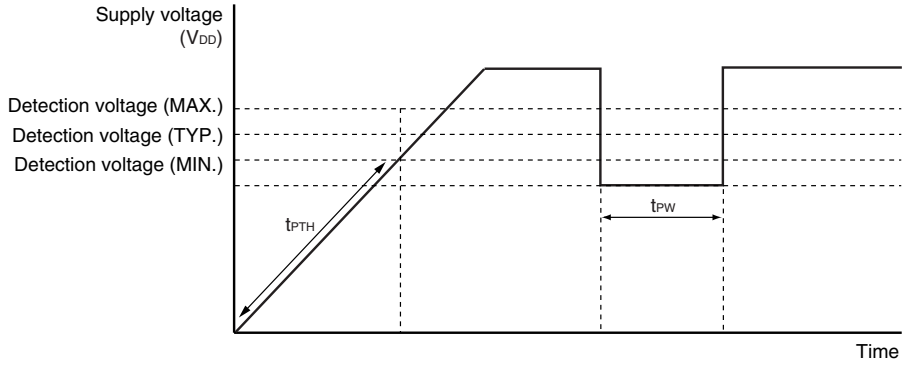


Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

POC Circuit Characteristics (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC0}		1.5	1.59	1.68	V
Power supply voltage rise inclination	t_{PTH}	Change inclination of V_{DD}: 0 V → V_{POC0}	0.5			V/ms
Minimum pulse width	t_{PW}	When the voltage drops	200			μs
Detection delay time					200	μs

POC Circuit Timing



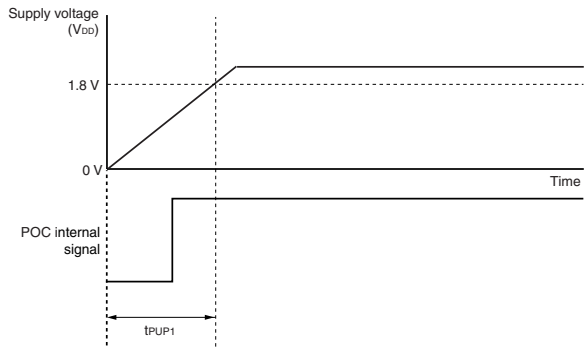
Supply Voltage Rise Time (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 1.8 V (V_{DD} (MIN.))[Note] (V_{DD}: 0 V → 1.8 V)	t_{PUP1}	LVI default start function stopped is set (LVIOFF (Option Byte) = 1), when $\overline{\text{RESET}}$ input is not used			3.6	ms
Maximum time to rise to 1.8 V (V_{DD} (MIN.))[Note] (releasing $\overline{\text{RESET}}$ input → V_{DD}: 1.8 V)	t_{PUP2}	LVI default start function stopped is set (LVIOFF (Option Byte) = 1), when $\overline{\text{RESET}}$ input is used			1.88	ms

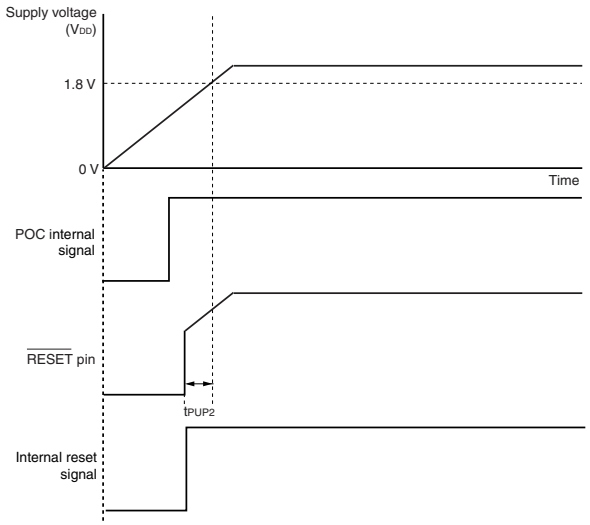
Note Make sure to raise the power supply in a shorter time than this.

Supply Voltage Rise Time Timing

- When $\overline{\text{RESET}}$ pin input is not used



- When $\overline{\text{RESET}}$ pin input is used (when external reset is released by the $\overline{\text{RESET}}$ pin, after POC has been released)



<R> **(2) X1 oscillation: Crystal resonator (AMPH = 0, RMC = 00H, T_A = –40 to +85°C)**

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants		Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
KYOCERA KINSEKI Co., Ltd.	HC49SFWB04194D0PPTZZ	Lead	4.194	10	10	1.8	5.5
	CX49GFWB04194D0PPTZZ						
	CX1255GB04194D0PPTZZ	SMD					
	HC49SFWB05000D0PPTZZ	Lead	5.0	10	10	1.8	
	CX49GFWB05000D0PPTZZ						
	CX1255GB05000D0PPTZZ	SMD					
	CX8045GB05000D0PPTZZ						
	HC49SFWB08380D0PPTZZ	Lead	8.38	10	10	1.8	
	CX49GFWB08380D0PPTZZ						
	CX1255GB08380D0PPTZZ	SMD					
	CX8045GB08380D0PPTZZ						
	CX5032GB08380D0PPTZZ						
	HC49SFWB10000D0PPTZZ	Lead	10.0	10	10	1.8	
	CX49GFWB10000D0PPTZZ						
	CX1255GB10000D0PPTZZ	SMD					
	CX8045GB10000D0PPTZZ						
	CX5032GB10000D0PPTZZ						
	CX5032SB10000D0PPTZZ						
	CX3225GB10000D0PPTZZ						

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

When doing so, check the conditions for using the AMPH bit, RMC register, and whether to enter or exit the STOP mode.

The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KF3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

DC Characteristics (2/12)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF0} ≤ V_{DD}, 1.8 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P02, P05, P06, P10 to P17, P30, P31, P40 to P47, P50 to P55, P64 to P67, P70 to P77, P90, P120, P130, P140, P141, P144, P145	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.5	mA
		Per pin for P03, P04, P142, P143	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.5	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.6	mA
		Per pin for P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			3.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.0	mA
		Total of P00 to P04, P40 to P47, P120, P130, P140 to P145 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P67, P70 to P77, P90 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			45.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty = 60%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			65.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			50.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			29.0	mA
	I_{OL2}	Per pin for P20 to P27	AV_{REF0} ≤ V_{DD}			0.4	mA
		P110, P111	AV_{REF1} ≤ V_{DD}			0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to EV_{SS}, V_{SS}, and AV_{SS} pin.

2. Specification under conditions where the duty factor is 60% or 70%.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OL} = 20.0 mA

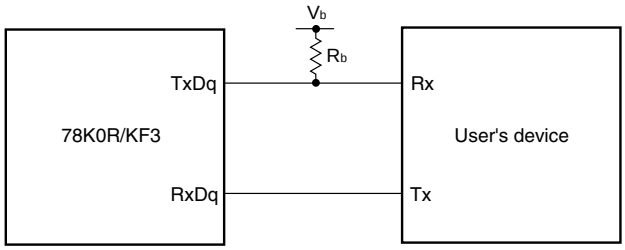
Total output current of pins = (20.0 × 0.7)/(50 × 0.01) = 28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

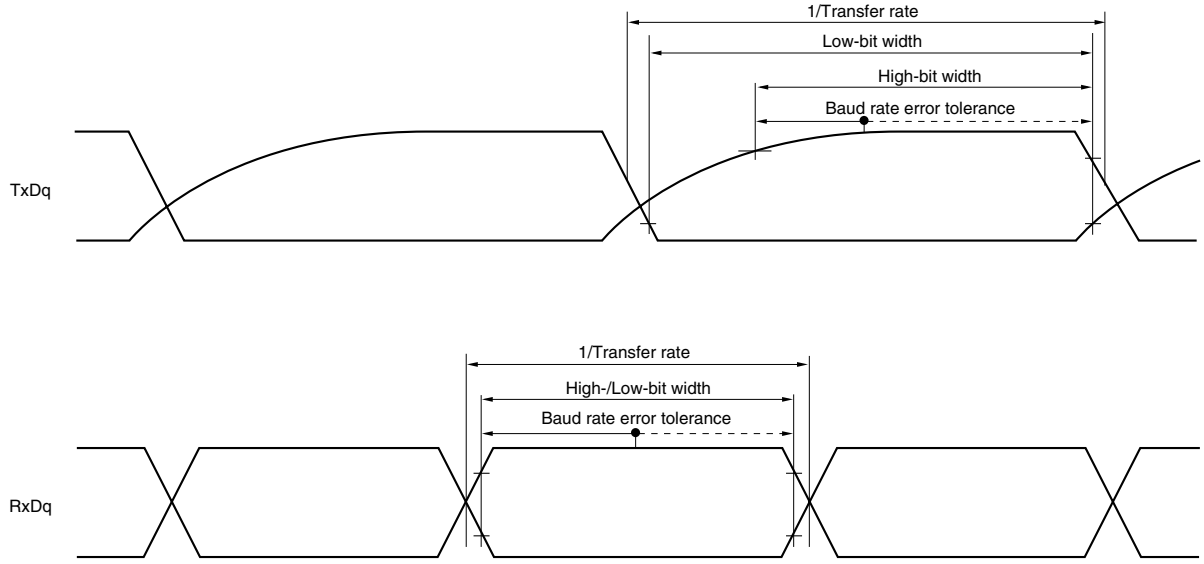
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Serial interface: Serial array unit (10/18)

UART mode connection diagram (During communication at different potential)



UART mode bit width (During communication at different potential)



Caution Select the TTL input buffer for RxDq and the N-ch open drain output (V_{DD} tolerance) mode for TxDq by using the PIMg and POMg registers.

Remarks 1. $R_b[\Omega]$:Communication line (TxDq) pull-up resistance, $V_b[V]$: Communication line voltage

2. q: UART number (q = 1, 2), g: PIM and POM number (g = 0, 14)

3. UART0 and UART3 cannot communicate at different potential. Use UART1 and UART2 for communication at different potential.