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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1155agk-gak-ax

2.2.9 P90 (port 9)

P90 function as an 1-bit I/O port.

The port mode can be specified in 1-bit units.

(1) Port mode

P90 function as an 1-bit I/O port. P90 can be set to input or output port in 1-bit units using port mode register 9 (PM9). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 9 (PU9).

2.2.10 P110, P111 (port 11)

P110 and P111 function as a 2-bit I/O port. These pins also function as D/A converter analog output.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P110 and P111 function as a 2-bit I/O port. P110 and P111 can be set to input or output port in 1-bit units using port mode register 11 (PM11).

(2) Control mode

P110 and P111 function as D/A converter analog output pins (ANO0, ANO1). When using these pins as analog input pins, see **11.4.3 Cautions**.

2.2.11 P120 to P124 (port 12)

P120 functions as a 1-bit I/O port. P121 to P124 function as a 4-bit input port. These pins also function as external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, and external clock input for main system clock.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P120 functions as a 1-bit I/O port. P120 can be set to input or output port using port mode register 12 (PM12). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

P121 to P124 function as a 4-bit input port.

(2) Control mode

P120 to P124 function as external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, and external clock input for main system clock.

(a) INTP0

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) EXLVI

This is a potential input pin for external low-voltage detection.

(c) X1, X2

These are the pins for connecting a resonator for main system clock.

(d) EXCLK

This is an external clock input pin for main system clock.

3.4 Addressing for Processing Data Addresses

3.4.1 Implied addressing

[Function]

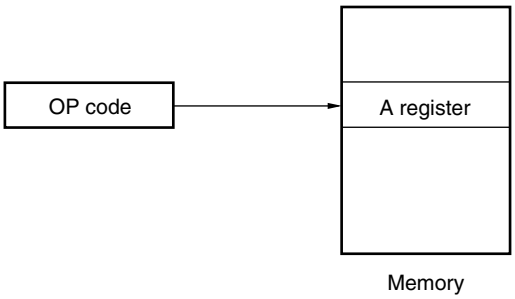
Instructions for accessing registers (such as accumulators) that have special functions are directly specified with the instruction word, without using any register specification field in the instruction word.

[Operand format]

Because implied addressing can be automatically employed with an instruction, no particular operand format is necessary.

Implied addressing can be applied only to MULU X.

Figure 3-23. Outline of Implied Addressing



3.4.2 Register addressing

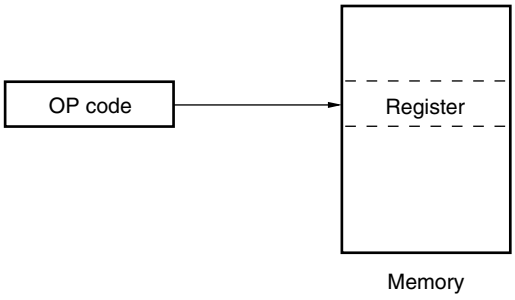
[Function]

Register addressing accesses a general-purpose register as an operand. The instruction word of 3-bit long is used to select an 8-bit register and the instruction word of 2-bit long is used to select a 16-bit register.

[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

Figure 3-24. Outline of Register Addressing



3.4.5 SFR addressing

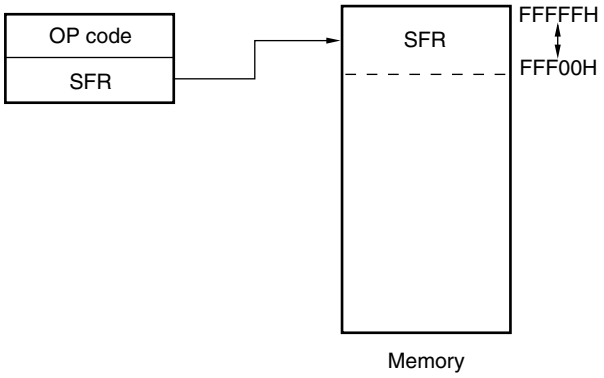
[Function]

SFR addressing directly specifies the target SFR addresses using 8-bit data in the instruction word. This type of addressing is applied only to the space from FFF00H to FFFFFH.

[Operand format]

Identifier	Description
SFR	SFR name
SFRP	16-bit-manipulatable SFR name (even address only)

Figure 3-28. Outline of SFR Addressing



3.4.8 Based indexed addressing

[Function]

Based indexed addressing uses the contents of a register pair specified with the instruction word as the base address, and the content of the B register or C register similarly specified with the instruction word as offset address. The sum of these values is used to specify the target address.

[Operand format]

Identifier	Description
–	[HL+B], [HL+C] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[HL+B], ES:[HL+C] (higher 4-bit addresses are specified by the ES register)

Figure 3-38. Example of [HL+B], [HL+C]

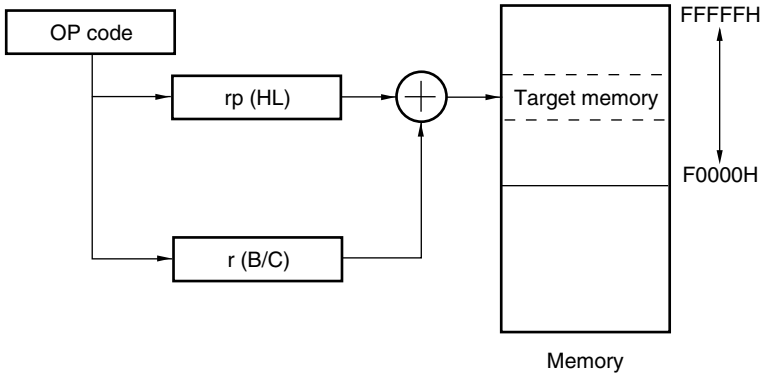
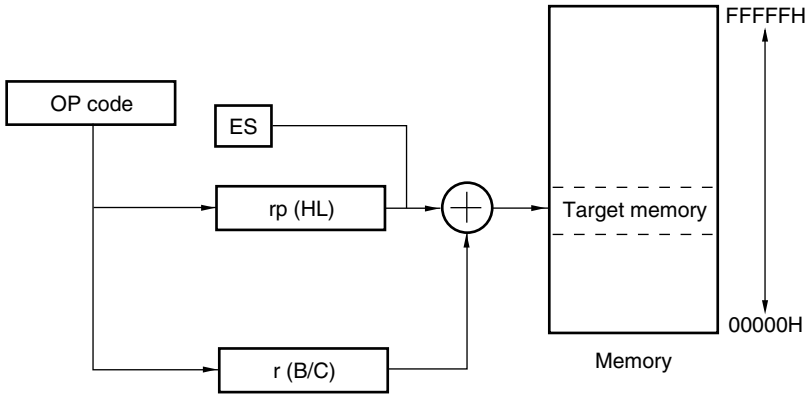


Figure 3-39. Example of ES:[HL+B], ES:[HL+C]



(e) Start timing in capture & one-count mode

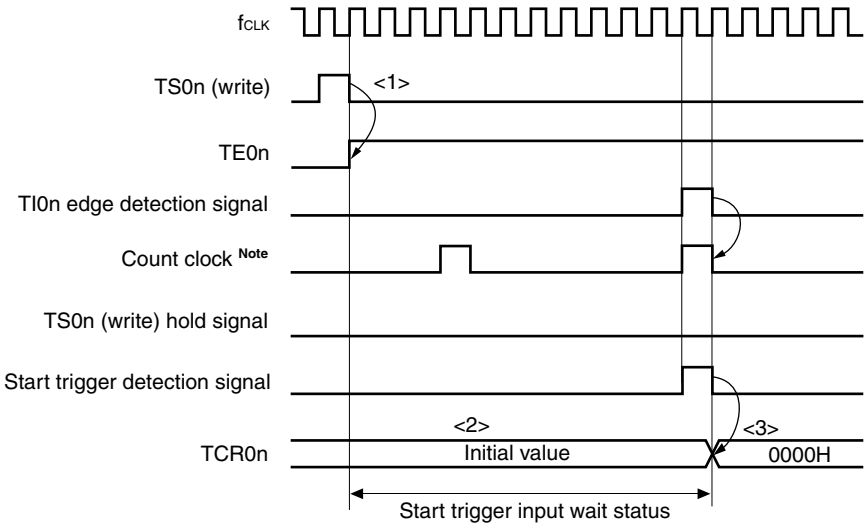
<1> Writing 1 to TS0n sets TE0n = 1

<2> Enters the start trigger input wait status, and TCR0n holds the initial value.

<3> On start trigger detection, 0000H is loaded to TCR0n and count starts.

Figure 6-14. Start Timing (In Capture & One-count Mode)

<R>



Note When the capture & one-count mode is set, the operation clock (MCK) is selected as count clock (CCS0n = 0).

Caution An input signal sampling error is generated since operation starts upon start trigger detection (The error is one count clock when TI0n is used).

Figure 7-3. Format of Real-Time Counter Control Register 0 (RTCC0)

Address: FFF9DH After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	3	2	1	0
RTCC0	RTCE	0	RCLOE1	RCLOE0	AMPM	CT2	CT1	CT0

RTCE	Real-time counter operation control
0	Stops counter operation.
1	Starts counter operation.

RCLOE1	RTC1HZ pin output control
0	Disables output of RTC1HZ pin (1 Hz).
1	Enables output of RTC1HZ pin (1 Hz).

RCLOE0[Note]	RTCCL pin output control
0	Disables output of RTCCL pin (32.768 kHz).
1	Enables output of RTCCL pin (32.768 kHz).

AMPM	Selection of 12-/24-hour system
0	12-hour system (a.m. and p.m. are displayed.)
1	24-hour system
Rewrite the AMPM value after setting RWAIT (bit 0 of RTCC1) to 1. If the AMPM value is changed, the values of the hour count register (HOUR) change according to the specified time system. Table 7-2 shows the displayed time digits.	

<R>

CT2	CT1	CT0	Constant-period interrupt (INTRTC) selection
0	0	0	Does not use constant-period interrupt function.
0	0	1	Once per 0.5 s (synchronized with second count up)
0	1	0	Once per 1 s (same time as second count up)
0	1	1	Once per 1 m (second 00 of every minute)
1	0	0	Once per 1 hour (minute 00 and second 00 of every hour)
1	0	1	Once per 1 day (hour 00, minute 00, and second 00 of every day)
1	1	×	Once per 1 month (Day 1, hour 00 a.m., minute 00, and second 00 of every month)
When changing the values of CT2 to CT0 while the counter operates (RTCE = 1), rewrite the values of CT2 to CT0 after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, after rewriting the values of CT2 to CT0, enable interrupt servicing after clearing the RIFG and RTCIF flags.			

Note RCLOE0 and RCLOE2 must not be enabled at the same time.

Caution If RCLOE0 and RCLOE1 are changed when RTCE = 1, glitches may occur in the 32.768 kHz and 1 Hz output signals.

Remark ×: don't care

10.7 Cautions for A/D Converter

(1) Operating current in STOP mode

Shift to STOP mode after clearing the A/D converter (by clearing bit 7 (ADCS) of the A/D converter mode register (ADM) to 0). The operating current can be reduced by clearing bit 0 (ADCE) of the A/D converter mode register (ADM) to 0 at the same time.

To restart from the standby status, clear bit 0 (ADIF) of interrupt request flag register 1L (IF1L) to 0 and start operation.

(2) Reducing current when A/D converter is stopped

Be sure that the voltage to be applied to AV_{REF0} normally satisfies the conditions stated in Table 10-1.

If bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) are set to 0, the current will not be increased by the A/D converter even if a voltage is applied to AV_{REF0}, while the A/D converter is stopped. If a current flows from the power supply that supplies a voltage to AV_{REF0} to an external circuit of the microcontroller as shown in Figure 10-25, AV_{REF0} = 0 V = AV_{SS} can be achieved and the external current can be reduced by satisfying the following conditions.

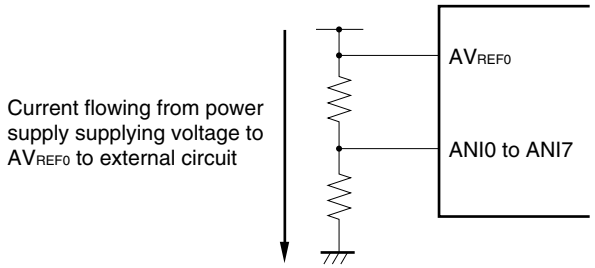
Set the following states before setting AV_{REF0} = 0 V.

- Set ADCS and ADCE of the A/D converter mode register (ADM) to 0.
- Set the port mode registers (PM20 to PM27) of the digital I/O pins to 1 to set to input mode, or set the digital I/O pins to low-level output (high-level output disabled) by setting the port mode registers (PM20 to PM27) and port registers (P20 to P27) to 0 to set to output mode.
- Make sure that no voltage is applied to all any of the analog or digital pins (P20/ANI0 to P27/ANI7) (set to 0 V).

Do not perform the following operation when AV_{REF0} = 0 V.

- Do not access the port registers (P20 to P27) or port mode registers (PM20 to PM27) by using instructions or via DMA transfer.

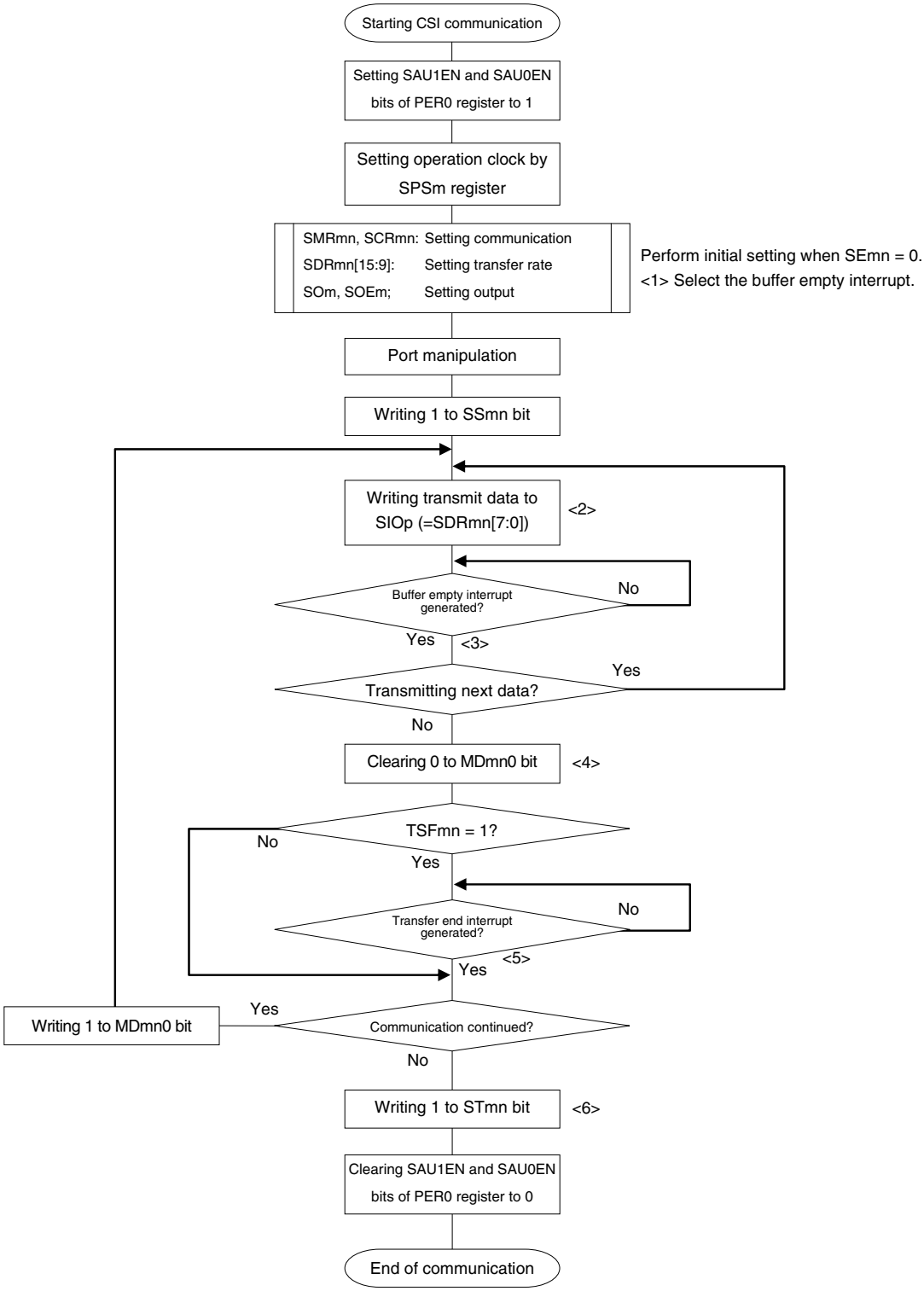
Figure 10-25. Example of Circuit Where Current Flows to External Circuit



When restarting the A/D converter, operate it after the AV_{REF0} voltage rises and stabilizes and setting ADCE = 1 (see **10.4.1 Basic operations of A/D converter** for the procedure for setting the A/D converter operation). Access digital ports after the AV_{REF0} voltage has risen and stabilized.

<R> Stop the conversion performed by the D/A converter when the AV_{REF0} voltage is rising or falling.

Figure 12-31. Flowchart of Master Transmission (in Continuous Transmission Mode)



Caution After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

Remark <1> to <6> in the figure correspond to <1> to <6> in **Figure 12-30 Timing Chart of Master Transmission (in Continuous Transmission Mode)**.

12.5.4 Slave transmission

Slave transmission is that the 78K0R/KF3 transmits data to another device in the state of a transfer clock being input from another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI20
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	$\overline{SCK00}$, SO00	$\overline{SCK01}$, SO01	$\overline{SCK10}$, SO10	$\overline{SCK20}$, SO20
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI20
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.			
Error detection flag	Overrun error detection flag (OVFmn) only			
Transfer data length	7 or 8 bits			
Transfer rate	Max. f_{MCK}/6 [Hz] Notes 1, 2			
Data phase	Selectable by DAPmn bit • DAPmn = 0: Data output starts from the start of the operation of the serial clock. • DAPmn = 1: Data output starts half a clock before the start of the serial clock operation.			
Clock phase	Selectable by CKPmn bit • CKPmn = 0: Forward • CKPmn = 1: Reverse			
Data direction	MSB or LSB first			

Notes 1. Because the external serial clock input to pins $\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, and $\overline{SCK20}$ is sampled internally and used, the fastest transfer rate is f_{MCK}/6 [Hz].

2. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 28 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) and CHAPTER 29 ELECTRICAL SPECIFICATIONS ((A) GRADE PRODUCTS)**).

Remarks 1. f_{MCK}: Operation clock (MCK) frequency of target channel

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2)

Table 12-7. Relationship between register settings and pins (Channel 2 of unit 0: CSI10, UART1 transmission, IIC10)

SE02 Note1	MD022	MD021	SOE02	SO02	CKO02	TXE02	RXE02	PM04	P04	PM03 Note2	P03 Note2	PM02	P02	Operation mode	Pin Function		
															$\overline{SCK10}$/SCL10/P04	SI10/SDA10/RxD1/P03 Note2	SO10/TxD1/P02
0	0	0	0	1	1	0	0	× Note3	× Note3	× Note3	× Note3	× Note3	× Note3	Operation stop mode	P04	P03	P02
	0	1														P03/RxD1	
	1	0														P03	
1	0	0	0	1	1	0	1	1	×	1	×	× Note3	× Note3	Slave CSI10 reception	$\overline{SCK10}$ (input)	SI10	P02
			1	0/1 Note4	1	1	0	1	×	× Note3	× Note3	0	1	Slave CSI10 transmission	$\overline{SCK10}$ (input)	P03	SO10
			1	0/1 Note4	1	1	1	1	×	1	×	0	1	Slave CSI10 transmission /reception	$\overline{SCK10}$ (input)	SI10	SO10
			0	1	0/1 Note4	0	1	0	1	1	×	× Note3	× Note3	Master CSI10 reception	$\overline{SCK10}$ (output)	SI10	P02
			1	0/1 Note4	0/1 Note4	1	0	0	1	× Note3	× Note3	0	1	Master CSI10 transmission	$\overline{SCK10}$ (output)	P03	SO10
			1	0/1 Note4	0/1 Note4	1	1	0	1	1	×	0	1	Master CSI10 transmission /reception	$\overline{SCK10}$ (output)	SI10	SO10
	0	1	1	0/1 Note4	1	1	0	× Note3	× Note3	× Note3	× Note3	0	1	UART1 transmission Note5	P04	P03/RxD1	TxD1
0	1	0	0	0/1 Note6	0/1 Note6	0	0	0	1	0	1	× Note3	× Note3	IIC10 start condition	SCL10	SDA10	P02
						1	0										
						0	1										
1			1	0/1 Note4	0/1 Note4	1	0	0	1	0	1	× Note3	× Note3	IIC10 address field transmission	SCL10	SDA10	P02
			1	0/1 Note4	0/1 Note4	1	0	0	1	0	1	× Note3	× Note3	IIC10 data transmission	SCL10	SDA10	P02
			1	0/1 Note4	0/1 Note4	0	1	0	1	0	1	× Note3	× Note3	IIC10 data reception	SCL10	SDA10	P02
0			0	0/1 Note7	0/1 Note7	0	0	0	1	0	1	× Note3	× Note3	IIC10 stop condition	SCL10	SDA10	P02
						1	0										
						0	1										

Notes 1. The SE0 register is a read-only status register which is set using the SS0 and ST0 registers.

2. When channel 3 of unit 0 is set to UART1 reception, this pin becomes an RxD1 function pin (refer to **Table 12-8**). In this case, operation stop mode or UART1 transmission must be selected for channel 2 of unit 0.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **12.3 (12) Serial output register m (SOm)**.

5. When using UART1 transmission and reception in a pair, set channel 3 of unit 0 to UART1 reception (refer to **Table 12-8**).

6. Set the CKO02 bit to 1 before a start condition is generated. Clear the SO02 bit from 1 to 0 when the start condition is generated.

7. Set the CKO02 bit to 1 before a stop condition is generated. Clear the SO02 bit from 0 to 1 when the stop condition is generated.

Remark X: Don't care

Table 13-3. Selection Clock Setting

IICX0	IICCL0			Transfer Clock (f_{CLK}/m)	Settable Selection Clock (f_{CLK}) Range	Operation Mode
Bit 0	Bit 3	Bit 1	Bit 0			
CLX0	SMC0	CL01	CL00			
0	0	0	0	f_{CLK}/88	4.00 MHz to 8.4 MHz	Normal mode (SMC0 bit = 0)
0	0	0	1	f_{CLK}/172	8.38 MHz to 16.76 MHz	
0	0	1	0	f_{CLK}/344	16.76 MHz to 20 MHz	
0	0	1	1	f_{CLK}/44	2.00 MHz to 4.2 MHz	
0	1	0	×	f_{CLK}/48	7.60 MHz to 16.76 MHz	Fast mode (SMC0 bit = 1)
0	1	1	0	f_{CLK}/96	16.00 MHz to 20 MHz	
0	1	1	1	f_{CLK}/24	4.00 MHz to 8.4 MHz	
1	0	×	×	Setting prohibited		
1	1	0	×	f_{CLK}/48	8.00 MHz to 8.38 MHz	Fast mode (SMC0 bit = 1)
1	1	1	0	Setting prohibited	16.00 MHz to 16.76 MHz	
1	1	1	1	f_{CLK}/24	4.00 MHz to 4.19 MHz	

Caution Determine the transfer clock frequency of I^2C by using CLX0, SMC0, CL01, and CL00 before enabling the operation (by setting bit 7 (IICE0) of IIC control register 0 (IICC0) to 1). To change the transfer clock frequency, clear IICE0 once to 0.

Remarks 1. ×: don't care

2. f_{CLK}: CPU/peripheral hardware clock frequency

13.5.5 Acknowledge ($\overline{ACK}$)

$\overline{ACK}$ is used to check the status of serial data at the transmission and reception sides.

The reception side returns $\overline{ACK}$ each time it has received 8-bit data.

The transmission side usually receives $\overline{ACK}$ after transmitting 8-bit data. When $\overline{ACK}$ is returned from the reception side, it is assumed that reception has been correctly performed and processing is continued. Whether $\overline{ACK}$ has been detected can be checked by using bit 2 (ACKD0) of IIC status register 0 (IICS0).

When the master receives the last data item, it does not return $\overline{ACK}$ and instead generates a stop condition. If a slave does not return $\overline{ACK}$ after receiving data, the master outputs a stop condition or restart condition and stops transmission. If $\overline{ACK}$ is not returned, the possible causes are as follows.

<1> Reception was not performed normally.

<2> The final data item was received.

<3> The reception side specified by the address does not exist.

To generate $\overline{ACK}$, the reception side makes the SDA0 line low at the ninth clock (indicating normal reception).

Automatic generation of $\overline{ACK}$ is enabled by setting bit 2 (ACKE0) of IIC control register 0 (IICC0) to 1. Bit 3 (TRC0) of the IICS0 register is set by the data of the eighth bit that follows 7-bit address information. Usually, set ACKE0 to 1 for reception (TRC0 = 0).

If a slave can receive no more data during reception (TRC0 = 0) or does not require the next data item, then the slave must inform the master, by clearing ACKE0 to 0, that it will not receive any more data.

When the master does not require the next data item during reception (TRC0 = 0), it must clear ACKE0 to 0 so that $\overline{ACK}$ is not generated. In this way, the master informs a slave at the transmission side that it does not require any more data (transmission will be stopped).

<R> **15.5.2 CSI master reception**

A flowchart showing an example of setting for CSI master reception is shown below.

- Master reception (256 KB) of CSI00
- DMA channel 0 is used to read received data and DMA channel 1 is used to write dummy data.
- DMA start source: INTCSI00
  (If the same start source is specified for DMA channels 0 and 1, the data of channel 0 is transferred, and then that of channel 1.)
- Interrupt of CSI00 is specified by IFC03 to IFC00 = IFC13 to IFC10 (bits 3 to 0 of the DMCn register) = 0110B.
- Data is transferred (received) from FFF10H of the CSI data register (SIO00) to FF100H to FF1FFH of RAM (256 bytes). (In successive reception mode, the data that is to be received when the first buffer empty interrupt occurs is invalid because the data has not been received.)
- Transfers dummy data FF101H to FF1FFH (255 bytes) of RAM to FFF10H of the data register (SIO00) of CSI. (Dummy data is written to the first byte by using software (an instruction).)

16.3 Registers Controlling Interrupt Functions

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)
- Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)
- Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H)
- External interrupt rising edge enable registers (EGP0, EGP1)
- External interrupt falling edge enable registers (EGN0, EGN1)
- Program status word (PSW)

Table 16-2 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 16-2. Flags Corresponding to Interrupt Request Sources (1/2)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTWDTI	WDTIIF	IF0L	WDTIMK	MK0L	WDTIPR0, WDTIPR1	PR00L, PR10L
INTLVI	LVIIF		LVIMK		LVIPR0, LVIPR1	
INTP0	PIF0		PMK0		PPR00, PPR10	
INTP1	PIF1		PMK1		PPR01, PPR11	
INTP2	PIF2		PMK2		PPR02, PPR12	
INTP3	PIF3		PMK3		PPR03, PPR13	
INTP4	PIF4		PMK4		PPR04, PPR14	
INTP5	PIF5		PMK5		PPR05, PPR15	
INTST3	STIF3	IF0H	STMK3	MK0H	STPR03, STPR13	PR00H, PR10H
INTSR3	SRIF3		SRMK3		SRPR03, SRPR13	
INTSRE3	SREIF3		SREMK3		SREPR03, SREPR13	
INTDMA0	DMAIF0		DMAMK0		DMAPR00, DMAPR10	
INTDMA1	DMAIF1		DMAMK1		DMAPR01, DMAPR11	
INTST0 Note 1	STIF0 Note 1		STMK0 Note 1		STPR00, STPR10 Note 1	
INTCSI00 Note 1	CSIIF00 Note 1		CSIMK00 Note 1		CSIPR000, CSIPR100 Note1	
INTSR0 Note 2	SRIF0 Note 2		SRMK0 Note 2		SRPR00, SRPR10 Note 2	
INTCSI01 Note 2	CSIIF01 Note 2		CSIMK01 Note 2		CSIPR001, CSIPR101 Note2	
INTSRE0	SREIF0		SREMK0		SREPR00, SREPR10	

Notes 1. Do not use UART0 and CSI00 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INTST0 and INTCSI00 is generated, bit 5 of IF1H is set to 1. Bit 5 of MK0H, PR00H, and PR10H supports these two interrupt sources.

2. Do not use UART0 and CSI01 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INTSR0 and INTCSI01 is generated, bit 6 of IF0H is set to 1. Bit 6 of MK0H, PR00H, and PR10H supports these two interrupt sources.

Table 18-2. Operating Statuses in STOP Mode

STOP Mode Setting / Item			When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
			When CPU Is Operating on Internal High-Speed Oscillation Clock (f_{IH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{IH}	Stopped		
		f_X			
		f_{EX}			
	Subsystem clock	f_{XT}	Status before STOP mode was set is retained		
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WTON) of option byte (000C0H) • WTON = 0: Stops • WTON = 1 and WDSTBYON = 1: Oscillates • WTON = 1 and WDSTBYON = 0: Stops		
CPU			Operation stopped		
Flash memory			Operation stopped		
RAM			Operation stopped. However, status before STOP mode was set is retained at voltage higher than POC detection voltage.		
Port (latch)			Status before STOP mode was set is retained		
Timer array unit (TAU)			Operation stopped		
Real-time counter (RTC)			Operable		
Watchdog timer			Set by bits 0 (WDSTBYON) and 4 (WTON) of option byte (000C0H) • WTON = 0: Stops • WTON = 1 and WDSTBYON = 1: Operates • WTON = 1 and WDSTBYON = 0: Stops		
Clock output/buzzer output			Operable only when subsystem clock is selected as the count clock		
A/D converter			Operation stopped		
D/A converter			Operation stopped (the pin in Hi-Z status)		
Serial array unit (SAU)			Operation stopped		
Serial interface (IIC0)					
Multiplier					
DMA controller					
Power-on-clear function			Operable		
Low-voltage detection function					
External interrupt					
Key interrupt function					

Remark f_{IH}: Internal high-speed oscillation clock
f_X: X1 clock
f_{EX}: External main system clock
f_{XT}: XT1 clock
f_{IL}: Internal low-speed oscillation clock

27.2 Operation List

Table 27-5. Operation List (1/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	MOV	r, #byte	2	1	–	r ← byte			
		saddr, #byte	3	1	–	(saddr) ← byte			
		sfr, #byte	3	1	–	sfr ← byte			
		!addr16, #byte	4	1	–	(addr16) ← byte			
		A, r Note 3	1	1	–	A ← r			
		r, A Note 3	1	1	–	r ← A			
		A, saddr	2	1	–	A ← (saddr)			
		saddr, A	2	1	–	(saddr) ← A			
		A, sfr	2	1	–	A ← sfr			
		sfr, A	2	1	–	sfr ← A			
		A, !addr16	3	1	4	A ← (addr16)			
		!addr16, A	3	1	–	(addr16) ← A			
		PSW, #byte	3	3	–	PSW ← byte	×	×	×
		A, PSW	2	1	–	A ← PSW			
		PSW, A	2	3	–	PSW ← A	×	×	×
		ES, #byte	2	1	–	ES ← byte			
		ES, saddr	3	1	–	ES ← (saddr)			
		A, ES	2	1	–	A ← ES			
		ES, A	2	1	–	ES ← A			
		CS, #byte	3	1	–	CS ← byte			
		A, CS	2	1	–	A ← CS			
		CS, A	2	1	–	CS ← A			
		A, [DE]	1	1	4	A ← (DE)			
		[DE], A	1	1	–	(DE) ← A			
		[DE + byte], #byte	3	1	–	(DE + byte) ← byte			
		A, [DE + byte]	2	1	4	A ← (DE + byte)			
		[DE + byte], A	2	1	–	(DE + byte) ← A			
		A, [HL]	1	1	4	A ← (HL)			
		[HL], A	1	1	–	(HL) ← A			
		[HL + byte], #byte	3	1	–	(HL + byte) ← byte			

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. Except r = A

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P55, P64 to P67, P70 to P77, P90, P120, P130, P140 to P145	−10	mA
		Total of all pins −80 mA	P00 to P04, P40 to P47, P120, P130, P140 to P145	−25	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P64 to P67, P70 to P77, P90	−55	mA
	I_{OH2}	Per pin	P20 to P27, P110, P111	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P55, P60 to P67, P70 to P77, P90, P120, P130, P140 to P145	30	mA
		Total of all pins 200 mA	P00 to P04, P40 to P47, P120, P130, P140 to P145	60	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P67, P70 to P77, P90	140	mA
	I_{OL2}	Per pin	P20 to P27, P110, P111	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

A/D Converter Characteristics (1/2)

(T_A = –40 to +85°C, 2.3 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 2.3 V ≤ AV_{REF0} ≤ V_{DD}, 1.8 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

(a) Conventional-specification products (μPD78F115x)

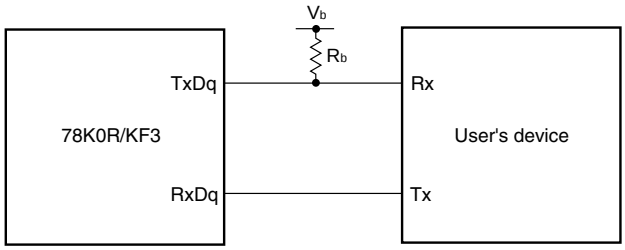
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				10	bit
Overall error[Notes 1, 2]	AINL	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF0} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF0} < 2.7 V			±0.7	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF0} ≤ 5.5 V	6.1		66.6	μs
		2.7 V ≤ AV_{REF0} < 4.0 V	12.2		66.6	μs
		2.3 V ≤ AV_{REF0} < 2.7 V	27		66.6	μs
Zero-scale error[Notes 1, 2]	EZS	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF0} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF0} < 2.7 V			±0.6	%FSR
Full-scale error[Notes 1, 2]	EFS	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF0} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF0} < 2.7 V			±0.6	%FSR
Integral linearity error[Note 1]	ILE	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF0} < 4.0 V			±4.5	LSB
		2.3 V ≤ AV_{REF0} < 2.7 V			±4.5	LSB
Differential linearity error[Note 1]	DLE	4.0 V ≤ AV_{REF0} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF0} < 4.0 V			±2.0	LSB
		2.3 V ≤ AV_{REF0} < 2.7 V			±2.0	LSB
Analog input voltage	V_{AIN}	2.3 V ≤ AV_{REF0} ≤ 5.5 V	AV_{SS}		AV_{REF0}	V

Notes 1. Excludes quantization error (±1/2 LSB).

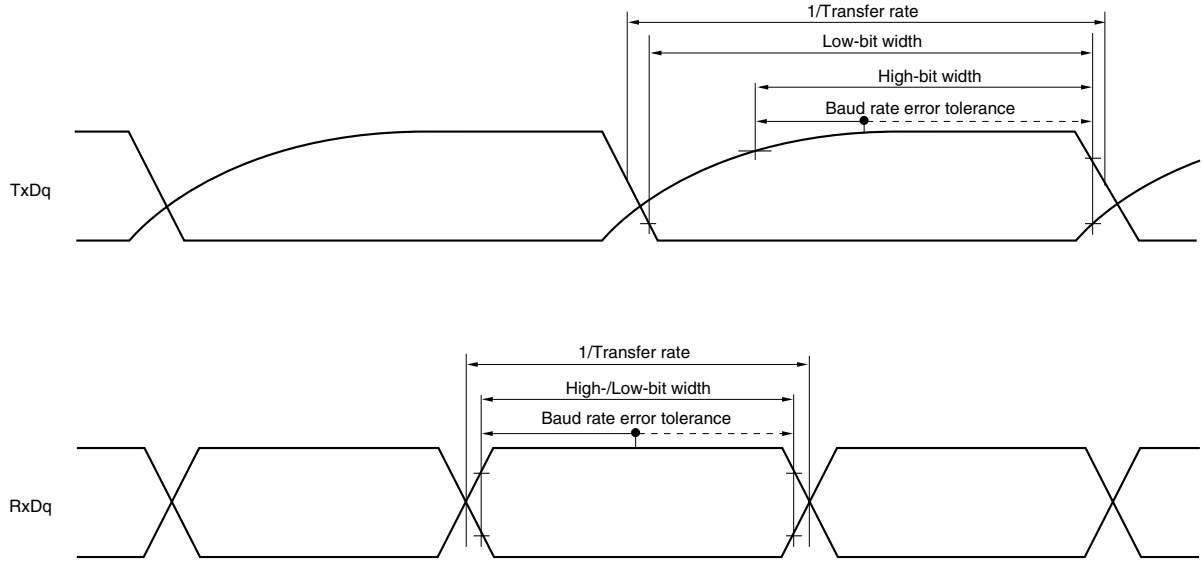
2. This value is indicated as a ratio (%FSR) to the full-scale value.

(2) Serial interface: Serial array unit (10/18)

UART mode connection diagram (During communication at different potential)



UART mode bit width (During communication at different potential)



Caution Select the TTL input buffer for RxDq and the N-ch open drain output (V_{DD} tolerance) mode for TxDq by using the PIMg and POMg registers.

Remarks 1. $R_b[\Omega]$:Communication line (TxDq) pull-up resistance, $V_b[V]$: Communication line voltage

2. q: UART number (q = 1, 2), g: PIM and POM number (g = 0, 14)

3. UART0 and UART3 cannot communicate at different potential. Use UART1 and UART2 for communication at different potential.

A.5.2 When using on-chip debug emulator with programming function QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This on-chip debug emulator serves to debug hardware and software when developing application systems using the 78K0R microcontrollers. It is available also as flash memory programmer dedicated to microcontrollers with on-chip flash memory. The QB-MINI2 is supplied with a USB interface cable and connection cables (10-pin cable and 16-pin cable), and the 78K0-OCD board. To use 78K0R/KF3, use USB interface cable and 16-pin connection cable.

Remark Download the software for operating the QB-MINI2 from the download site for MINICUBE2 (http://www.necel.com/micro/en/development/asia/minicube2/minicube2.html).

A.6 Debugging Tools (Software)

SM+ for 78K0R System simulator	SM+ for 78K0R is Windows-based software. It is used to perform debugging at the C source level or assembler level while simulating the operation of the target system on a host machine. Use of SM+ for 78K0R allows the execution of application logical testing and performance testing on an independent basis from hardware development, thereby providing higher development efficiency and software quality. SM+ for 78K0R should be used in combination with the device file (DF781188).
	Part number: μS××××SM781000
ID78K0R-QB Integrated debugger	This debugger supports the in-circuit emulators for the 78K0R microcontrollers. The ID78K0R-QB is Windows-based software. It has improved C-compatible debugging functions and can display the results of tracing with the source program using an integrating window function that associates the source program, disassemble display, and memory display with the trace result. ID78K0R-QB should be used in combination with the device file.
	Part number: μS××××ID78K0R-QB

Remark ×××× in the part number differs depending on the host machine and OS used.

μS××××SM781000
μS××××ID78K0R-QB

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	CD-ROM
BB17		Windows (English version)	

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 28	Hard	Electrical specifications (standard products)	Recommended oscillator constants	The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. When doing so, check the conditions for using the RMC register, and whether to enter or exit the STOP mode. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KF3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.	p.735 ☐
			DC characteristics	P02 to P04, P43, P45, P142 to P144 do not output high level in N-ch open-drain mode.	p.736 ☐
				The maximum value of V_{IH} of pins P02 to P04, P43, P45, and P142 to P144 is V_{DD}, even in the N-ch open-drain mode.	pp.738, 739 ☐
				For P122/EXCLK, the value of V_{IH} and V_{IL} differs according to the input port mode or external clock mode. Make sure to satisfy the DC characteristics of EXCLK in external clock input mode.	pp.738, 739 ☐
	Soft		During communication at same potential (UART mode) (dedicated baud rate generator output)	Select the normal input buffer for RxDi and the normal output mode for TxDi by using the PIMg and POMg registers.	p.754 ☐
			During communication at same potential (CSI mode) (master mode, $\overline{SCK}$p... internal clock output)	Select the normal input buffer for SIj and the normal output mode for SOj and $\overline{SCK}$j by using the PIMg and POMg registers.	p.755 ☐
			During communication at same potential (CSI mode) (slave mode, $\overline{SCK}$p... external clock input)	Select the normal input buffer for SIj and $\overline{SCK}$j and the normal output mode for SOj by using the PIMg and POMg registers.	p.756 ☐
			During communication at same potential (simplified I^2C mode)	Select the normal input buffer and the N-ch open-drain output (V_{DD} tolerance) mode for SDAr and the normal output mode for SCLr by using the PIMg and POMg registers.	p.759 ☐
			During communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output)	Select the TTL input buffer for RxDq and the N-ch open-drain output (V_{DD} tolerance) mode for TxDq by using the PIMg and POMg registers.	pp.760, 761, 763 ☐