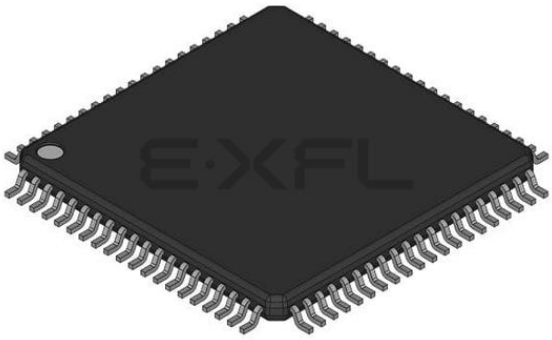


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1156agc-gad-ax

CONTENTS

CHAPTER 1 OUTLINE 17

1.1 Differences Between Conventional-Specification Products (μPD78F115x) and Expanded-Specification Products (μPD78F115xA) 17
1.2 Features 18
1.3 Applications 19
1.4 Ordering Information 19
1.5 Pin Configuration (Top View) 20
1.6 78K0R/Kx3 Microcontroller Lineup 22
1.7 Block Diagram 23
1.8 Outline of Functions 24

CHAPTER 2 PIN FUNCTIONS 26

2.1 Pin Function List 26
2.2 Description of Pin Functions 32
2.2.1 P00 to P06 (port 0) 32
2.2.2 P10 to P17 (port 1) 33
2.2.3 P20 to P27 (port 2) 34
2.2.4 P30, P31 (port 3) 34
2.2.5 P40 to P47 (port 4) 35
2.2.6 P50 to P55 (port 5) 36
2.2.7 P60 to P67 (port 6) 37
2.2.8 P70 to P77 (port 7) 37
2.2.9 P90 (port 9) 38
2.2.10 P110, P111 (port 11) 38
2.2.11 P120 to P124 (port 12) 38
2.2.12 P130 (port 13) 39
2.2.13 P140 to P145 (port 14) 39
2.2.14 AV_{REF0} 40
2.2.15 AV_{REF1} 41
2.2.16 AV_{SS} 41
2.2.17 $\overline{RESET}$ 41
2.2.18 REGC 41
2.2.19 V_{DD}, EV_{DD} 42
2.2.20 V_{SS}, EV_{SS} 42
2.2.21 FLMD0 42
2.3 Pin I/O Circuits and Recommended Connection of Unused Pins 43

CHAPTER 3 CPU ARCHITECTURE 48

3.1 Memory Space 48
3.1.1 Internal program memory space 55
3.1.2 Mirror area 57
3.1.3 Internal data memory space 58
3.1.4 Special function register (SFR) area 59

2.2 Description of Pin Functions

2.2.1 P00 to P06 (port 0)

P00 to P06 function as a 7-bit I/O port. These pins also function as timer I/O, serial interface data I/O, and clock I/O.

Input to the P03 and P04 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units, using port input mode register 0 (PIM0).

Output from the P02 to P04 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units, using port output mode register 0 (POM0).

The following operation modes can be specified in 1-bit units.

(1) Port mode

P00 to P06 function as a 7-bit I/O port. P00 to P06 can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

(2) Control mode

P00 to P06 function as timer I/O, serial interface data I/O, and clock I/O.

(a) TI00, TI05, TI06

These are the pin for inputting an external count clock/capture trigger to 16-bit timer 00, 05, and 06.

(b) TO00, TO05, TO06

These are the timer output pin of 16-bit timer 00, 05, and 06.

(c) SI10

This is a serial data input pin of serial interface CSI10.

(d) SO10

This is a serial data output pin of serial interface CSI10.

(e) $\overline{\text{SCK10}}$

This is a serial clock I/O pin of serial interface CSI10.

(f) TxD1

This is a serial data output pin of serial interface UART1.

(g) RxD1

This is a serial data input pin of serial interface UART1.

(h) SDA10

This is a serial data I/O pin of serial interface for simplified I^2C.

(i) SCL10

This is a serial clock I/O pin of serial interface for simplified I^2C.

CHAPTER 4 PORT FUNCTIONS

4.1 Port Functions

There are four types of pin I/O buffer power supplies: AV_{REF0}, AV_{REF1}, EV_{DD}, and V_{DD}. The relationship between these power supplies and the pins is shown below.

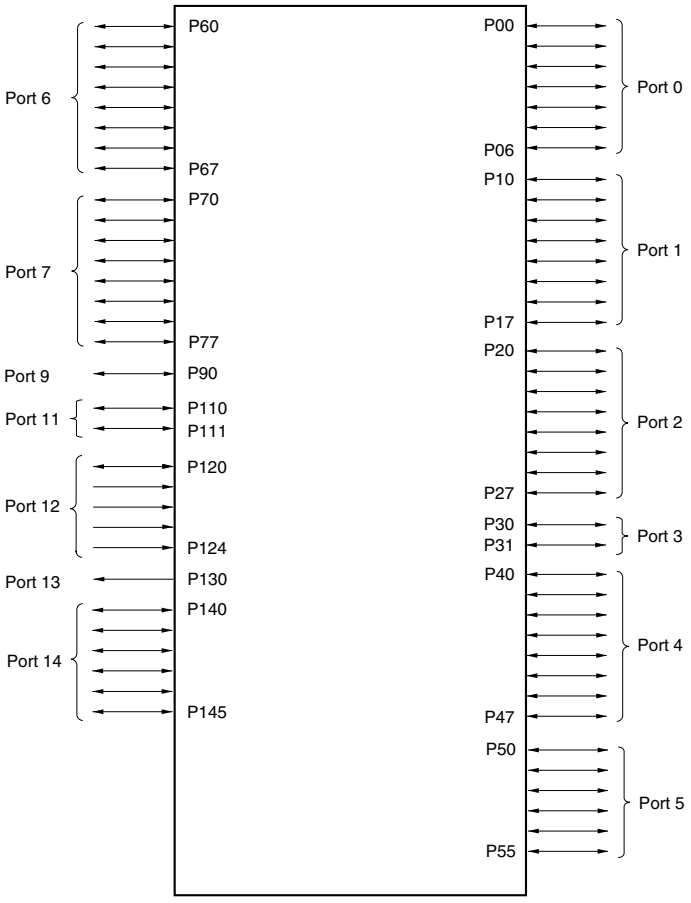
Table 4-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF0}	P20 to P27
AV_{REF1}	P110, P111
EV_{DD}	• Port pins other than P20 to P27, P110, P111, and P121 to P124 • $\overline{\text{RESET}}$ pin and FLMD0 pin
V_{DD}	• P121 to P124 • Pins other than port pins (except $\overline{\text{RESET}}$ pin and FLMD0 pin)

78K0R/KF3 products are provided with the ports shown in Figure 4-1, which enable variety of control operations. The functions of each port are shown in Table 4-2.

In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see **CHAPTER 2 PIN FUNCTIONS**.

Figure 4-1. Port Types



CHAPTER 5 CLOCK GENERATOR

5.1 Functions of Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.
The following three kinds of system clocks and clock oscillators are selectable.

(1) Main system clock

<1> X1 oscillator

This circuit oscillates a clock of f_X = 2 to 20 MHz by connecting a resonator to X1 and X2.
Oscillation can be stopped by executing the STOP instruction or setting of MSTOP (bit 7 of the clock operation status control register (CSC)).

<2> Internal high-speed oscillator

This circuit oscillates a clock of f_{IH} = 8 MHz (TYP.). After a reset release, the CPU always starts operating with this internal high-speed oscillation clock. Oscillation can be stopped by executing the STOP instruction or setting of HIOSTOP (bit 0 of CSC).

An external main system clock (f_{EX} = 2 to 20 MHz) can also be supplied from the EXCLK/X2/P122 pin. An external main system clock input can be disabled by executing the STOP instruction or setting of MSTOP.
As the main system clock, a high-speed system clock (X1 clock or external main system clock) or internal high-speed oscillation clock can be selected by setting of MCM0 (bit 4 of the system clock control register (CKC)).

(2) Subsystem clock

- **XT1 clock oscillator**

This circuit oscillates a clock of f_{SUB} = 32.768 kHz by connecting a 32.768 kHz resonator to XT1 and XT2.
Oscillation can be stopped by setting XTSTOP (bit 6 of CSC).

(3) Internal low-speed oscillation clock (clock for watchdog timer)

- **Internal low-speed oscillator**

This circuit oscillates a clock of f_{IL} = 240 kHz (TYP.).
The internal low-speed oscillation clock cannot be used as the CPU clock. The only hardware that operates with the internal low-speed oscillation clock is the watchdog timer.
Oscillation is stopped when the watchdog timer stops.

Remarks 1. f_X: X1 clock oscillation frequency
f_{IH}: Internal high-speed oscillation clock frequency
f_{EX}: External main system clock frequency
f_{SUB}: Subsystem clock frequency
f_{IL}: Internal low-speed oscillation clock frequency

2. The watchdog timer stops in the following cases.
- When bit 4 (WDTON) of an option byte (000C0H) = 0
- If the HALT or STOP instruction is executed when bit 4 (WDTON) of an option byte (000C0H) = 1 and bit 0 (WDSTBYON) = 0

(2) Timer data register 0n (TDR0n)

This is a 16-bit register from which a capture function and a compare function can be selected.

The capture or compare function can be switched by selecting an operation mode by using the MD0n3 to MD0n0 bits of TMR0n.

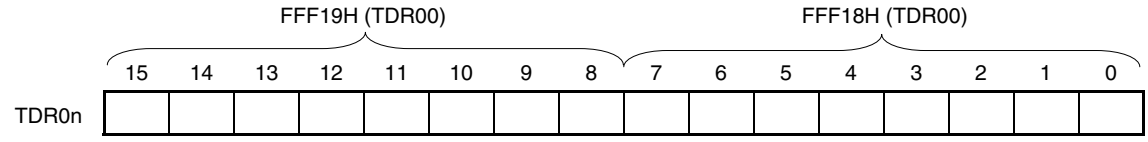
The value of TDR0n can be changed at any time.

This register can be read or written in 16-bit units.

Reset signal generation clears this register to 0000H.

Figure 6-3. Format of Timer Data Register 0n (TDR0n)

Address: FFF18H, FFF19H (TDR00), FFF1AH, FFF1BH (TDR01), FFF64H, FFF65H (TDR02) to FFF6EH, FFF6FH (TDR07) After reset: 0000H R/W



(n = 0 to 7)

(i) When TDR0n is used as compare register

Counting down is started from the value set to TDR0n. When the count value reaches 0000H, an interrupt signal (INTTM0n) is generated. TDR0n holds its value until it is rewritten.

Caution TDR0n does not perform a capture operation even if a capture trigger is input, when it is set to the compare function.

(ii) When TDR0n is used as capture register

The count value of TCR0n is captured to TDR0n when the capture trigger is input.

A valid edge of the TI0n pin can be selected as the capture trigger. This selection is made by TMR0n.

Remark n = 0 to 7

Figure 6-58. Example of Set Contents of Registers When PWM Function (Slave Channel) Is Used

(a) Timer mode register 0m (TMR0m)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR0m	CKS0m			CCS0m	MASTER0m	STS0m2	STS0m1	STS0m0	CIS0m1	CIS0m0			MD0m3	MD0m2	MD0m1	MD0m0
	1/0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1

Operation mode of channel m
100B: One-count mode

Start trigger during operation
1: Trigger input is valid.

Selection of TI0m pin input edge
00B: Sets 00B because these are not used.

Start trigger selection
100B: Selects INTTM0n of master channel.

Slave/master selection
0: Slave channel

Count clock selection
0: Selects operation clock.

Operation clock selection
0: Selects CK00 as operation clock of channel m.
1: Selects CK01 as operation clock of channel m.
* Make the same setting as master channel.

(b) Timer output register 0 (TO0)

	Bit m
TO0	TO0m
	1/0

0: Outputs 0 from TO0m.
1: Outputs 1 from TO0m.

(c) Timer output enable register 0 (TOE0)

	Bit m
TOE0	TOE0m
	1/0

0: Stops the TO0m output operation by counting operation.
1: Enables the TO0m output operation by counting operation.

(d) Timer output level register 0 (TOL0)

	Bit m
TOL0	TOL0m
	1/0

0: Positive logic output (active-high)
1: Inverted output (active-low)

(e) Timer output mode register 0 (TOM0)

	Bit m
TOM0	TOM0m
	1

1: Sets the combination-operation mode.

Remark n = 0, 2, 4, 6
m = n + 1

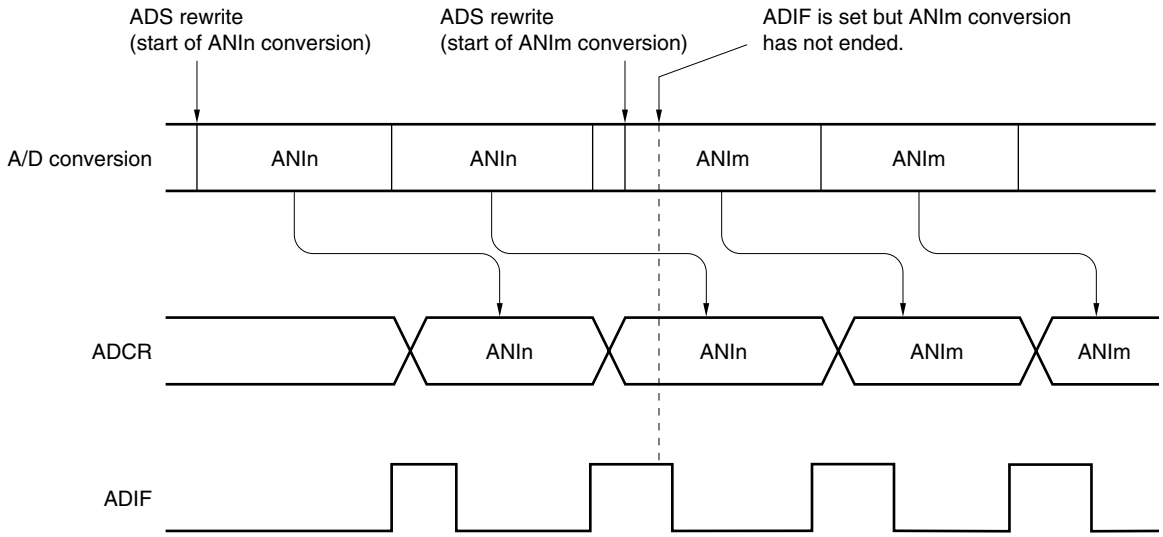
(9) Interrupt request flag (ADIF)

The interrupt request flag (ADIF) is not cleared even if the analog input channel specification register (ADS) is changed.

Therefore, if an analog input pin is changed during A/D conversion, the A/D conversion result and ADIF for the pre-change analog input may be set just before the ADS rewrite. Caution is therefore required since, at this time, when ADIF is read immediately after the ADS rewrite, ADIF is set despite the fact A/D conversion for the post-change analog input has not ended.

When A/D conversion is stopped and then resumed, clear ADIF before the A/D conversion operation is resumed.

Figure 10-27. Timing of A/D Conversion End Interrupt Request Generation



Remarks 1. n = 0 to 7

2. m = 0 to 7

(10) Conversion results just after A/D conversion start

The first A/D conversion value immediately after A/D conversion starts may not fall within the rating range if the ADCS bit is set to 1 within 1 μs after the ADCE bit was set to 1. Take measures such as polling the A/D conversion end interrupt request (INTAD) and removing the first conversion result.

(11) A/D conversion result register (ADCR, ADCRH) read operation

When a write operation is performed to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCR and ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using a timing other than the above may cause an incorrect conversion result to be read.

12.5.5 Slave reception

Slave reception is that the 78K0R/KF3 receives data from another device in the state of a transfer clock being input from another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI20
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	$\overline{SCK00}$, SI00	$\overline{SCK01}$, SI01	$\overline{SCK10}$, SI10	$\overline{SCK20}$, SI20
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI20
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)			
Error detection flag	Overrun error detection flag (OVFmn) only			
Transfer data length	7 or 8 bits			
Transfer rate	Max. f_{MCK}/6 [Hz]Notes 1, 2			
Data phase	Selectable by DAPmn bit • DAPmn = 0: Data input starts from the start of the operation of the serial clock. • DAPmn = 1: Data input starts half a clock before the start of the serial clock operation.			
Clock phase	Selectable by CKPmn bit • CKPmn = 0: Forward • CKPmn = 1: Reverse			
Data direction	MSB or LSB first			

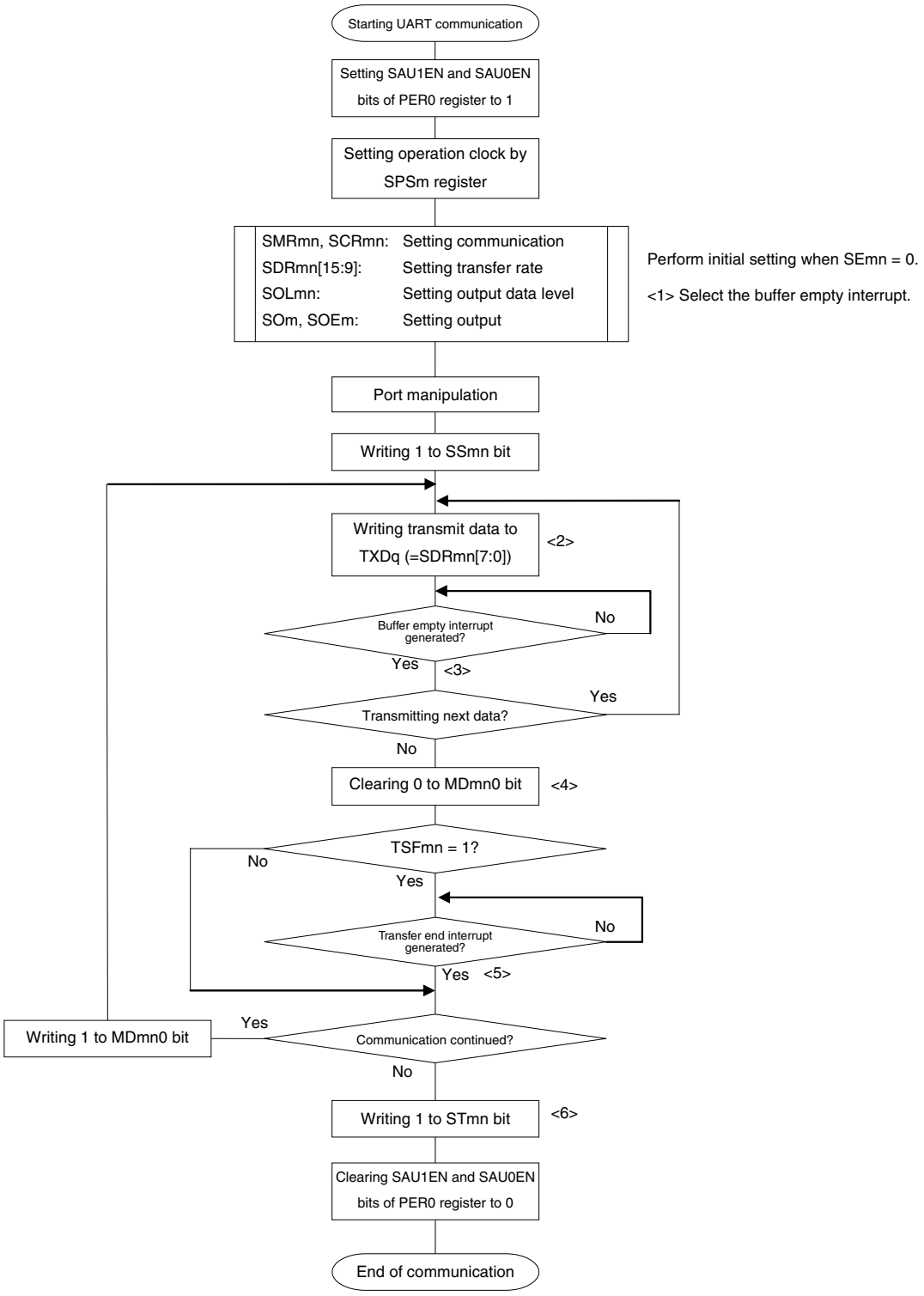
Notes 1. Because the external serial clock input to pins $\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, and $\overline{SCK20}$ is sampled internally and used, the fastest transfer rate is f_{MCK}/6 [Hz].

2. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 28 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) and CHAPTER 29 ELECTRICAL SPECIFICATIONS ((A) GRADE PRODUCTS)**).

Remarks 1. f_{MCK}: Operation clock (MCK) frequency of target channel

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2)

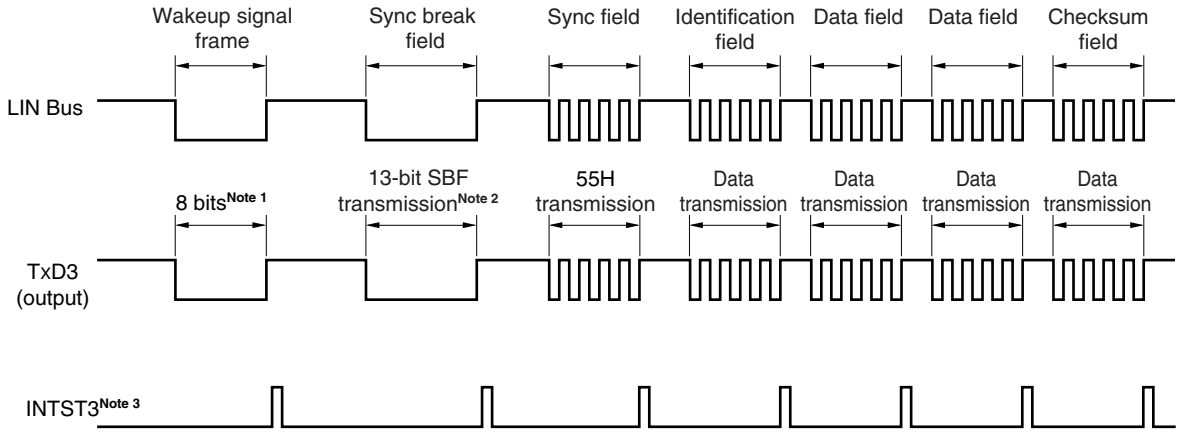
Figure 12-78. Flowchart of UART Transmission (in Continuous Transmission Mode)



Caution After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

Remark <1> to <6> in the figure correspond to <1> to <6> in **Figure 12-77 Timing Chart of UART Transmission (in Continuous Transmission Mode)**.

Figure 12-85. Transmission Operation of LIN



Notes 1. The baud rate is set so as to satisfy the standard of the wakeup signal and data of 00H is transmitted.

2. A sync break field is defined to have a width of 13 bits and output a low level. Where the baud rate for main transfer is N [bps], therefore, the baud rate of the sync break field is calculated as follows.

(Baud rate of sync break field) = 9/13 × N

By transmitting data of 00H at this baud rate, a sync break field is generated.

3. INTST3 is output upon completion of transmission. INTST3 is also output when SBF transmission is executed.

Remark The interval between fields is controlled by software.

Table 13-6. Status During Arbitration and Interrupt Request Generation Timing

Status During Arbitration	Interrupt Request Generation Timing
During address transmission	At falling edge of eighth or ninth clock following byte transfer[Note 1]
Read/write data after address transmission	
During extension code transmission	
Read/write data after extension code transmission	
During data transmission	
During $\overline{\text{ACK}}$ transfer period after data transmission	
When restart condition is detected during data transfer	
When stop condition is detected during data transfer	When stop condition is generated (when SPIE0 = 1)[Note 2]
When data is at low level while attempting to generate a restart condition	At falling edge of eighth or ninth clock following byte transfer[Note 1]
When stop condition is detected while attempting to generate a restart condition	When stop condition is generated (when SPIE0 = 1)[Note 2]
When data is at low level while attempting to generate a stop condition	At falling edge of eighth or ninth clock following byte transfer[Note 1]
When SCL0 is at low level while attempting to generate a restart condition	

Notes 1. When WTIM0 (bit 3 of IIC control register 0 (IICC0)) = 1, an interrupt request occurs at the falling edge of the ninth clock. When WTIM0 = 0 and the extension code's slave address is received, an interrupt request occurs at the falling edge of the eighth clock.

2. When there is a chance that arbitration will occur, set SPIE0 = 1 for master device operation.

Remark SPIE0: Bit 4 of IIC control register 0 (IICC0)

13.5.14 Wakeup function

The I^2C bus slave function is a function that generates an interrupt request signal (INTIIC0) when a local address and extension code have been received.

This function makes processing more efficient by preventing unnecessary INTIIC0 signal from occurring when addresses do not match.

When a start condition is detected, wakeup standby mode is set. This wakeup standby mode is in effect while addresses are transmitted due to the possibility that an arbitration loss may change the master device (which has generated a start condition) to a slave device.

However, when a stop condition is detected, bit 4 (SPIE0) of IIC control register 0 (IICC0) is set regardless of the wakeup function, and this determines whether interrupt requests are enabled or disabled.

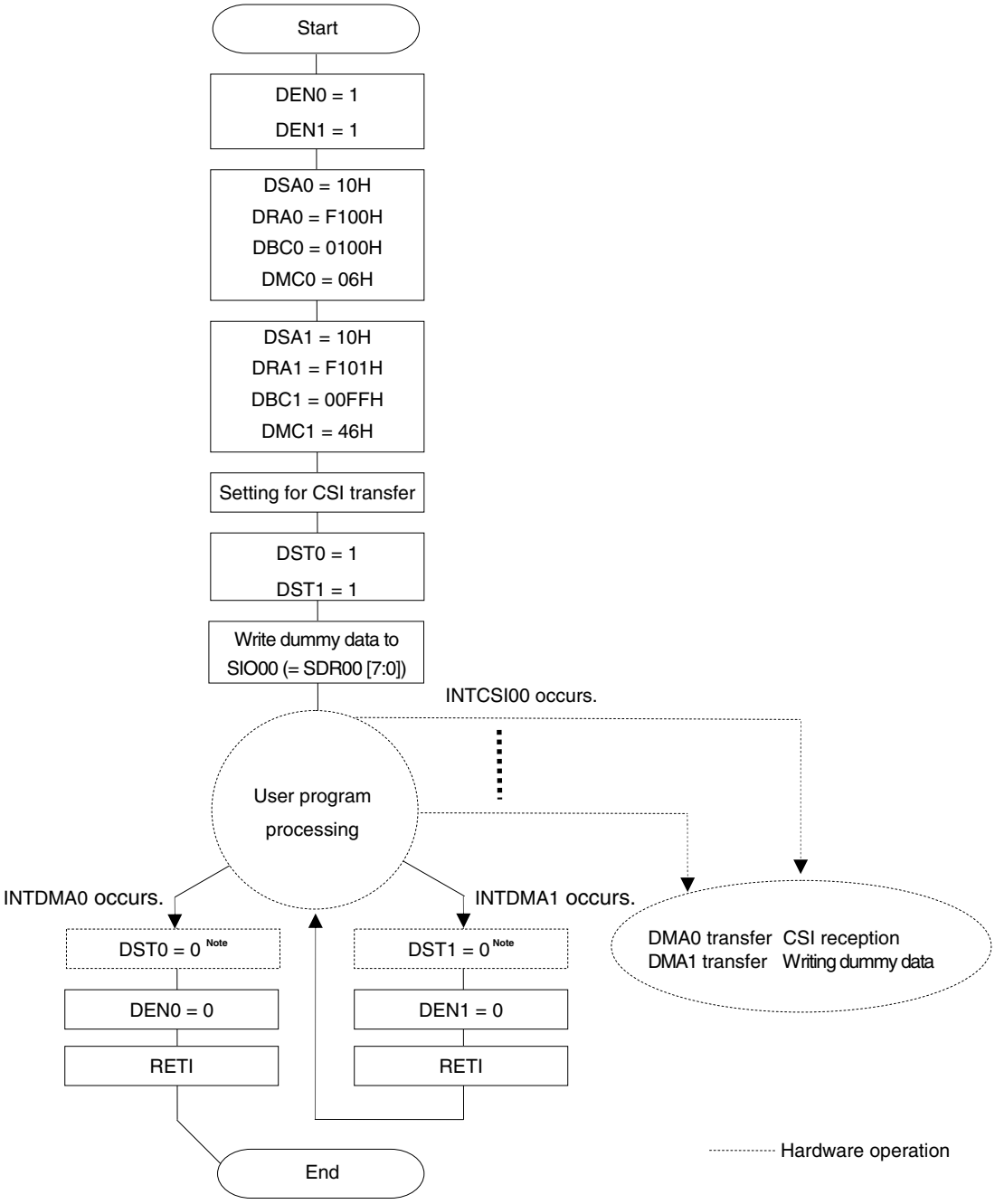
(2) When communication reservation function is disabled (bit 0 (IICRSV) of IIC flag register 0 (IICF0) = 1)

When bit 1 (STT0) of IIC control register 0 (IICC0) is set to 1 when the bus is not used in a communication during bus communication, this request is rejected and a start condition is not generated. The following two statuses are included in the status where bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{ACK}$ is not returned and the bus was released by setting bit 6 (LREL0) of IICC0 to 1 and saving communication)

To confirm whether the start condition was generated or request was rejected, check STCF (bit 7 of IICF0). It takes up to 5 clocks until STCF is set to 1 after setting STT0 = 1. Therefore, secure the time by software.

Figure 15-8. Setting Example of CSI Master Reception



Note The DSTn flag is automatically cleared to 0 when a DMA transfer is completed.
Writing the DENn flag is enabled only when DSTn = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMAn (INTDMAn), set DSTn to 0 and then DENn to 0 (for details, refer to **15.5.7 Forcible termination by software**).

Because no CSI interrupt is generated when reception starts during CSI master reception, dummy data is written using software in this example.

The received data is automatically transferred from the first byte. (In successive reception mode, the data that is to be received when the first buffer empty interrupt occurs is invalid because the valid data has not been received.)

A DMA interrupt (INTDMA1) occurs when the last dummy data has been writing to the data register. A DMA interrupt (INTDMA0) occurs when the last received data has been read from the data register. To restart the DMA transfer, the CSI transfer must be completed.

(1) Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter.

The X1 clock oscillation stabilization time can be checked in the following case,

- If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating.

OSTC can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset is released (reset by $\overline{\text{RESET}}$ input, POC, LVI, WDT, and executing an illegal instruction), the STOP instruction and MSTOP (bit 7 of CSC register) = 1 clear this register to 00H.

Figure 18-1. Format of Oscillation Stabilization Time Counter Status Register (OSTC)

Address: FFFA2H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18

MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18	Oscillation stabilization time status		
									f_X = 10 MHz	f_X = 20 MHz
0	0	0	0	0	0	0	0	$2^8/f_X$ max.	25.6 μs max.	12.8 μs max.
1	0	0	0	0	0	0	0	$2^8/f_X$ min.	25.6 μs min.	12.8 μs min.
1	1	0	0	0	0	0	0	$2^9/f_X$ min.	51.2 μs min.	25.6 μs min.
1	1	1	0	0	0	0	0	$2^{10}/f_X$ min.	102.4 μs min.	51.2 μs min.
1	1	1	1	0	0	0	0	$2^{11}/f_X$ min.	204.8 μs min.	102.4 μs min.
1	1	1	1	1	0	0	0	$2^{13}/f_X$ min.	819.2 μs min.	409.6 μs min.
1	1	1	1	1	1	0	0	$2^{15}/f_X$ min.	3.27 ms min.	1.64 ms min.
1	1	1	1	1	1	1	0	$2^{17}/f_X$ min.	13.11 ms min.	6.55 ms min.
1	1	1	1	1	1	1	1	$2^{18}/f_X$ min.	26.21 ms min.	13.11 ms min.

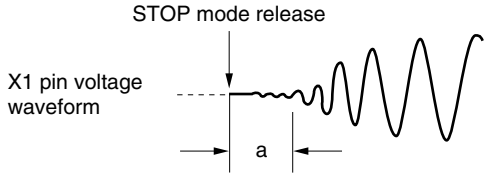
Cautions 1. After the above time has elapsed, the bits are set to 1 in order from MOST8 and remain 1.

2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

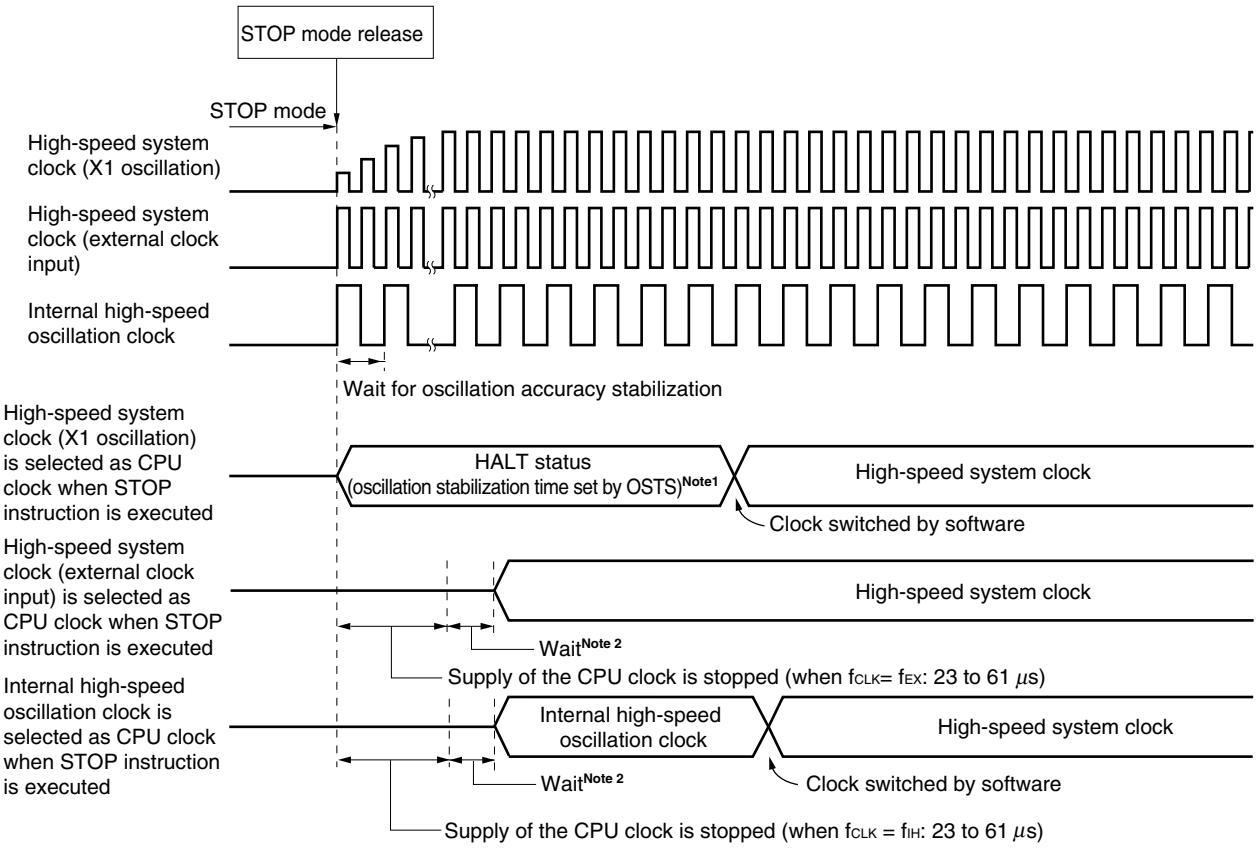
3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark f_X: X1 clock oscillation frequency

(2) STOP mode release

Figure 18-5. Operation Timing When STOP Mode Is Released (Release by Unmasked Interrupt Request)



Notes 1. When the oscillation stabilization time set by OSTS is equal to or shorter than 61 μs, the HALT status is retained to a maximum of "61μs + wait time."

2. The wait time is as follows:

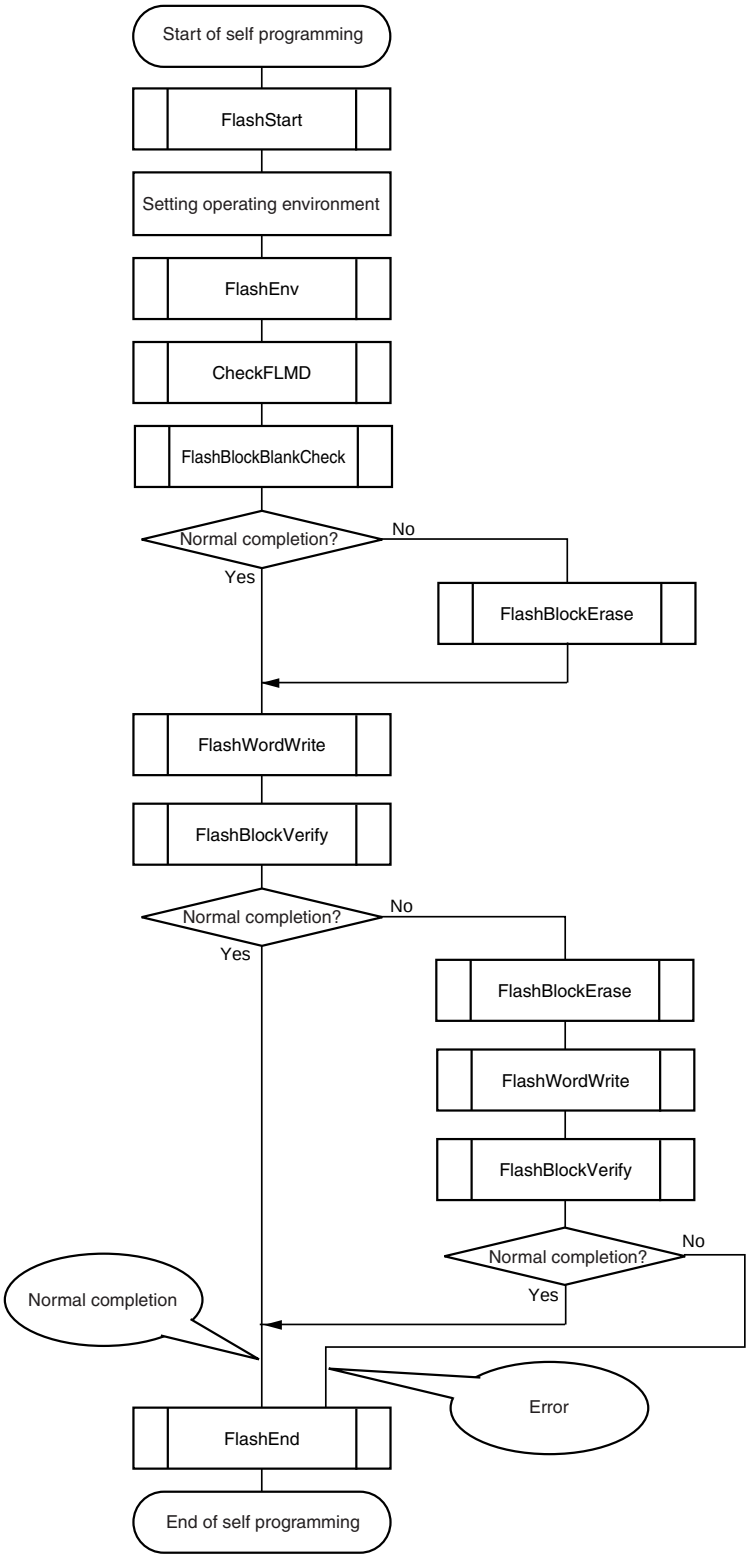
- When vectored interrupt servicing is carried out: 10 to 12 clocks
- When vectored interrupt servicing is not carried out: 5 or 6 clocks

Remark f_{EX}: External main system clock frequency
f_{IH}: Internal high-speed oscillation clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency

The STOP mode can be released by the following two sources.

The following figure illustrates a flow of rewriting the flash memory by using a self programming library.

Figure 24-10. Flow of Self Programming (Rewriting Flash Memory)



Remark For details of the self programming library, refer to **78K0R Microcontroller Self Programming Library Type01 User's Manual (U18706E)**.

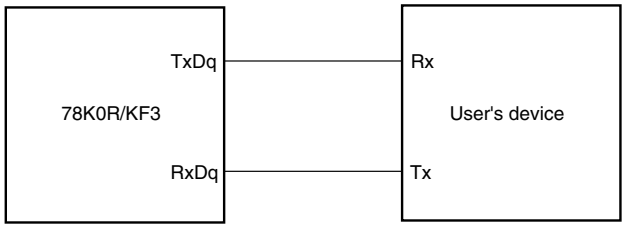
(2) Serial interface: Serial array unit (1/18)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

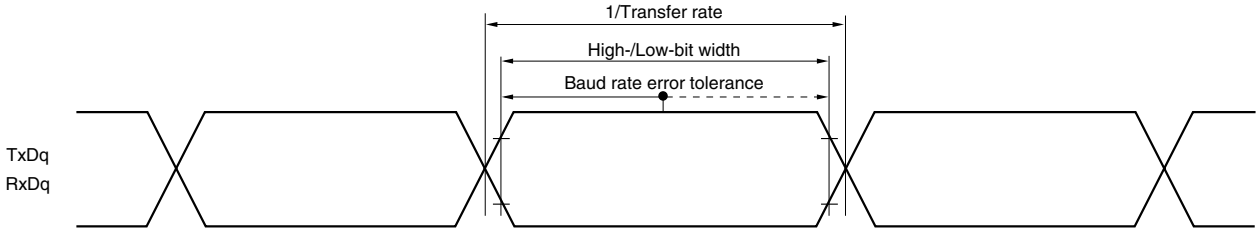
(a) During communication at same potential (UART mode) (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					f_{MCK}/6	bps
		f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}			3.3	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for RxDi and the normal output mode for TxDi by using the PIMg and POMg registers.

Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 14),
i: UART number for which communication at different potential can be selected (i = 1, 2)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of the SMRmn register. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

(2) Serial interface: Serial array unit (12/18)

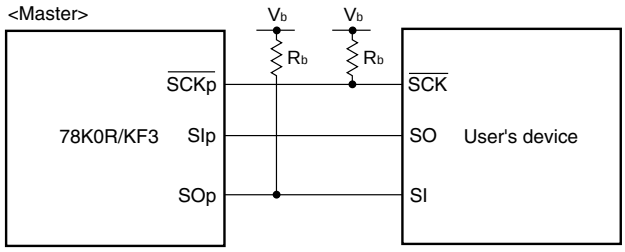
(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

<R> **(f) During Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (2/2)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SIp setup time (to $\overline{SCKp}$↓) Note	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	70			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	100			ns
SIp hold time (from $\overline{SCKp}$↓) Note	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	30			ns
Delay time from $\overline{SCKp}$↑ to SOp output Note	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			40	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			40	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

CSI mode connection diagram (during communication at different potential)



Caution Select the TTL input buffer for SIp and the N-ch open drain output (V_{DD} tolerance) mode for SOp and $\overline{SCKp}$ by using the PIMg and POMg registers.

Remarks 1. p: CSI number (p = 01, 10, 20), g: PIM and POM number (g = 0, 4, 14)

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2)

3. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance,
C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

5. CSI00 cannot communicate at different potential. Use CSI01, CSI10, and CSI20 for communication at different potential.

DC Characteristics (10/12)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF0} ≤ V_{DD}, 1.8 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current	I_{DD2} Note 1	HALT mode	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V		Square wave input		1.0	2.7	mA
					Resonator connection		1.3	3.0	mA
			f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V		Square wave input		1.0	2.7	mA
					Resonator connection		1.3	3.0	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 5.0 V		Square wave input		0.52	1.4	mA
					Resonator connection		0.62	1.5	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 3.0 V		Square wave input		0.52	1.4	mA
					Resonator connection		0.62	1.5	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 3.0 V	Normal current mode	Square wave input		0.36	0.75	mA
					Resonator connection		0.41	0.8	mA
				Low consumption current mode Note 4	Square wave input		0.22	0.5	mA
					Resonator connection		0.27	0.55	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 2.0 V	Normal current mode	Square wave input		0.22	0.5	mA
					Resonator connection		0.27	0.55	mA
				Low consumption current mode Note 4	Square wave input		0.22	0.5	mA
					Resonator connection		0.27	0.55	mA
			f_{IH} = 8 MHz Note 5		V_{DD} = 5.0 V		0.45	1.2	mA
					V_{DD} = 3.0 V		0.45	1.2	mA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, AV_{REF0}, and AV_{REF1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. During HALT instruction execution by flash memory.

2. When internal high-speed oscillator and subsystem clock are stopped.

3. When AMPH (bit 0 of clock operation mode control register (CMC)) = 0 and FSEL (bit 0 of operation speed mode control register (OSMC)) = 0.

4. When the RMC register is set to 5AH.

5. When high-speed system clock and subsystem clock are stopped. When FSEL (bit 0 of operation speed mode control register (OSMC)) = 0 is set.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

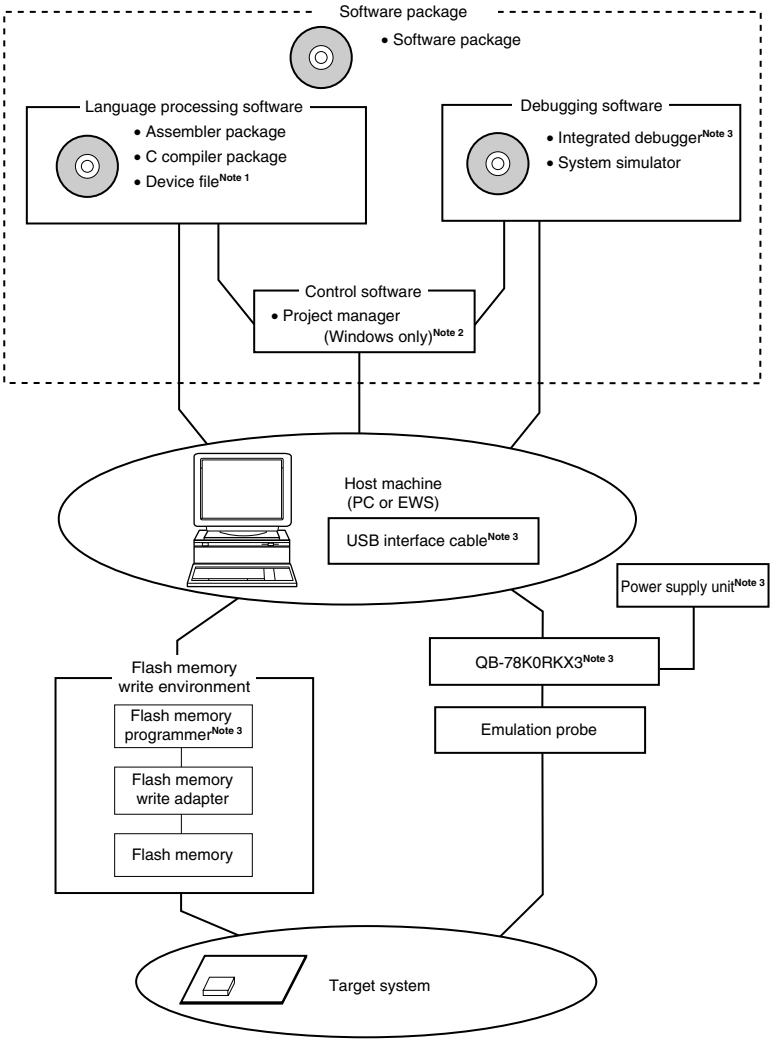
f_{IH}: Internal high-speed oscillation clock frequency

2. For details on the normal current mode and low consumption current mode according to the regulator output voltage, refer to **CHAPTER 22 REGULATOR**.

<R> **3.** Temperature condition of the TYP. value is T_A = 25°C

Figure A-1. Development Tool Configuration (1/2)

(1) When using the in-circuit emulator QB-78K0RKX3



Notes 1. Download the device file for 78K0R/KF3 (DF781188) from the download site for development tools (http://www.necel.com/micro/ods/eng/index.html).

2. The project manager PM+ is included in the assembler package.
The PM+ is only used for Windows.

3. In-circuit emulator QB-78K0RKX3 is supplied with integrated debugger ID78K0R-QB, on-chip debug emulator with programming function QB-MINI2, power supply unit, and USB interface cable. Any other products are sold separately.