Infineon Technologies - SAF-XC164S-16F40F BB Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	79
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	PG-TQFP-100-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc164s-16f40f-bb

Table 2 Pin Definitions and Functions

Symbol	Pin Num.	Input Outp.	Function
$\overline{\text{RSTIN}}$	1	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the XC164S. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. *Note: The reset duration must be sufficient to let the hardware configuration signals settle. External circuitry must guarantee low level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.*
P20.12	2	IO	For details, please refer to the description of **P20**.
$\overline{\text{NMI}}$	3	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the XC164S into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.
P0H.0-P0H.3	4…7	IO	For details, please refer to the description of **PORT0**.
P9		IO	Port 9 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 9 is selectable (standard or special). The following Port 9 pins also serve for alternate functions:
P9.0	10	I/O I	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp., EX7IN Fast External Interrupt 7 Input (alternate pin B)
P9.1	11	I/O I	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp., EX6IN Fast External Interrupt 6 Input (alternate pin B)
P9.2	12	I/O I	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp., EX7IN Fast External Interrupt 7 Input (alternate pin A)
P9.3	13	I/O I	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp., EX6IN Fast External Interrupt 6 Input (alternate pin A)
P9.4	14	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.
P9.5	15	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
P3		IO	Port 3 is a 14-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:	
P3.1	39	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin A),
		I	TCK	Debug System: JTAG Clock Input
P3.2	40	I	CAPIN	GPT2 Register CAPREL Capture Input,
		I	TDI	Debug System: JTAG Data In
P3.3	41	O	T3OUT	GPT1 Timer T3 Toggle Latch Output,
		O	TDO	Debug System: JTAG Data Out
P3.4	42	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input,
		I	TMS	Debug System: JTAG Test Mode Selection
P3.5	43	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp
		O	TxD1	ASC0 Clock/Data Output (Async./Sync.),
		O	BRKOUT	Debug System: Break Out
P3.6	44	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	45	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp
		I	BRKIN	Debug System: Break In
P3.8	46	I/O	MRST0	SSC0 Master-Receive/Slave-Transmit In/Out.
P3.9	47	I/O	MTSR0	SSC0 Master-Transmit/Slave-Receive Out/In.
P3.10	48	O	TxD0	ASC0 Clock/Data Output (Async./Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin B)
P3.11	49	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin A)
P3.12	50	O	BHE	External Memory High Byte Enable Signal,
		O	WRH	External Memory High Byte Write Strobe,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin B)
P3.13	51	I/O	SCLK0	SSC0 Master Clock Output / Slave Clock Input.,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin A)
P3.15	52	O	CLKOUT	System Clock Output (= CPU Clock),
		O	FOUT	Programmable Frequency Output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
P20		IO	Port 20 is a 5-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output. The input threshold of Port 20 is selectable (standard or special). The following Port 20 pins also serve for alternate functions:	
P20.0	63	O	$\overline{RD}$	External Memory Read Strobe, activated for every external instruction or data read access.
P20.1	64	O	$\overline{WR}$/$\overline{WRL}$	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus.
P20.4	65	O	ALE	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P20.5	66	I	$\overline{EA}$	External Access Enable pin. **A low level** at this pin during and after Reset forces the XC164S to latch the configuration from PORT0 and pin $\overline{RD}$, and to begin instruction execution out of external memory. **A high level** forces the XC164S to latch the configuration from pins $\overline{RD}$, ALE, and $\overline{WR}$, and to begin instruction execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
P20.12	2	O	$\overline{RSTOUT}$	Internal Reset Indication Output. **Is activated** asynchronously with an external hardware reset. It may also be activated (selectable) synchronously with an internal software or watchdog reset. **Is deactivated** upon the execution of the EINIT instruction, optionally at the end of reset, or at any time (before EINIT) via user software.
			Note: Port 20 pins may input configuration values (see $\overline{EA}$).	

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
PORT0 P0L.0 - P0L.7 P0H.0 - P0L.3 P0H.4 - P0L.7	 67 - 74 4 - 7 75 - 78	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. Each pin can be programmed for input (output driver in high-impedance state) or output. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** 8-bit data bus: P0H = I/O, P0L = D7 - D0 16-bit data bus: P0H = D15 - D8, P0L = D7 - D0 **Multiplexed bus modes:** 8-bit data bus: P0H = A15 - A8, P0L = AD7 - AD0 16-bit data bus: P0H = AD15 - AD8, P0L = AD7 - AD0 *Note: At the end of an external reset ($\overline{EA}$ = 0) PORT0 also may input configuration values*
PORT1 P1L.0 P1L.1 P1L.2 P1L.3 P1L.4 P1L.5 P1L.6 P1L.7 P1H	 79 80 81 82 83 84 85 86 …	IO I/O O I/O O I/O O O I I/O	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes (also after switching from a demultiplexed to a multiplexed bus mode). The following PORT1 pins also serve for alt. functions: CC60 CAPCOM6: Input / Output of Channel 0 COUT60 CAPCOM6: Output of Channel 0 CC61 CAPCOM6: Input / Output of Channel 1 COUT61 CAPCOM6: Output of Channel 1 CC62 CAPCOM6: Input / Output of Channel 2 COUT62 CAPCOM6: Output of Channel 2 COUT63 Output of 10-bit Compare Channel $\overline{CTRAP}$ CAPCOM6: Trap Input $\overline{CTRAP}$ is an input pin with an internal pull-up resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled). CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp. …continued…

3 Functional Description

The architecture of the XC164S combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources as well as external resources (see **Figure 3**).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC164S.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC164S.

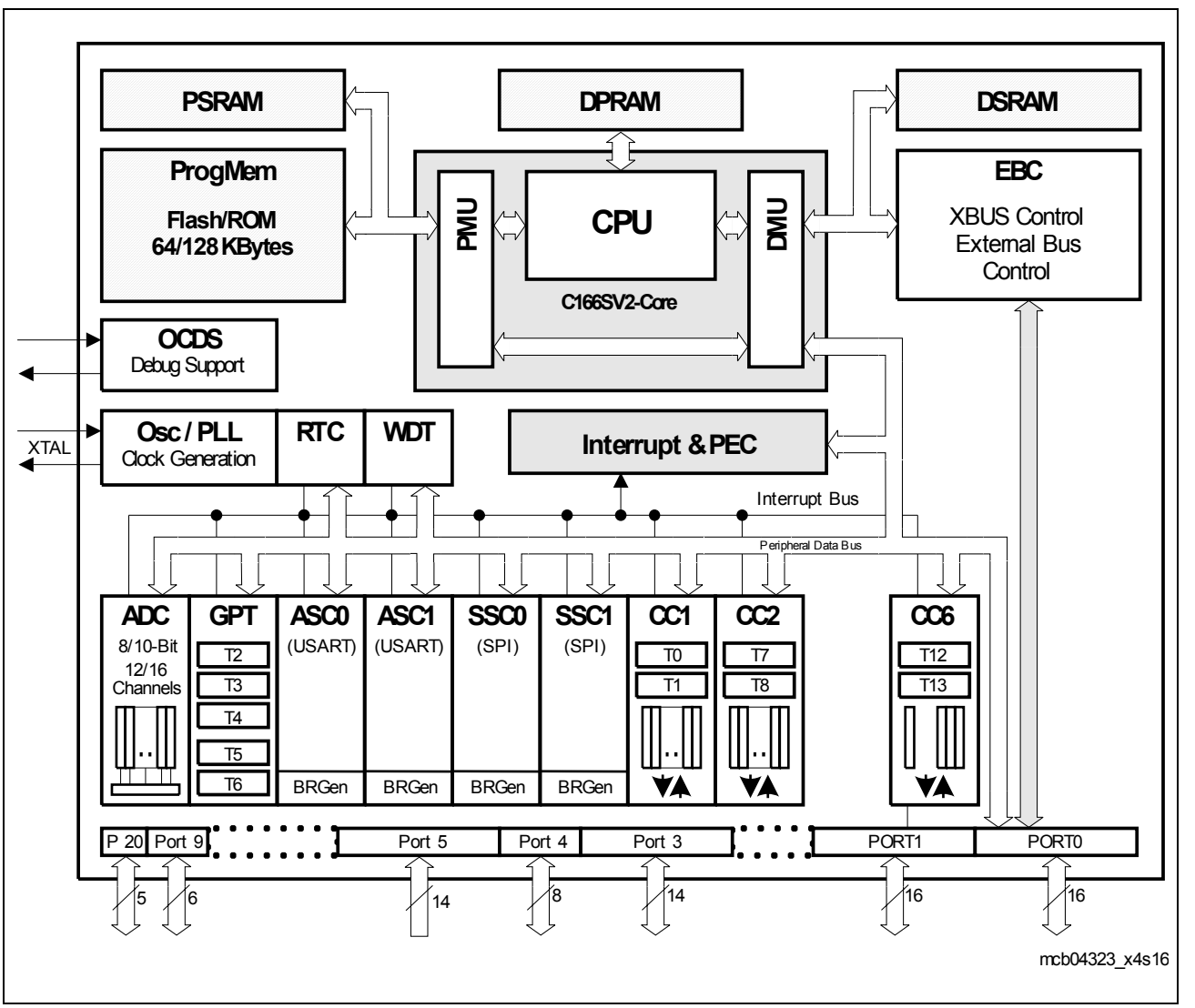


Figure 3 Block Diagram

3.1 Memory Subsystem and Organization

The memory space of the XC164S is configured in a Von Neumann architecture, which means that all internal and external resources, such as code memory, data memory, registers and I/O ports, are organized within the same linear address space. This common memory space includes 16 Mbytes and is arranged as 256 segments of 64 Kbytes each, where each segment consists of four data pages of 16 Kbytes each. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (E/SFR) have additionally been made directly bitaddressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls accesses to the program memories, such as Flash memory, and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls accesses to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected via the high-speed system bus to exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources, including peripherals on the LXBus (such as TwinCAN). The system bus allows concurrent two-way communication for maximum transfer performance.

64/128 Kbytes[1] **of on-chip Flash memory or mask-programmable ROM** store code or constant data. The on-chip Flash memory is organized as four 8-Kbyte sectors, one 32-Kbyte sector, and one 64-Kbyte sector. Each sector can be separately write protected[2], erased and programmed (in blocks of 128 Bytes). The complete Flash or ROM area can be read-protected. A password sequence temporarily unlocks protected areas. The Flash module combines very fast 64-bit one-cycle read accesses with protected and efficient writing algorithms for programming and erasing. Thus, program execution out of the internal Flash results in maximum performance. Dynamic error correction provides extremely high read data security for all read accesses.
For timing characteristics, please refer to **Section 4.4.2**.

2 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is therefore optimized for code fetches.

2/4 Kbytes[1] **of on-chip Data SRAM (DSRAM)** are provided as a storage for general user data. The DSRAM is accessed via the DMU and is therefore optimized for data accesses.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) are provided as a storage for user defined variables, for the system stack, and general purpose register banks. A register

1) Depends on the respective derivative. The derivatives are listed in **Table 1**.

2) Each two 8-Kbyte sectors are combined for write-protection purposes.

example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. Also multiplication and most MAC instructions execute in one single cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: for example, a division algorithm is performed in 18 to 21 CPU cycles, depending on the data and division type. Four cycles are always visible, the rest runs in the background. Another pipeline optimization, the branch target prediction, allows eliminating the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 wordwide GPRs each at its disposal. The global register bank is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active global register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided as a storage for temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area), and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient XC164S instruction set which includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Table 4 XC164S Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM Register 29	CC2_CC29IC	xx'0110$_H$	44$_H$ / 68$_D$
CAPCOM Register 30	CC2_CC30IC	xx'0114$_H$	45$_H$ / 69$_D$
CAPCOM Register 31	CC2_CC31IC	xx'0118$_H$	46$_H$ / 70$_D$
CAPCOM Timer 0	CC1_T0IC	xx'0080$_H$	20$_H$ / 32$_D$
CAPCOM Timer 1	CC1_T1IC	xx'0084$_H$	21$_H$ / 33$_D$
CAPCOM Timer 7	CC2_T7IC	xx'00F4$_H$	3D$_H$ / 61$_D$
CAPCOM Timer 8	CC2_T8IC	xx'00F8$_H$	3E$_H$ / 62$_D$
GPT1 Timer 2	GPT12E_T2IC	xx'0088$_H$	22$_H$ / 34$_D$
GPT1 Timer 3	GPT12E_T3IC	xx'008C$_H$	23$_H$ / 35$_D$
GPT1 Timer 4	GPT12E_T4IC	xx'0090$_H$	24$_H$ / 36$_D$
GPT2 Timer 5	GPT12E_T5IC	xx'0094$_H$	25$_H$ / 37$_D$
GPT2 Timer 6	GPT12E_T6IC	xx'0098$_H$	26$_H$ / 38$_D$
GPT2 CAPREL Register	GPT12E_CRIC	xx'009C$_H$	27$_H$ / 39$_D$
A/D Conversion Complete	ADC_CIC	xx'00A0$_H$	28$_H$ / 40$_D$
A/D Overrun Error	ADC_EIC	xx'00A4$_H$	29$_H$ / 41$_D$
ASC0 Transmit	ASC0_TIC	xx'00A8$_H$	2A$_H$ / 42$_D$
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C$_H$	47$_H$ / 71$_D$
ASC0 Receive	ASC0_RIC	xx'00AC$_H$	2B$_H$ / 43$_D$
ASC0 Error	ASC0_EIC	xx'00B0$_H$	2C$_H$ / 44$_D$
ASC0 Autobaud	ASC0_ABIC	xx'017C$_H$	5F$_H$ / 95$_D$
SSC0 Transmit	SSC0_TIC	xx'00B4$_H$	2D$_H$ / 45$_D$
SSC0 Receive	SSC0_RIC	xx'00B8$_H$	2E$_H$ / 46$_D$
SSC0 Error	SSC0_EIC	xx'00BC$_H$	2F$_H$ / 47$_D$
PLL/OWD	PLLIC	xx'010C$_H$	43$_H$ / 67$_D$
ASC1 Transmit	ASC1_TIC	xx'0120$_H$	48$_H$ / 72$_D$
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178$_H$	5E$_H$ / 94$_D$
ASC1 Receive	ASC1_RIC	xx'0124$_H$	49$_H$ / 73$_D$
ASC1 Error	ASC1_EIC	xx'0128$_H$	4A$_H$ / 74$_D$
ASC1 Autobaud	ASC1_ABIC	xx'0108$_H$	42$_H$ / 66$_D$
End of PEC Subchannel	EOPIC	xx'0130$_H$	4C$_H$ / 76$_D$

Table 4 XC164S Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM6 Timer T12	CCU6_T12IC	xx'0134$_H$	4D$_H$ / 77$_D$
CAPCOM6 Timer T13	CCU6_T13IC	xx'0138$_H$	4E$_H$ / 78$_D$
CAPCOM6 Emergency	CCU6_EIC	xx'013C$_H$	4F$_H$ / 79$_D$
CAPCOM6	CCU6_IC	xx'0140$_H$	50$_H$ / 80$_D$
SSC1 Transmit	SSC1_TIC	xx'0144$_H$	51$_H$ / 81$_D$
SSC1 Receive	SSC1_RIC	xx'0148$_H$	52$_H$ / 82$_D$
SSC1 Error	SSC1_EIC	xx'014C$_H$	53$_H$ / 83$_D$
Unassigned node	–	xx'0150$_H$	54$_H$ / 84$_D$
Unassigned node	–	xx'0154$_H$	55$_H$ / 85$_D$
Unassigned node	–	xx'0158$_H$	56$_H$ / 86$_D$
Unassigned node	–	xx'015C$_H$	57$_H$ / 87$_D$
Unassigned node	–	xx'0164$_H$	59$_H$ / 89$_D$
Unassigned node	–	xx'0168$_H$	5A$_H$ / 90$_D$
Unassigned node	–	xx'016C$_H$	5B$_H$ / 91$_D$
Unassigned node	–	xx'0170$_H$	5C$_H$ / 92$_D$
Unassigned node	–	xx'0174$_H$	5D$_H$ / 93$_D$
Unassigned node	–	xx'0100$_H$	40$_H$ / 64$_D$
Unassigned node	–	xx'0104$_H$	41$_H$ / 65$_D$
Unassigned node	–	xx'012C$_H$	4B$_H$ / 75$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'0160$_H$	58$_H$ / 88$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

The XC164S also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 5 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 5 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location[1)]	Trap Number	Trap Priority
Reset Functions:	–				
• Hardware Reset		RESET	$xx'0000_H$	00_H	III
• Software Reset		RESET	$xx'0000_H$	00_H	III
• Watchdog Timer Overflow		RESET	$xx'0000_H$	00_H	III
Class A Hardware Traps:					
• Non-Maskable Interrupt	NMI	NMITRAP	$xx'0008_H$	02_H	II
• Stack Overflow	STKOF	STOTRAP	$xx'0010_H$	04_H	II
• Stack Underflow	STKUF	STUTRAP	$xx'0018_H$	06_H	II
• Software Break	SOFTBRK	SBRKTRAP	$xx'0020_H$	08_H	II
Class B Hardware Traps:					
• Undefined Opcode	UNDOPC	BTRAP	$xx'0028_H$	$0A_H$	I
• PMI Access Error	PACER	BTRAP	$xx'0028_H$	$0A_H$	I
• Protected Instruction Fault	PRTFLT	BTRAP	$xx'0028_H$	$0A_H$	I
• Illegal Word Operand Access	ILLOPA	BTRAP	$xx'0028_H$	$0A_H$	I
Reserved	–	–	$[2C_H - 3C_H]$	$[0B_H - 0F_H]$	–
Software Traps • TRAP Instruction	–	–	Any $[xx'0000_H - xx'01FC_H]$ in steps of 4_H	Any $[00_H - 7F_H]$	Current CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.

compare function.
12 registers of the CAPCOM2 module have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

Table 6 Compare Modes (CAPCOM1/2)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare timer overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; can be used with any compare mode

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

The RTC module can be used for different purposes:

- System clock to determine the current time and date,
  optionally during idle mode, sleep mode, and power down mode.
- Cyclic time based interrupt, to provide a system time tick independent of CPU frequency and other resources, e.g. to wake up regularly from idle mode.
- 48-bit timer for long term measurements (maximum timespan is >> 100 years).
- Alarm interrupt for wake-up on a defined time.

Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC164S. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage for the core	V_{DDI}	2.35	2.7	V	Active mode, $f_{CPU} = f_{CPUmax}$ [1)2)]
Digital supply voltage for IO pads	V_{DDP}	4.4	5.5	V	Active mode[2)3)]
Supply Voltage Difference	ΔV_{DD}	-0.5	–	V	V_{DDP} - V_{DDI}[4)]
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-5	5	mA	Per IO pin[5)6)]
		-2	5	mA	Per analog input pin[5)6)]
Overload current coupling factor for analog inputs[7)]	K_{OVA}	–	1.0×10^{-4}	–	$I_{OV} > 0$
		–	1.5×10^{-3}	–	$I_{OV} < 0$
Overload current coupling factor for digital I/O pins[7)]	K_{OVD}	–	5.0×10^{-3}	–	$I_{OV} > 0$
		–	1.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	[6)]
External Load Capacitance	C_L	–	50	pF	Pin drivers in **default** mode[8)]
Ambient temperature	T_A	–	–	°C	see **Table 1**

1) f_{CPUmax} = 40 MHz for devices marked … 40F, f_{CPUmax} = 20 MHz for devices marked … 20F.

2) External circuitry must guarantee low-level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.

3) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of V_{DDP} = 4.75 V to 5.25 V.

4) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes.

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time.
For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and $\Sigma\text{-}I_{OH}$) must remain below 50 mA.

Table 13 Power Consumption XC164S (Operating Conditions apply)

Parameter	Sym-bol	Limit Values		Unit	Test Condition
		Min.	Max.		
Power supply current (active) with all peripherals active	I_{DDI}	–	15 + 2.6 × f_{CPU}	mA	f_{CPU} in [MHz] 1)2)
Pad supply current	I_{DDP}	–	5	mA	3)
Idle mode supply current with all peripherals active	I_{IDX}	–	15 + 1.2 × f_{CPU}	mA	f_{CPU} in [MHz] 2)
Sleep and Power down mode supply current caused by leakage 4)	I_{PDL} 5)	–	128,000 × $e^{-\alpha}$	mA	V_{DDI} = V_{DDImax} 6) T_J in [°C] α = 4670 / (273 + T_J)
Sleep and Power down mode supply current caused by leakage and the RTC running, clocked by the main oscillator 4)	I_{PDM} 7)	–	0.6 + 0.02 × f_{OSC} + I_{PDL}	mA	V_{DDI} = V_{DDImax} f_{OSC} in [MHz]

1) During Flash programming or erase operations the supply current is increased by max. 5 mA.

2) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 10**. These parameters are tested at V_{DDImax} and maximum CPU clock frequency with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

3) The pad supply voltage pins (V_{DDP}) mainly provides the current consumed by the pin output drivers. A small amount of current is consumed even though no outputs are driven, because the drivers' input stages are switched and also the Flash module draws some power from the V_{DDP} supply.

4) The total supply current in Sleep and Power down mode is the sum of the temperature dependent leakage current and the frequency dependent current for RTC and main oscillator (if active).

5) This parameter is determined mainly by the transistor leakage currents. This current heavily depends on the junction temperature (see **Figure 12**). The junction temperature T_J is the same as the ambient temperature T_A if no current flows through the port output drivers. Otherwise, the resulting temperature difference must be taken into account.

6) All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP}, all outputs (including pins configured as outputs) disconnected. This parameter is tested at 25 °C and is valid for $T_J \geq 25$ °C.

7) This parameter is determined mainly by the current consumed by the oscillator switched to low gain mode (see **Figure 11**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The given values refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

4.3 Analog/Digital Converter Parameters

Table 14 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	4.5	V_{DDP} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.1	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	20	MHz	3)
Conversion time for 10-bit result[4]	t_{C10P}	CC	$52 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. on
	t_{C10}	CC	$40 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. off
Conversion time for 8-bit result[4]	t_{C8P}	CC	$44 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. on
	t_{C8}	CC	$32 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. off
Calibration time after reset	t_{CAL}	CC	484	11,696	t_{BC}	5)
Total unadjusted error	TUE	CC	–	±2	LSB	1)
Total capacitance of an analog input	C_{AINT}	CC	–	15	pF	6)
Switched capacitance of an analog input	C_{AINS}	CC	–	10	pF	6)
Resistance of the analog input path	R_{AIN}	CC	–	2	kΩ	6)
Total capacitance of the reference input	C_{AREFT}	CC	–	20	pF	6)
Switched capacitance of the reference input	C_{AREFS}	CC	–	15	pF	6)
Resistance of the reference input path	R_{AREF}	CC	–	1	kΩ	6)

1) TUE is tested at $V_{AREF} = V_{DDP} + 0.1$ V, $V_{AGND} = 0$ V. It is verified by design for all other voltages within the defined voltage range.
If the analog reference supply voltage drops below 4.5 V (i.e. $V_{AREF} \geq 4.0$ V) or exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} = V_{DDP} + 0.2$ V) the maximum TUE is increased to ±3 LSB. This range is not subject to production test.
The specified TUE is guaranteed only, if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the respective period of time. During the reset calibration sequence the maximum TUE may be ±4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

3) The limit values for f_{BC} must not be exceeded when selecting the peripheral frequency and the ADCTC setting.
4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result (t_{SYS} = 1/f_{SYS}).
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 15**.
When the post-calibration is switched off, the conversion time is reduced by 12 × t_{BC}.
5) The actual duration of the reset calibration depends on the noise on the reference signal. Conversions executed during the reset calibration increase the calibration time. The TUE for those conversions may be increased.
6) Not subject to production test - verified by design/characterization.
The given parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) reduced values can be used for calculations. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 7 pF, R_{AINtyp} = 1.5 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 13 pF, $R_{AREFtyp}$ = 0.7 kΩ.

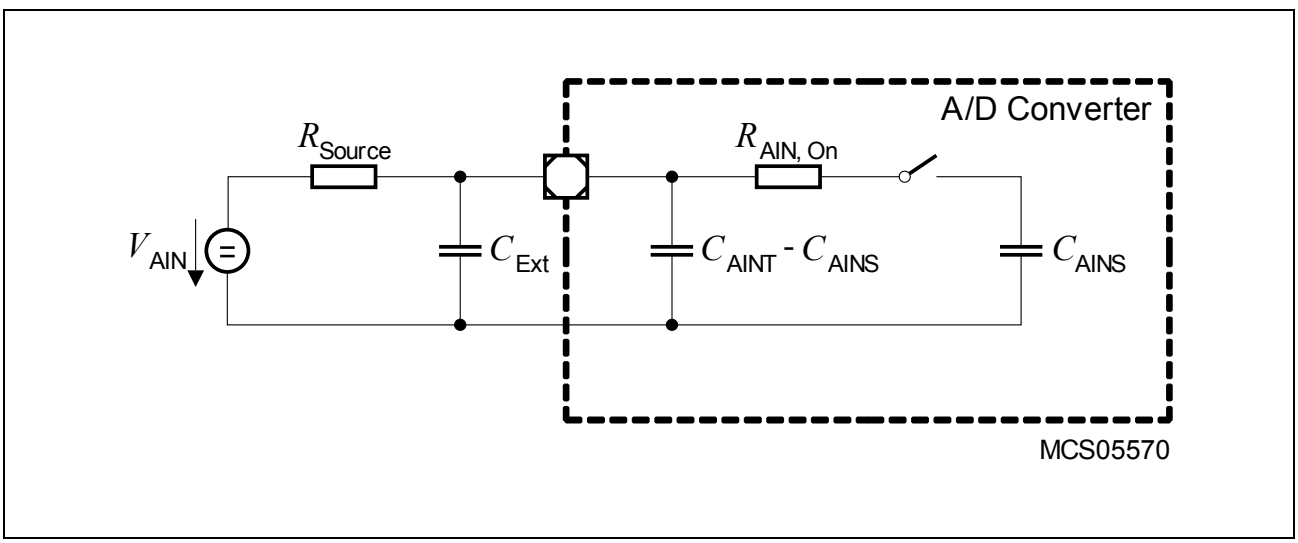
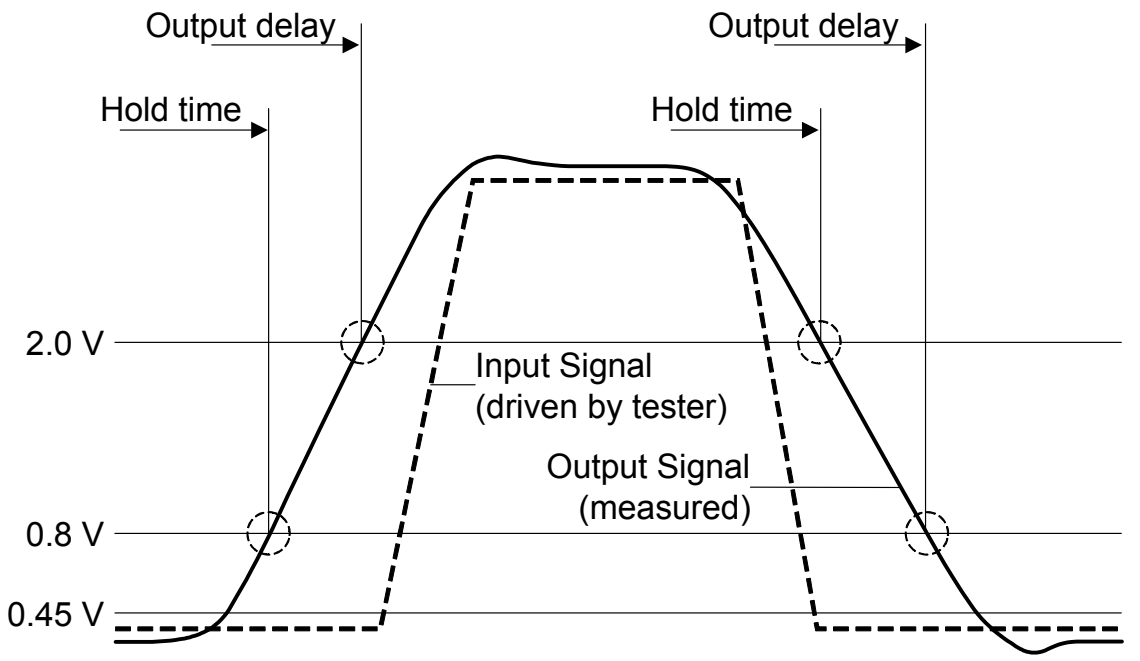


Figure 13 Equivalent Circuitry for Analog Inputs

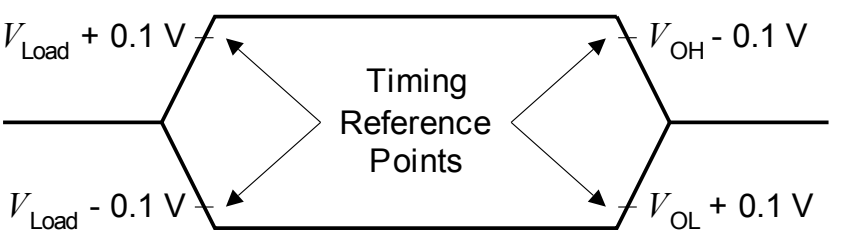
4.4.4 Testing Waveforms



Output timings refer to the rising edge of CLKOUT.
Input timings are calculated from the time, when the input signal reaches V_{IH} or V_{IL}, respectively.

MCD05556

Figure 17 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

MCA05565

Figure 18 Float Waveforms

Table 22 External Bus Cycle Timing (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
Output valid delay for: RD, WR(L/H)	tc_{10}	CC	1	13	ns
Output valid delay for: BHE, ALE	tc_{11}	CC	-1	7	ns
Output valid delay for: A23 … A16, A15 … A0 (on PORT1)	tc_{12}	CC	1	16	ns
Output valid delay for: A15 … A0 (on PORT0)	tc_{13}	CC	3	16	ns
Output valid delay for: CS	tc_{14}	CC	1	14	ns
Output valid delay for: D15 … D0 (write data, MUX-mode)	tc_{15}	CC	3	17	ns
Output valid delay for: D15 … D0 (write data, DEMUX-mode)	tc_{16}	CC	3	17	ns
Output hold time for: RD, WR(L/H)	tc_{20}	CC	-3	3	ns
Output hold time for: BHE, ALE	tc_{21}	CC	0	8	ns
Output hold time for: A23 … A16, A15 … A0 (on PORT0)	tc_{23}	CC	1	13	ns
Output hold time for: CS	tc_{24}	CC	-3	3	ns
Output hold time for: D15 … D0 (write data)	tc_{25}	CC	1	13	ns
Input setup time for: D15 … D0 (read data)	tc_{30}	SR	24	–	ns
Input hold time D15 … D0 (read data)[1)]	tc_{31}	SR	-5	–	ns

1) Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of RD. Therefore address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can be removed after the rising edge of RD.

Note: The shaded parameters have been verified by characterization. They are not subject to production test.

Package Outlines

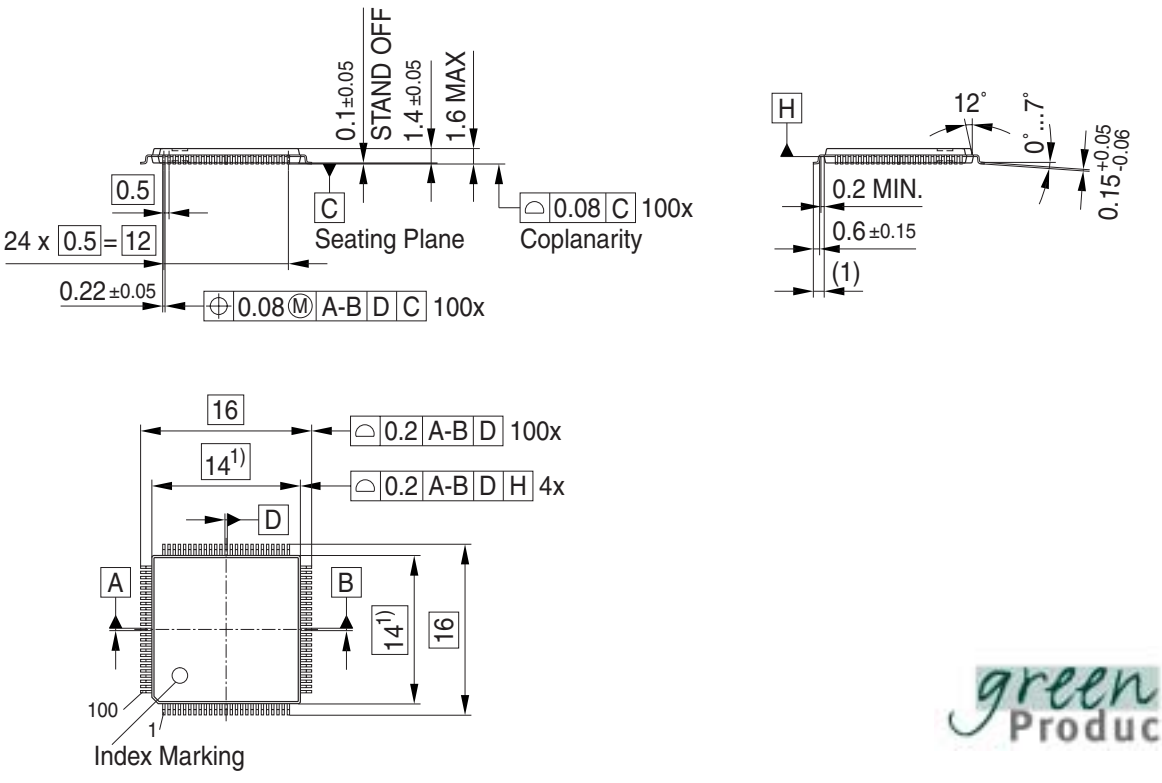


Figure 22 PG-TQFP-100-5 (Plastic Green Thin Quad Flat Package)