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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166SV2
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	79
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	PG-TQFP-100-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc164s-8f20f-bb

XC164S-16F/16R
XC164S-8F/8R

16-Bit Single-Chip Microcontroller with C166SV2 Core

Microcontrollers

Never stop thinking

2.2 Pin Configuration and Definition

The pins of the XC164S are described in detail in **Table 3**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the package. E*) mark pins to be used as alternate external interrupt inputs.

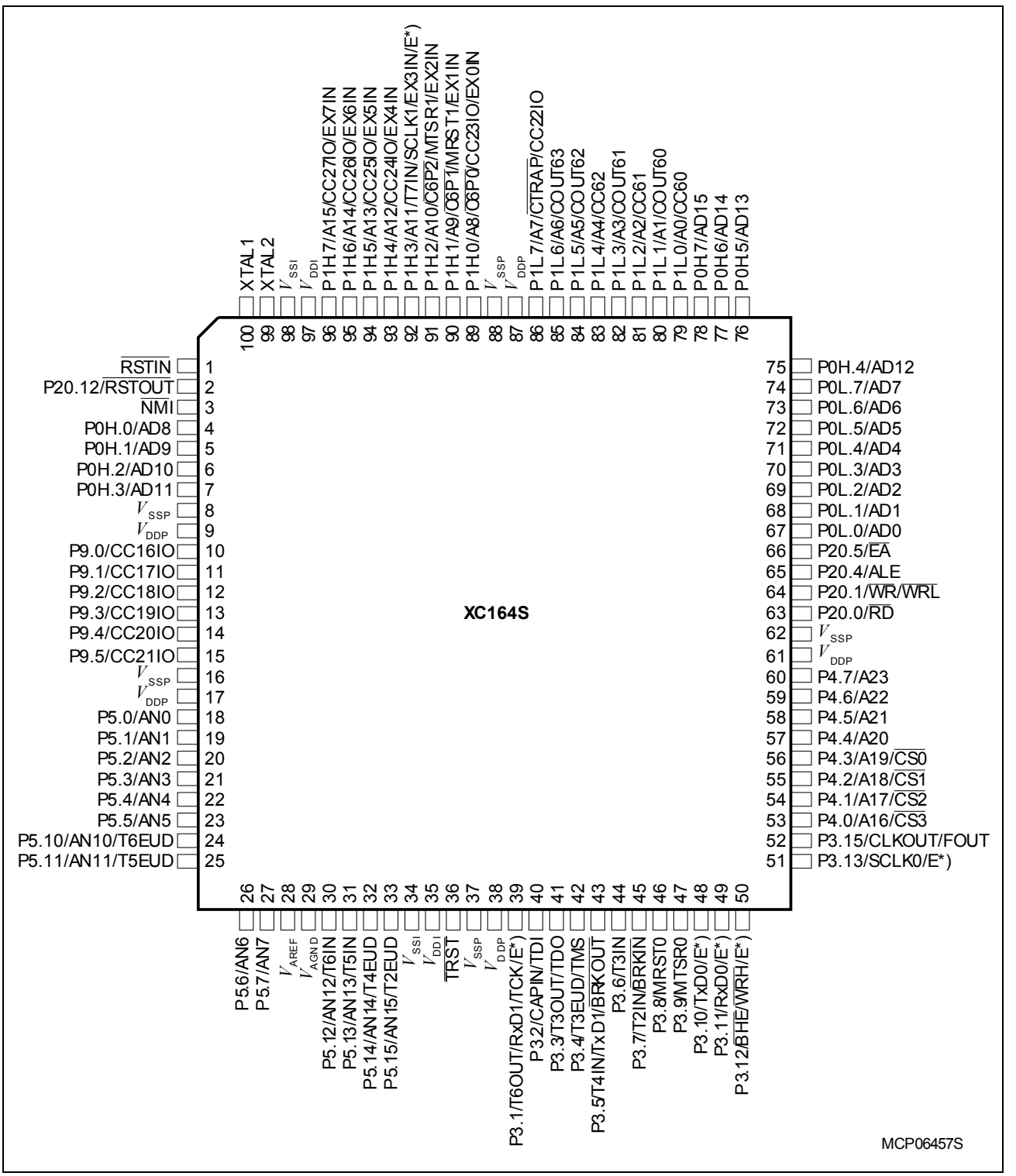


Figure 2 Pin Configuration (top view)

3 Functional Description

The architecture of the XC164S combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources as well as external resources (see **Figure 3**).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC164S.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC164S.

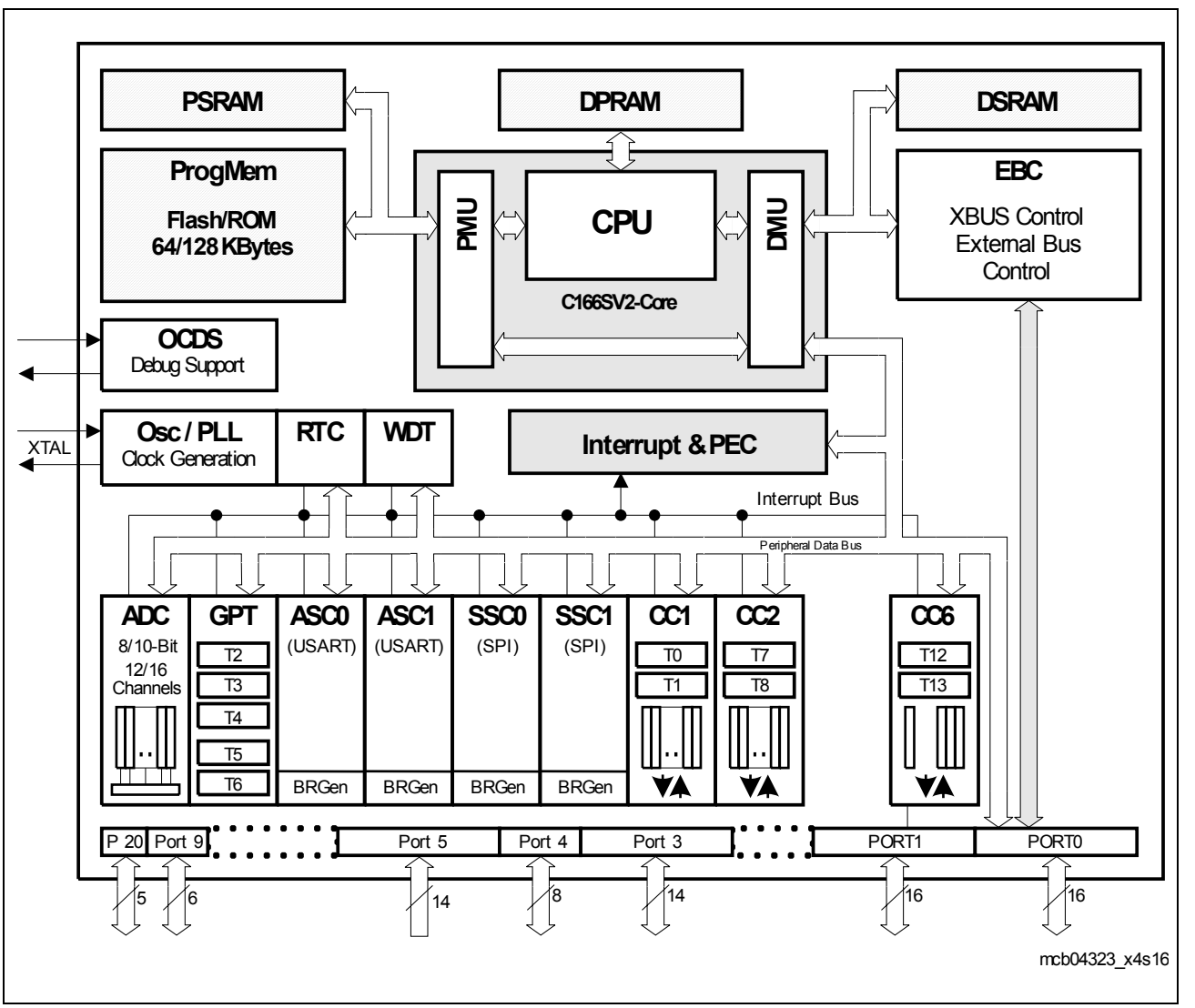


Figure 3 Block Diagram

bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bitaddressable. When used by a GPR, any location in the DPRAM is bitaddressable.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC166 Family. Therefore, they should either not be accessed, or written with zeros, to ensure upward compatibility.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 12 Mbytes (approximately, see **Table 3**) of external RAM and/or ROM can be connected to the microcontroller.

Table 3 XC164S Memory Map[1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
Flash register space	$FF'F000_H$	$FF'FFFF_H$	4 Kbytes	Flash only[3)]
Reserved (Acc. trap)	$F8'0000_H$	$FF'EFFF_H$	< 0.5 Mbytes	Minus Flash register space
Reserved for PSRAM	$E0'0800_H$	$F7'FFFF_H$	< 1.5 Mbytes	Minus PSRAM
Program SRAM	$E0'0000_H$	$E0'07FF_H$	2 Kbytes	Maximum
Reserved for program memory	$C2'0000_H$	$DF'FFFF_H$	< 2 Mbytes	Minus Flash
Program Flash/ROM	$C0'0000_H$	$C1'FFFF_H$	128 Kbytes	[4)]
Reserved	$BF'0000_H$	$BF'FFFF_H$	64 Kbytes	–
External memory area	$40'0000_H$	$BE'FFFF_H$	< 8 Mbytes	Minus reserved segment
External IO area[5)]	$20'0800_H$	$3F'FFFF_H$	< 2 Mbytes	Minus 2 Kbytes
Reserved	$20'0000_H$	$20'07FF_H$	2 Kbytes	–
External memory area	$01'0000_H$	$1F'FFFF_H$	< 2 Mbytes	Minus segment 0
Data RAMs and SFRs	$00'8000_H$	$00'FFFF_H$	32 Kbytes	Partly used[4)]
External memory area	$00'0000_H$	$00'7FFF_H$	32 Kbytes	–

1) Accesses to the shaded areas generate external bus accesses.
2) The areas marked with “<” are slightly smaller than indicated, see column “Notes”.
3) Not defined register locations return a trap code.
4) Depends on the respective derivative. The derivatives are listed in **Table 1**.
5) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes[1)], which are as follows:

- 16 … 24-bit Addresses, 16-bit Data, Demultiplexed
- 16 … 24-bit Addresses, 16-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output. The high order address (segment) lines use Port 4. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines are assigned to Port 4.

Up to 4 external $\overline{CS}$ signals (3 windows plus default) can be generated in order to save external glue logic. External modules can directly be connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface have been made programmable (via registers TCONCSx/FCONCSx) to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via registers ADDRSELx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these 4 address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

Note: The chip select signal of address window 4 is not available on a pin.

The external bus timing is related to the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

The EBC also controls accesses to resources connected to the on-chip LXBus. The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

The TwinCAN module is connected and accessed via the LXBus.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

3.3 Central Processing Unit (CPU)

The main core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply and divide unit, a bit-mask generator, and a barrel shifter.

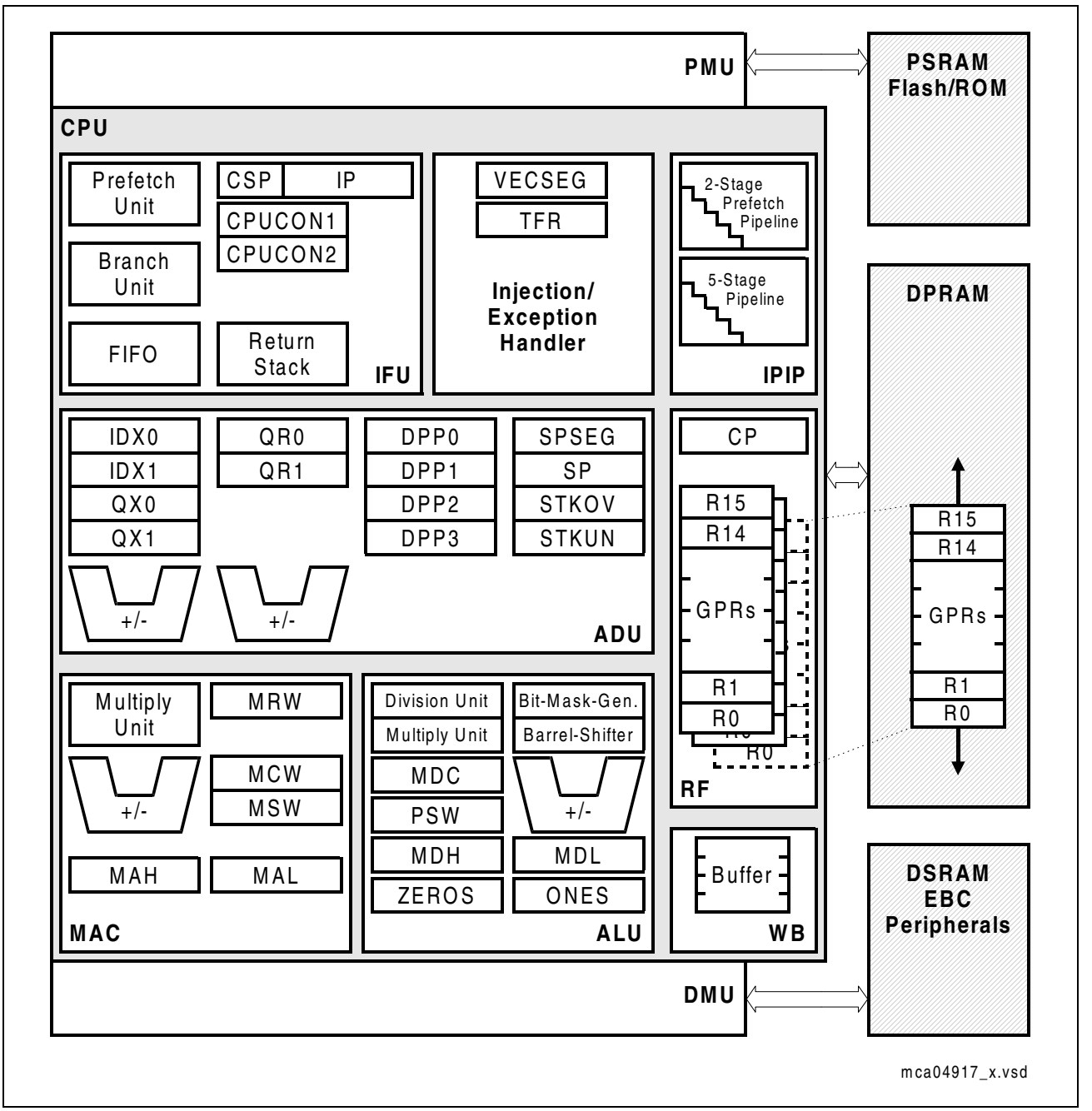


Figure 4 CPU Block Diagram

Based on these hardware provisions, most of the XC164S's instructions can be executed in just one machine cycle which requires 25 ns at 40 MHz CPU clock. For

3.4 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164S is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164S supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164S has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 4 shows all of the possible XC164S interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 4 XC164S Interrupt Nodes

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM Register 0	CC1_CC0IC	xx'0040$_H$	10$_H$ / 16$_D$
CAPCOM Register 1	CC1_CC1IC	xx'0044$_H$	11$_H$ / 17$_D$
CAPCOM Register 2	CC1_CC2IC	xx'0048$_H$	12$_H$ / 18$_D$
CAPCOM Register 3	CC1_CC3IC	xx'004C$_H$	13$_H$ / 19$_D$
CAPCOM Register 4	CC1_CC4IC	xx'0050$_H$	14$_H$ / 20$_D$
CAPCOM Register 5	CC1_CC5IC	xx'0054$_H$	15$_H$ / 21$_D$
CAPCOM Register 6	CC1_CC6IC	xx'0058$_H$	16$_H$ / 22$_D$
CAPCOM Register 7	CC1_CC7IC	xx'005C$_H$	17$_H$ / 23$_D$
CAPCOM Register 8	CC1_CC8IC	xx'0060$_H$	18$_H$ / 24$_D$
CAPCOM Register 9	CC1_CC9IC	xx'0064$_H$	19$_H$ / 25$_D$
CAPCOM Register 10	CC1_CC10IC	xx'0068$_H$	1A$_H$ / 26$_D$
CAPCOM Register 11	CC1_CC11IC	xx'006C$_H$	1B$_H$ / 27$_D$
CAPCOM Register 12	CC1_CC12IC	xx'0070$_H$	1C$_H$ / 28$_D$
CAPCOM Register 13	CC1_CC13IC	xx'0074$_H$	1D$_H$ / 29$_D$
CAPCOM Register 14	CC1_CC14IC	xx'0078$_H$	1E$_H$ / 30$_D$
CAPCOM Register 15	CC1_CC15IC	xx'007C$_H$	1F$_H$ / 31$_D$
CAPCOM Register 16	CC2_CC16IC	xx'00C0$_H$	30$_H$ / 48$_D$
CAPCOM Register 17	CC2_CC17IC	xx'00C4$_H$	31$_H$ / 49$_D$
CAPCOM Register 18	CC2_CC18IC	xx'00C8$_H$	32$_H$ / 50$_D$
CAPCOM Register 19	CC2_CC19IC	xx'00CC$_H$	33$_H$ / 51$_D$
CAPCOM Register 20	CC2_CC20IC	xx'00D0$_H$	34$_H$ / 52$_D$
CAPCOM Register 21	CC2_CC21IC	xx'00D4$_H$	35$_H$ / 53$_D$
CAPCOM Register 22	CC2_CC22IC	xx'00D8$_H$	36$_H$ / 54$_D$
CAPCOM Register 23	CC2_CC23IC	xx'00DC$_H$	37$_H$ / 55$_D$
CAPCOM Register 24	CC2_CC24IC	xx'00E0$_H$	38$_H$ / 56$_D$
CAPCOM Register 25	CC2_CC25IC	xx'00E4$_H$	39$_H$ / 57$_D$
CAPCOM Register 26	CC2_CC26IC	xx'00E8$_H$	3A$_H$ / 58$_D$
CAPCOM Register 27	CC2_CC27IC	xx'00EC$_H$	3B$_H$ / 59$_D$
CAPCOM Register 28	CC2_CC28IC	xx'00F0$_H$	3C$_H$ / 60$_D$

Table 4 XC164S Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM Register 29	CC2_CC29IC	xx'0110$_H$	44$_H$ / 68$_D$
CAPCOM Register 30	CC2_CC30IC	xx'0114$_H$	45$_H$ / 69$_D$
CAPCOM Register 31	CC2_CC31IC	xx'0118$_H$	46$_H$ / 70$_D$
CAPCOM Timer 0	CC1_T0IC	xx'0080$_H$	20$_H$ / 32$_D$
CAPCOM Timer 1	CC1_T1IC	xx'0084$_H$	21$_H$ / 33$_D$
CAPCOM Timer 7	CC2_T7IC	xx'00F4$_H$	3D$_H$ / 61$_D$
CAPCOM Timer 8	CC2_T8IC	xx'00F8$_H$	3E$_H$ / 62$_D$
GPT1 Timer 2	GPT12E_T2IC	xx'0088$_H$	22$_H$ / 34$_D$
GPT1 Timer 3	GPT12E_T3IC	xx'008C$_H$	23$_H$ / 35$_D$
GPT1 Timer 4	GPT12E_T4IC	xx'0090$_H$	24$_H$ / 36$_D$
GPT2 Timer 5	GPT12E_T5IC	xx'0094$_H$	25$_H$ / 37$_D$
GPT2 Timer 6	GPT12E_T6IC	xx'0098$_H$	26$_H$ / 38$_D$
GPT2 CAPREL Register	GPT12E_CRIC	xx'009C$_H$	27$_H$ / 39$_D$
A/D Conversion Complete	ADC_CIC	xx'00A0$_H$	28$_H$ / 40$_D$
A/D Overrun Error	ADC_EIC	xx'00A4$_H$	29$_H$ / 41$_D$
ASC0 Transmit	ASC0_TIC	xx'00A8$_H$	2A$_H$ / 42$_D$
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C$_H$	47$_H$ / 71$_D$
ASC0 Receive	ASC0_RIC	xx'00AC$_H$	2B$_H$ / 43$_D$
ASC0 Error	ASC0_EIC	xx'00B0$_H$	2C$_H$ / 44$_D$
ASC0 Autobaud	ASC0_ABIC	xx'017C$_H$	5F$_H$ / 95$_D$
SSC0 Transmit	SSC0_TIC	xx'00B4$_H$	2D$_H$ / 45$_D$
SSC0 Receive	SSC0_RIC	xx'00B8$_H$	2E$_H$ / 46$_D$
SSC0 Error	SSC0_EIC	xx'00BC$_H$	2F$_H$ / 47$_D$
PLL/OWD	PLLIC	xx'010C$_H$	43$_H$ / 67$_D$
ASC1 Transmit	ASC1_TIC	xx'0120$_H$	48$_H$ / 72$_D$
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178$_H$	5E$_H$ / 94$_D$
ASC1 Receive	ASC1_RIC	xx'0124$_H$	49$_H$ / 73$_D$
ASC1 Error	ASC1_EIC	xx'0128$_H$	4A$_H$ / 74$_D$
ASC1 Autobaud	ASC1_ABIC	xx'0108$_H$	42$_H$ / 66$_D$
End of PEC Subchannel	EOPIC	xx'0130$_H$	4C$_H$ / 76$_D$

Table 4 XC164S Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM6 Timer T12	CCU6_T12IC	xx'0134$_H$	4D$_H$ / 77$_D$
CAPCOM6 Timer T13	CCU6_T13IC	xx'0138$_H$	4E$_H$ / 78$_D$
CAPCOM6 Emergency	CCU6_EIC	xx'013C$_H$	4F$_H$ / 79$_D$
CAPCOM6	CCU6_IC	xx'0140$_H$	50$_H$ / 80$_D$
SSC1 Transmit	SSC1_TIC	xx'0144$_H$	51$_H$ / 81$_D$
SSC1 Receive	SSC1_RIC	xx'0148$_H$	52$_H$ / 82$_D$
SSC1 Error	SSC1_EIC	xx'014C$_H$	53$_H$ / 83$_D$
Unassigned node	–	xx'0150$_H$	54$_H$ / 84$_D$
Unassigned node	–	xx'0154$_H$	55$_H$ / 85$_D$
Unassigned node	–	xx'0158$_H$	56$_H$ / 86$_D$
Unassigned node	–	xx'015C$_H$	57$_H$ / 87$_D$
Unassigned node	–	xx'0164$_H$	59$_H$ / 89$_D$
Unassigned node	–	xx'0168$_H$	5A$_H$ / 90$_D$
Unassigned node	–	xx'016C$_H$	5B$_H$ / 91$_D$
Unassigned node	–	xx'0170$_H$	5C$_H$ / 92$_D$
Unassigned node	–	xx'0174$_H$	5D$_H$ / 93$_D$
Unassigned node	–	xx'0100$_H$	40$_H$ / 64$_D$
Unassigned node	–	xx'0104$_H$	41$_H$ / 65$_D$
Unassigned node	–	xx'012C$_H$	4B$_H$ / 75$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'0160$_H$	58$_H$ / 88$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

compare function.
12 registers of the CAPCOM2 module have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

Table 6 Compare Modes (CAPCOM1/2)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare timer overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; can be used with any compare mode

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

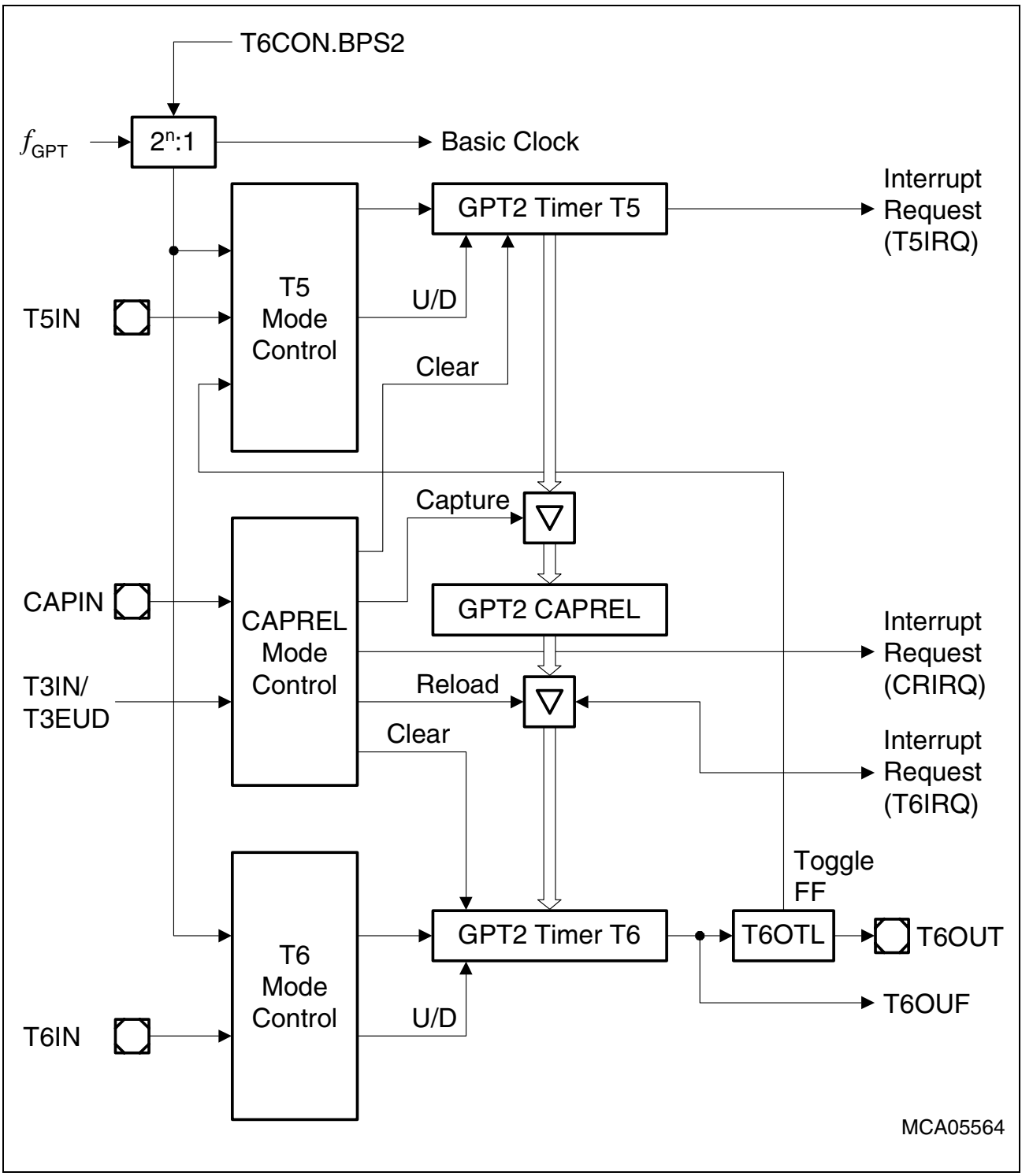


Figure 8 Block Diagram of GPT2

3.12 High Speed Synchronous Serial Channels (SSC0/SSC1)

The High Speed Synchronous Serial Channels SSC0/SSC1 support full-duplex and half-duplex synchronous communication. It may be configured so it interfaces with serially linked peripheral components, full SPI functionality is supported.

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling three separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 … 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit error and receive error supervise the correct handling of the data buffer. Phase error and baudrate error detect incorrect serial data.

Summary of Features

- Master or Slave mode operation
- Full-duplex or Half-duplex transfers
- Baudrate generation from 20 Mbit/s to 305.18 bit/s (@ 40 MHz)
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB-first or MSB-first
  - Programmable clock polarity: idle low or idle high
  - Programmable clock/data phase: data shift with leading or trailing clock edge
- Loop back option available for testing purposes
- Interrupt generation on transmitter buffer empty condition, receive buffer full condition, error condition (receive, phase, baudrate, transmit error)
- Three pin interface with flexible SSC pin configuration

Table 11 DC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Level inactive hold current[13]	I_{LHI}[10]		–	-10	µA	V_{OUT} = 0.5 × V_{DDP}
Level active hold current[13]	I_{LHA}[11]		-100	–	µA	V_{OUT} = 0.45 V
XTAL1 input current	I_{IL}	CC	–	±20	µA	0 V < V_{IN} < V_{DDI}
Pin capacitance[14] (digital inputs/outputs)	C_{IO}	CC	–	10	pF	–

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) If XTAL1 is driven by a crystal, reaching an amplitude (peak to peak) of 0.4 × V_{DDI} is sufficient.

3) This parameter is tested for P3, P4, P9.

4) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 12, Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

5) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are guaranteed.

6) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

7) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

8) The driver of P3.15 is designed for faster switching, because this pin can deliver the reference clock for the bus interface (CLKOUT). The maximum leakage current for P3.15 is, therefore, increased to 1 µA.

9) This specification is valid during Reset for configuration on $\overline{RD}$, $\overline{WR}$, $\overline{EA}$, PORT0

10) The maximum current may be drawn while the respective signal line remains inactive.

11) The minimum current must be drawn to drive the respective signal line active.

12) This specification is valid during Reset for configuration on ALE.

13) This specification is valid during Reset for pins P4.3-0, which can act as $\overline{CS}$ outputs, and for P3.12.

14) Not subject to production test - verified by design/characterization.

Table 12 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]	Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)
Strong driver	10 mA	2.5 mA
Medium driver	4.0 mA	1.0 mA
Weak driver	0.5 mA	0.1 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time.
For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and $\Sigma\text{-}I_{OH}$) must remain below 50 mA.

Table 13 Power Consumption XC164S (Operating Conditions apply)

Parameter	Sym-bol	Limit Values		Unit	Test Condition
		Min.	Max.		
Power supply current (active) with all peripherals active	I_{DDI}	–	15 + 2.6 × f_{CPU}	mA	f_{CPU} in [MHz] 1)2)
Pad supply current	I_{DDP}	–	5	mA	3)
Idle mode supply current with all peripherals active	I_{IDX}	–	15 + 1.2 × f_{CPU}	mA	f_{CPU} in [MHz] 2)
Sleep and Power down mode supply current caused by leakage 4)	I_{PDL} 5)	–	128,000 × $e^{-\alpha}$	mA	V_{DDI} = V_{DDImax} 6) T_J in [°C] α = 4670 / (273 + T_J)
Sleep and Power down mode supply current caused by leakage and the RTC running, clocked by the main oscillator 4)	I_{PDM} 7)	–	0.6 + 0.02 × f_{OSC} + I_{PDL}	mA	V_{DDI} = V_{DDImax} f_{OSC} in [MHz]

1) During Flash programming or erase operations the supply current is increased by max. 5 mA.

2) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 10**. These parameters are tested at V_{DDImax} and maximum CPU clock frequency with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

3) The pad supply voltage pins (V_{DDP}) mainly provides the current consumed by the pin output drivers. A small amount of current is consumed even though no outputs are driven, because the drivers' input stages are switched and also the Flash module draws some power from the V_{DDP} supply.

4) The total supply current in Sleep and Power down mode is the sum of the temperature dependent leakage current and the frequency dependent current for RTC and main oscillator (if active).

5) This parameter is determined mainly by the transistor leakage currents. This current heavily depends on the junction temperature (see **Figure 12**). The junction temperature T_J is the same as the ambient temperature T_A if no current flows through the port output drivers. Otherwise, the resulting temperature difference must be taken into account.

6) All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP}, all outputs (including pins configured as outputs) disconnected. This parameter is tested at 25 °C and is valid for $T_J \geq 25$ °C.

7) This parameter is determined mainly by the current consumed by the oscillator switched to low gain mode (see **Figure 11**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The given values refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

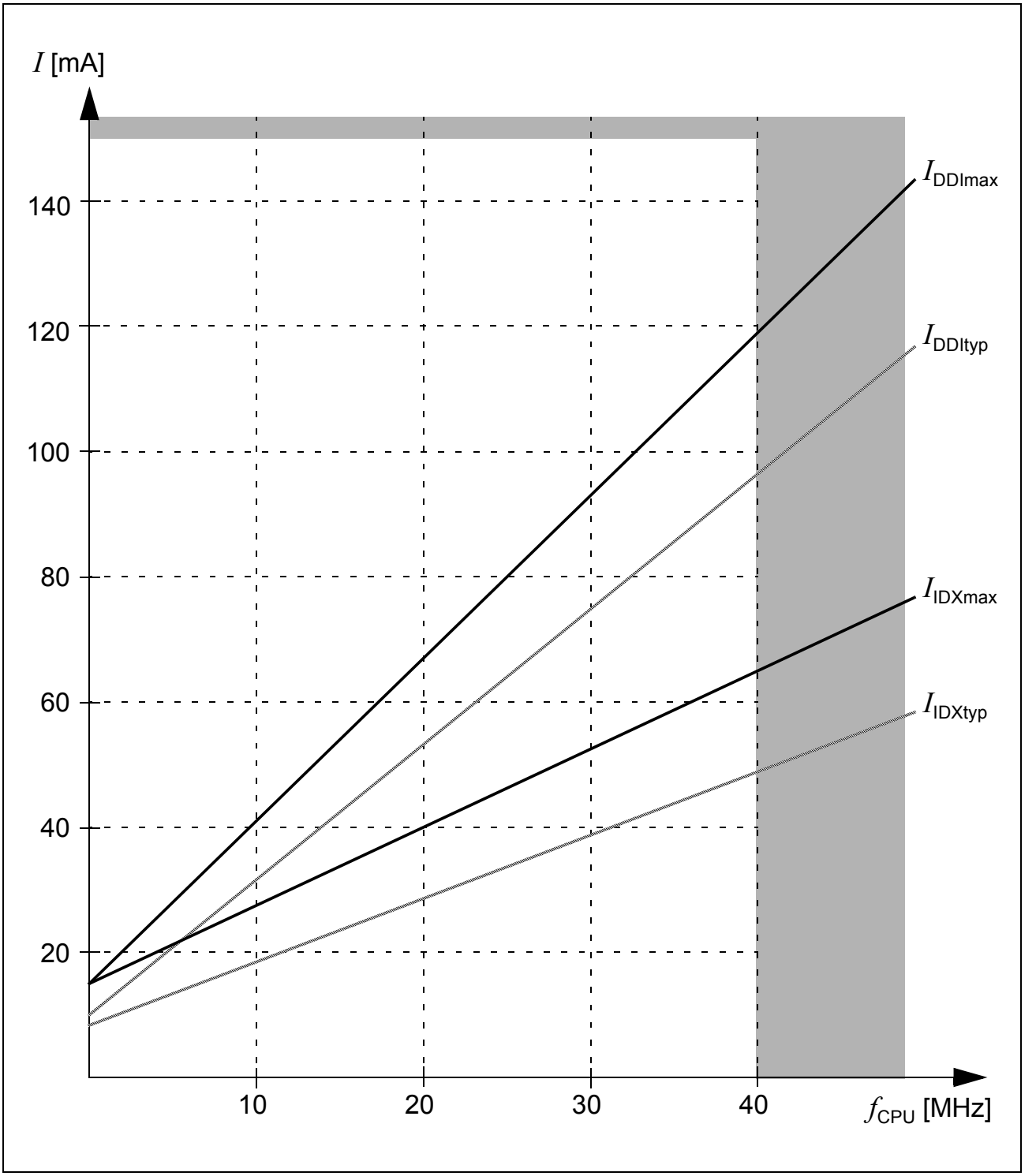


Figure 10 Supply/Idle Current as a Function of Operating Frequency

3) The limit values for f_{BC} must not be exceeded when selecting the peripheral frequency and the ADCTC setting.
4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result (t_{SYS} = 1/f_{SYS}).
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 15**.
When the post-calibration is switched off, the conversion time is reduced by 12 × t_{BC}.
5) The actual duration of the reset calibration depends on the noise on the reference signal. Conversions executed during the reset calibration increase the calibration time. The TUE for those conversions may be increased.
6) Not subject to production test - verified by design/characterization.
The given parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) reduced values can be used for calculations. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 7 pF, R_{AINtyp} = 1.5 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 13 pF, $R_{AREFtyp}$ = 0.7 kΩ.

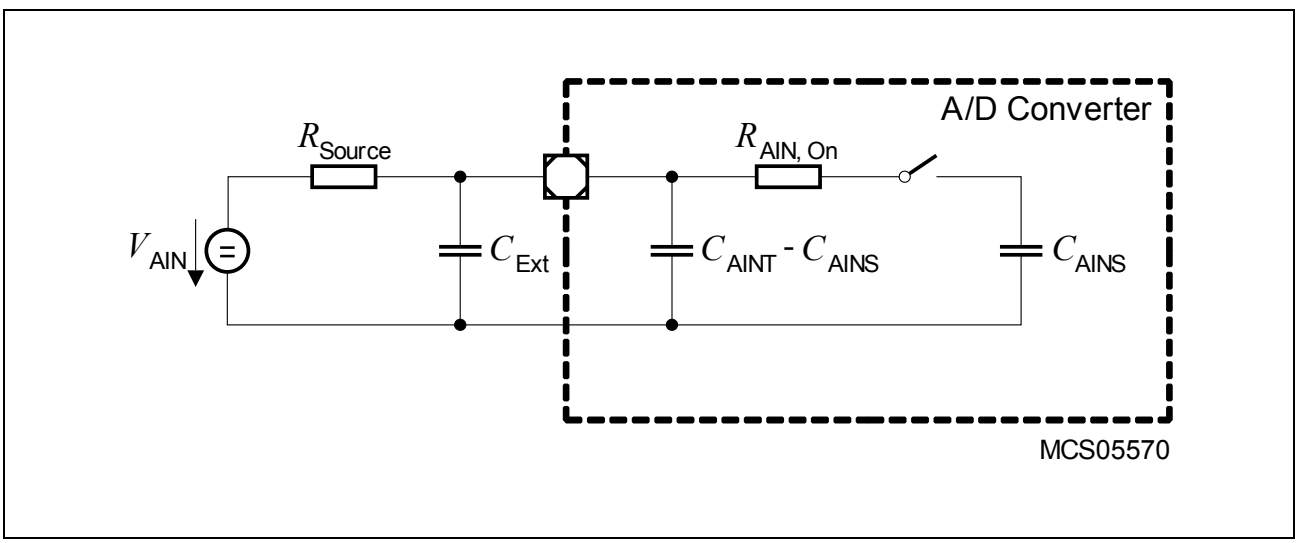
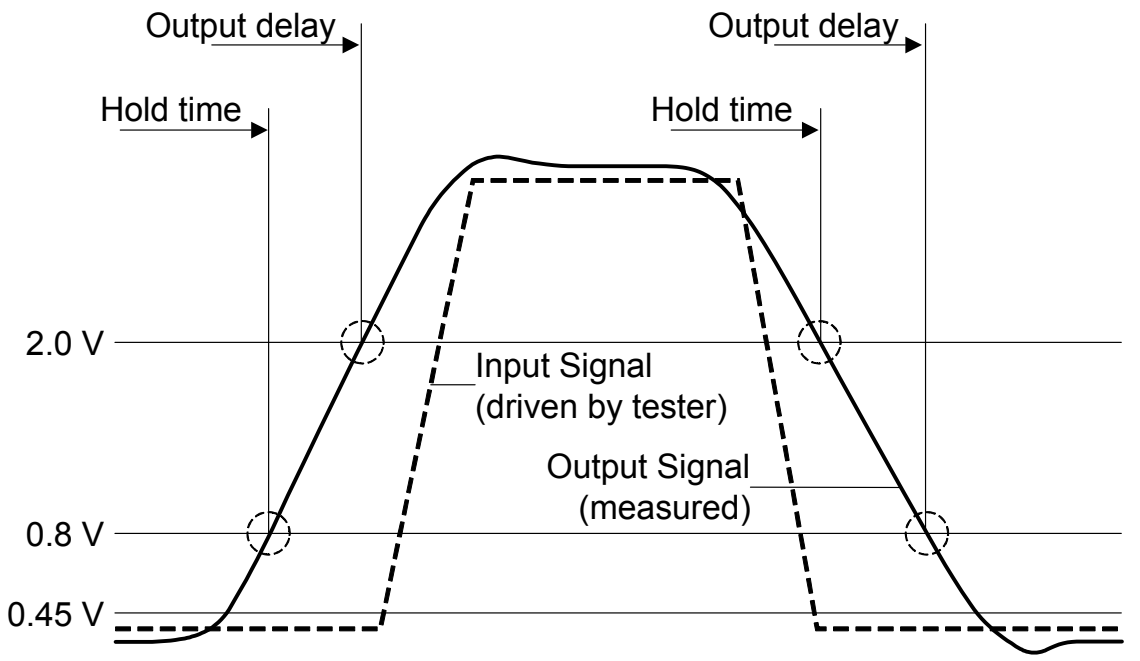


Figure 13 Equivalent Circuitry for Analog Inputs

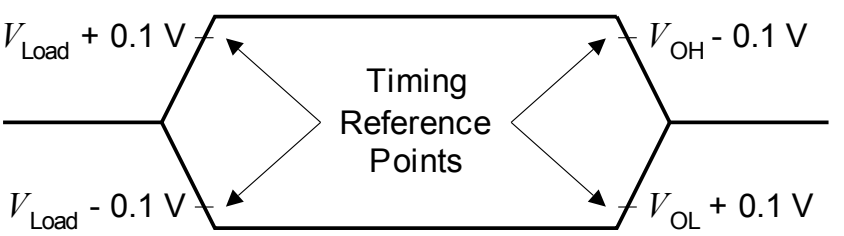
4.4.4 Testing Waveforms



Output timings refer to the rising edge of CLKOUT.
Input timings are calculated from the time, when the input signal reaches V_{IH} or V_{IL}, respectively.

MCD05556

Figure 17 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

MCA05565

Figure 18 Float Waveforms

Package Outlines

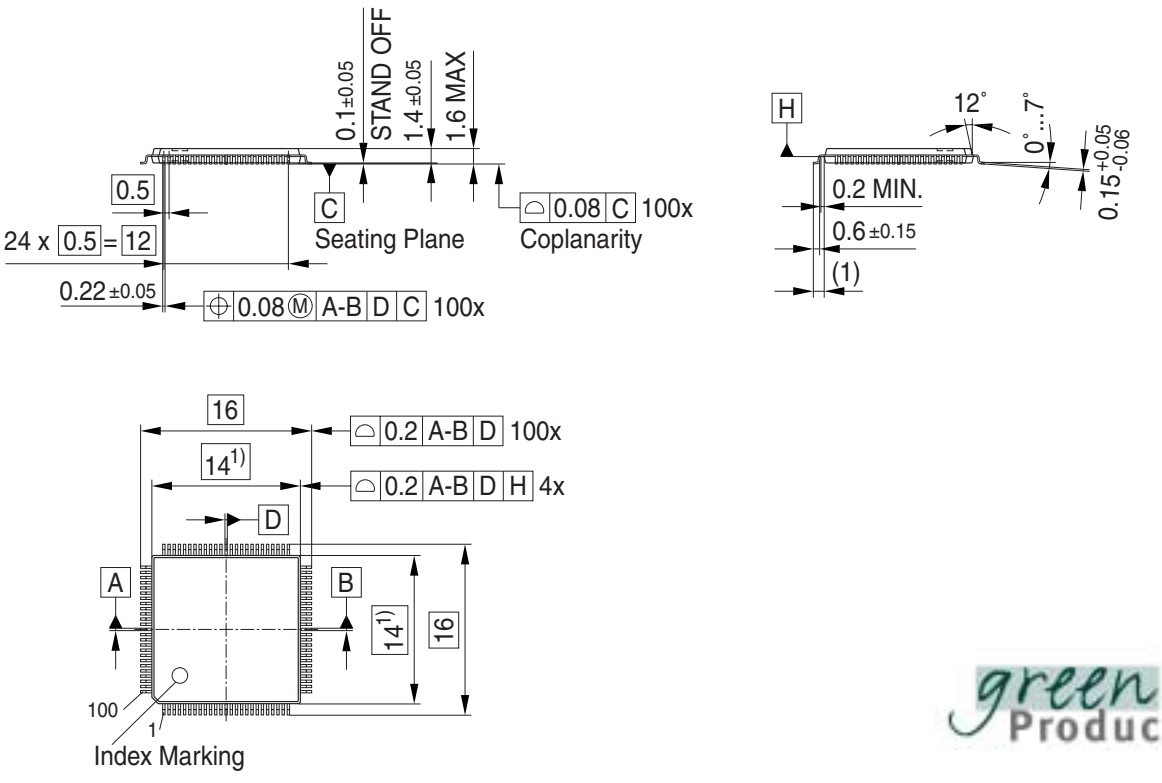


Figure 22 PG-TQFP-100-5 (Plastic Green Thin Quad Flat Package)

w w w . i n f i n e o n . c o m

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