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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	79
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	PG-TQFP-100-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc164s-8f40f-bb

XC164S
Revision History: V1.2, 2006-08

Previous Version(s):
V1.1, 2006-03
V1.0, 2005-01

Page	Subjects (major changes since last revision)
6	New derivatives added.
10	Description of the $\overline{\text{TRST}}$ signal modified.
45	Instructions Set Summary improved.
48	Footnote added about pin XTAL1 belonging to V_{DDI} power domain.
52	Footnote added about amplitude at XTAL1 pin.
71	Thermal Resistance: R_{THA} replaced by $R_{\Theta JC}$ and $R_{\Theta JL}$ because R_{THA} strongly depends on the external system (PCB, environment). P_{DISS} removed, because no static parameter, but derived from thermal resistance.
72	Green Package added.

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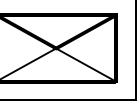

Table of Contents

Table 2 Pin Definitions and Functions

Symbol	Pin Num.	Input Outp.	Function
$\overline{\text{RSTIN}}$	1	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the XC164S. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. *Note: The reset duration must be sufficient to let the hardware configuration signals settle. External circuitry must guarantee low level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.*
P20.12	2	IO	For details, please refer to the description of **P20**.
$\overline{\text{NMI}}$	3	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the XC164S into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.
P0H.0-P0H.3	4…7	IO	For details, please refer to the description of **PORT0**.
P9		IO	Port 9 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 9 is selectable (standard or special). The following Port 9 pins also serve for alternate functions:
P9.0	10	I/O I	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp., EX7IN Fast External Interrupt 7 Input (alternate pin B)
P9.1	11	I/O I	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp., EX6IN Fast External Interrupt 6 Input (alternate pin B)
P9.2	12	I/O I	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp., EX7IN Fast External Interrupt 7 Input (alternate pin A)
P9.3	13	I/O I	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp., EX6IN Fast External Interrupt 6 Input (alternate pin A)
P9.4	14	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.
P9.5	15	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
P3		IO	Port 3 is a 14-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:	
P3.1	39	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin A),
		I	TCK	Debug System: JTAG Clock Input
P3.2	40	I	CAPIN	GPT2 Register CAPREL Capture Input,
		I	TDI	Debug System: JTAG Data In
P3.3	41	O	T3OUT	GPT1 Timer T3 Toggle Latch Output,
		O	TDO	Debug System: JTAG Data Out
P3.4	42	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input,
		I	TMS	Debug System: JTAG Test Mode Selection
P3.5	43	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp
		O	TxD1	ASC0 Clock/Data Output (Async./Sync.),
		O	BRKOUT	Debug System: Break Out
P3.6	44	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	45	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp
		I	BRKIN	Debug System: Break In
P3.8	46	I/O	MRST0	SSC0 Master-Receive/Slave-Transmit In/Out.
P3.9	47	I/O	MTSR0	SSC0 Master-Transmit/Slave-Receive Out/In.
P3.10	48	O	TxD0	ASC0 Clock/Data Output (Async./Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin B)
P3.11	49	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin A)
P3.12	50	O	BHE	External Memory High Byte Enable Signal,
		O	WRH	External Memory High Byte Write Strobe,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin B)
P3.13	51	I/O	SCLK0	SSC0 Master Clock Output / Slave Clock Input.,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin A)
P3.15	52	O	CLKOUT	System Clock Output (= CPU Clock),
		O	FOUT	Programmable Frequency Output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
P4		IO	Port 4 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 4 is selectable (standard or special). Port 4 can be used to output the segment address lines, the optional chip select lines, and for serial interface lines:	
P4.0	53	O	$\overline{\text{A16}}$	Least Significant Segment Address Line,
		O	$\overline{\text{CS3}}$	Chip Select 3 Output
P4.1	54	O	$\overline{\text{A17}}$	Segment Address Line,
		O	$\overline{\text{CS2}}$	Chip Select 2 Output
P4.2	55	O	$\overline{\text{A18}}$	Segment Address Line,
		O	$\overline{\text{CS1}}$	Chip Select 1 Output
P4.3	56	O	$\overline{\text{A19}}$	Segment Address Line,
		O	$\overline{\text{CS0}}$	Chip Select 0 Output
P4.4	57	O	A20	Segment Address Line,
		I	EX5IN	Fast External Interrupt 5 Input (alternate pin B)
P4.5	58	O	A21	Segment Address Line,
		I	EX4IN	Fast External Interrupt 4 Input (alternate pin B)
P4.6	59	O	A22	Segment Address Line,
		I	EX5IN	Fast External Interrupt 5 Input (alternate pin A)
P4.7	60	O	A23	Most Significant Segment Address Line,
		I	EX4IN	Fast External Interrupt 4 Input (alternate pin A)

3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes[1)], which are as follows:

- 16 … 24-bit Addresses, 16-bit Data, Demultiplexed
- 16 … 24-bit Addresses, 16-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output. The high order address (segment) lines use Port 4. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines are assigned to Port 4.

Up to 4 external $\overline{CS}$ signals (3 windows plus default) can be generated in order to save external glue logic. External modules can directly be connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface have been made programmable (via registers TCONCSx/FCONCSx) to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via registers ADDRSELx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these 4 address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

Note: The chip select signal of address window 4 is not available on a pin.

The external bus timing is related to the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

The EBC also controls accesses to resources connected to the on-chip LXBus. The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

The TwinCAN module is connected and accessed via the LXBus.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

3.4 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164S is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164S supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164S has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 4 shows all of the possible XC164S interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 4 XC164S Interrupt Nodes

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM Register 0	CC1_CC0IC	xx'0040$_H$	10$_H$ / 16$_D$
CAPCOM Register 1	CC1_CC1IC	xx'0044$_H$	11$_H$ / 17$_D$
CAPCOM Register 2	CC1_CC2IC	xx'0048$_H$	12$_H$ / 18$_D$
CAPCOM Register 3	CC1_CC3IC	xx'004C$_H$	13$_H$ / 19$_D$
CAPCOM Register 4	CC1_CC4IC	xx'0050$_H$	14$_H$ / 20$_D$
CAPCOM Register 5	CC1_CC5IC	xx'0054$_H$	15$_H$ / 21$_D$
CAPCOM Register 6	CC1_CC6IC	xx'0058$_H$	16$_H$ / 22$_D$
CAPCOM Register 7	CC1_CC7IC	xx'005C$_H$	17$_H$ / 23$_D$
CAPCOM Register 8	CC1_CC8IC	xx'0060$_H$	18$_H$ / 24$_D$
CAPCOM Register 9	CC1_CC9IC	xx'0064$_H$	19$_H$ / 25$_D$
CAPCOM Register 10	CC1_CC10IC	xx'0068$_H$	1A$_H$ / 26$_D$
CAPCOM Register 11	CC1_CC11IC	xx'006C$_H$	1B$_H$ / 27$_D$
CAPCOM Register 12	CC1_CC12IC	xx'0070$_H$	1C$_H$ / 28$_D$
CAPCOM Register 13	CC1_CC13IC	xx'0074$_H$	1D$_H$ / 29$_D$
CAPCOM Register 14	CC1_CC14IC	xx'0078$_H$	1E$_H$ / 30$_D$
CAPCOM Register 15	CC1_CC15IC	xx'007C$_H$	1F$_H$ / 31$_D$
CAPCOM Register 16	CC2_CC16IC	xx'00C0$_H$	30$_H$ / 48$_D$
CAPCOM Register 17	CC2_CC17IC	xx'00C4$_H$	31$_H$ / 49$_D$
CAPCOM Register 18	CC2_CC18IC	xx'00C8$_H$	32$_H$ / 50$_D$
CAPCOM Register 19	CC2_CC19IC	xx'00CC$_H$	33$_H$ / 51$_D$
CAPCOM Register 20	CC2_CC20IC	xx'00D0$_H$	34$_H$ / 52$_D$
CAPCOM Register 21	CC2_CC21IC	xx'00D4$_H$	35$_H$ / 53$_D$
CAPCOM Register 22	CC2_CC22IC	xx'00D8$_H$	36$_H$ / 54$_D$
CAPCOM Register 23	CC2_CC23IC	xx'00DC$_H$	37$_H$ / 55$_D$
CAPCOM Register 24	CC2_CC24IC	xx'00E0$_H$	38$_H$ / 56$_D$
CAPCOM Register 25	CC2_CC25IC	xx'00E4$_H$	39$_H$ / 57$_D$
CAPCOM Register 26	CC2_CC26IC	xx'00E8$_H$	3A$_H$ / 58$_D$
CAPCOM Register 27	CC2_CC27IC	xx'00EC$_H$	3B$_H$ / 59$_D$
CAPCOM Register 28	CC2_CC28IC	xx'00F0$_H$	3C$_H$ / 60$_D$

Table 4 XC164S Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM6 Timer T12	CCU6_T12IC	xx'0134$_H$	4D$_H$ / 77$_D$
CAPCOM6 Timer T13	CCU6_T13IC	xx'0138$_H$	4E$_H$ / 78$_D$
CAPCOM6 Emergency	CCU6_EIC	xx'013C$_H$	4F$_H$ / 79$_D$
CAPCOM6	CCU6_IC	xx'0140$_H$	50$_H$ / 80$_D$
SSC1 Transmit	SSC1_TIC	xx'0144$_H$	51$_H$ / 81$_D$
SSC1 Receive	SSC1_RIC	xx'0148$_H$	52$_H$ / 82$_D$
SSC1 Error	SSC1_EIC	xx'014C$_H$	53$_H$ / 83$_D$
Unassigned node	–	xx'0150$_H$	54$_H$ / 84$_D$
Unassigned node	–	xx'0154$_H$	55$_H$ / 85$_D$
Unassigned node	–	xx'0158$_H$	56$_H$ / 86$_D$
Unassigned node	–	xx'015C$_H$	57$_H$ / 87$_D$
Unassigned node	–	xx'0164$_H$	59$_H$ / 89$_D$
Unassigned node	–	xx'0168$_H$	5A$_H$ / 90$_D$
Unassigned node	–	xx'016C$_H$	5B$_H$ / 91$_D$
Unassigned node	–	xx'0170$_H$	5C$_H$ / 92$_D$
Unassigned node	–	xx'0174$_H$	5D$_H$ / 93$_D$
Unassigned node	–	xx'0100$_H$	40$_H$ / 64$_D$
Unassigned node	–	xx'0104$_H$	41$_H$ / 65$_D$
Unassigned node	–	xx'012C$_H$	4B$_H$ / 75$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'0160$_H$	58$_H$ / 88$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

3.5 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system provides a broad range of debug and emulation features built into the XC164S. The user software running on the XC164S can thus be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface, consisting of the IEEE-1149-conforming JTAG port and a break interface. The debugger controls the OCDS via a set of dedicated registers accessible via the JTAG interface. Additionally, the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported as well as the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU-halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing data can be obtained via the JTAG interface or via the external bus interface for increased performance.

The debug interface uses a set of 6 interface signals (4 JTAG lines, 2 break lines) to communicate with external circuitry. These interface signals are realized as alternate functions on Port 3 pins.

Complete system emulation is supported by the New Emulation Technology (NET) interface.

3.6 Capture/Compare Units (CAPCOM1/2)

The CAPCOM units support generation and control of timing sequences on up to 32 channels with a maximum resolution of 1 system clock cycle (8 cycles in staggered mode). The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for each capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Both of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or

3.8 General Purpose Timer Unit (GPT12E)

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer over-flow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

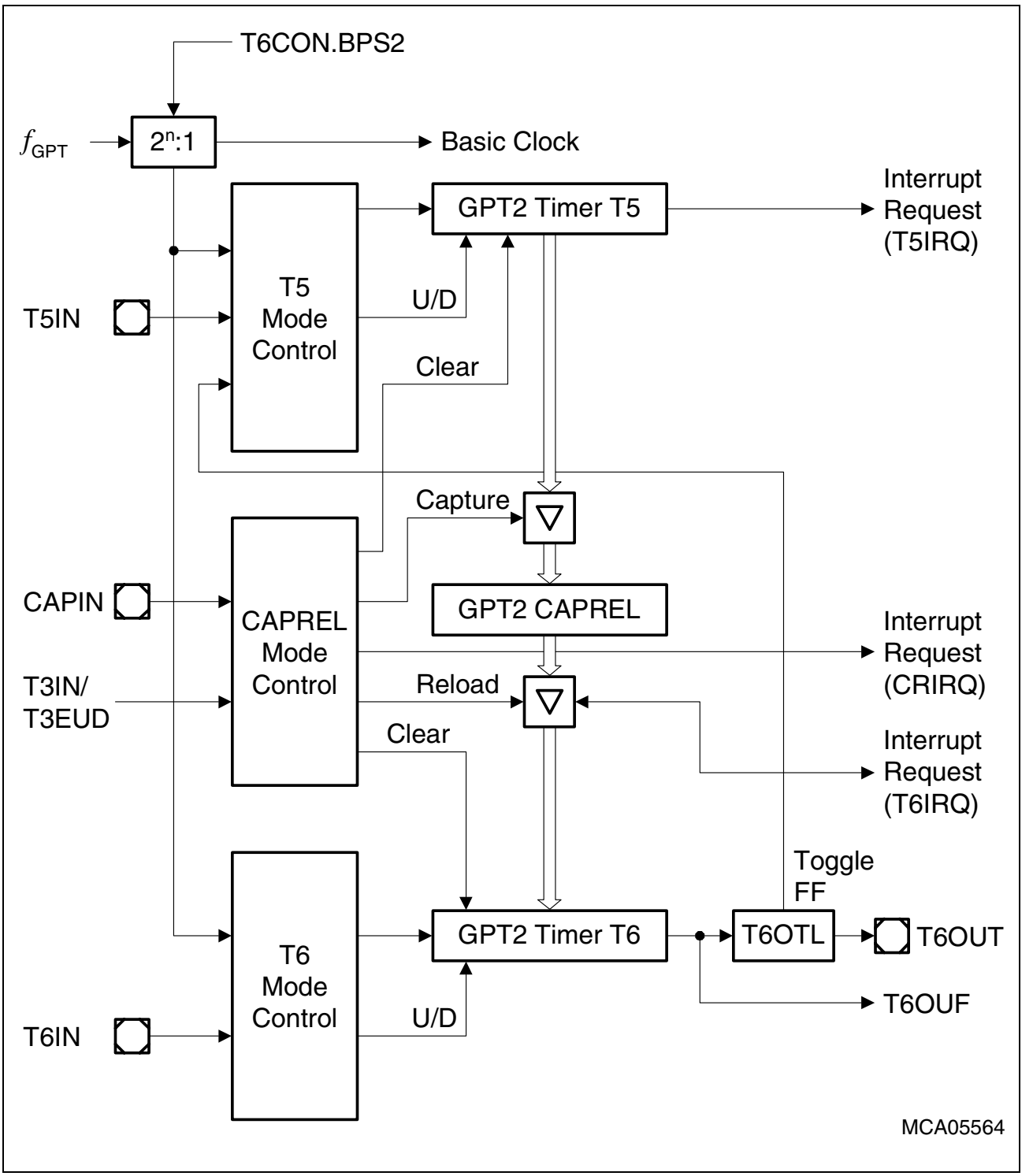

Figure 8 Block Diagram of GPT2

The RTC module can be used for different purposes:

- System clock to determine the current time and date,
  optionally during idle mode, sleep mode, and power down mode.
- Cyclic time based interrupt, to provide a system time tick independent of CPU frequency and other resources, e.g. to wake up regularly from idle mode.
- 48-bit timer for long term measurements (maximum timespan is >> 100 years).
- Alarm interrupt for wake-up on a defined time.

3.12 High Speed Synchronous Serial Channels (SSC0/SSC1)

The High Speed Synchronous Serial Channels SSC0/SSC1 support full-duplex and half-duplex synchronous communication. It may be configured so it interfaces with serially linked peripheral components, full SPI functionality is supported.

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling three separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 … 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit error and receive error supervise the correct handling of the data buffer. Phase error and baudrate error detect incorrect serial data.

Summary of Features

- Master or Slave mode operation
- Full-duplex or Half-duplex transfers
- Baudrate generation from 20 Mbit/s to 305.18 bit/s (@ 40 MHz)
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB-first or MSB-first
  - Programmable clock polarity: idle low or idle high
  - Programmable clock/data phase: data shift with leading or trailing clock edge
- Loop back option available for testing purposes
- Interrupt generation on transmitter buffer empty condition, receive buffer full condition, error condition (receive, phase, baudrate, transmit error)
- Three pin interface with flexible SSC pin configuration

Table 7 Summary of the XC164S's Parallel Ports

Port	Control	Alternate Functions
PORT0	Pad drivers	Address/Data lines or data lines[1)]
PORT1	Pad drivers	Address lines[2)]
		Capture inputs or compare outputs, Serial interface lines, Fast external interrupt inputs
Port 3	Pad drivers, Open drain, Input threshold	Timer control signals, serial interface lines, Optional bus control signal $\overline{BHE}$/$\overline{WRH}$, System clock output CLKOUT (or FOUT), Debug interface lines
Port 4	Pad drivers, Open drain, Input threshold	Segment address lines[3)]
		Optional chip select signals
Port 5	–	Analog input channels to the A/D converter, Timer control signals
Port 9	Pad drivers, Open drain, Input threshold	Capture inputs or compare outputs
Port 20	Pad drivers, Open drain	Bus control signals $\overline{RD}$, $\overline{WR}$/$\overline{WRL}$, ALE, External access enable pin $\overline{EA}$, Reset indication output $\overline{RSTOUT}$

1) For multiplexed bus cycles.

2) For demultiplexed bus cycles.

3) For more than 64 Kbytes of external resources.

Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4

4.4.2 On-chip Flash Operation

The XC164S's Flash module delivers data within a fixed access time (see **Table 17**).

Accesses to the Flash module are controlled by the PMI and take 1+WS clock cycles, where WS is the number of Flash access waitstates selected via bitfield WSFLASH in register IMBCTRL. The resulting duration of the access phase must cover the access time t_{ACC} of the Flash array. Therefore, the required Flash waitstates depend on the available speed grade as well as on the actual system frequency.

Note: The Flash access waitstates only affect non-sequential accesses. Due to prefetching mechanisms, the performance for sequential accesses (depending on the software structure) is only partially influenced by waitstates.
In typical applications, eliminating one waitstate increases the average performance by 5% … 15%.

Table 17 Flash Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit
			Min.	Typ.	Max.	
Flash module access time	t_{ACC}	CC	–	–	50	ns
Programming time per 128-byte block	t_{PR}	CC	–	2[1)]	5	ms
Erase time per sector	t_{ER}	CC	–	200[1)]	500	ms

1) Programming and erase time depends on the system frequency. Typical values are valid for 40 MHz.

Example: For an operating frequency of 40 MHz (clock cycle = 25 ns), devices can be operated with 1 waitstate: ((1+1) × 25 ns) ≥ 50 ns.

Table 18 indicates the interrelation of waitstates and system frequency.

Table 18 Flash Access Waitstates

Required Waitstates	Frequency Range
0 WS (WSFLASH = 00_B)	$f_{CPU} \leq 20$ MHz
1 WS (WSFLASH = 01_B)	$f_{CPU} \leq 40$ MHz

Note: The maximum achievable system frequency is limited by the properties of the respective derivative, i.e. 40 MHz (or 20 MHz for XC164S-xxF20F devices).

4.4.5 External Bus Timing

Table 20 CLKOUT Reference Signal

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
CLKOUT cycle time	tc_5	CC	40/30/25[1]		ns
CLKOUT high time	tc_6	CC	8	–	ns
CLKOUT low time	tc_7	CC	6	–	ns
CLKOUT rise time	tc_8	CC	–	4	ns
CLKOUT fall time	tc_9	CC	–	4	ns

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{CPU} = 25/33/40 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

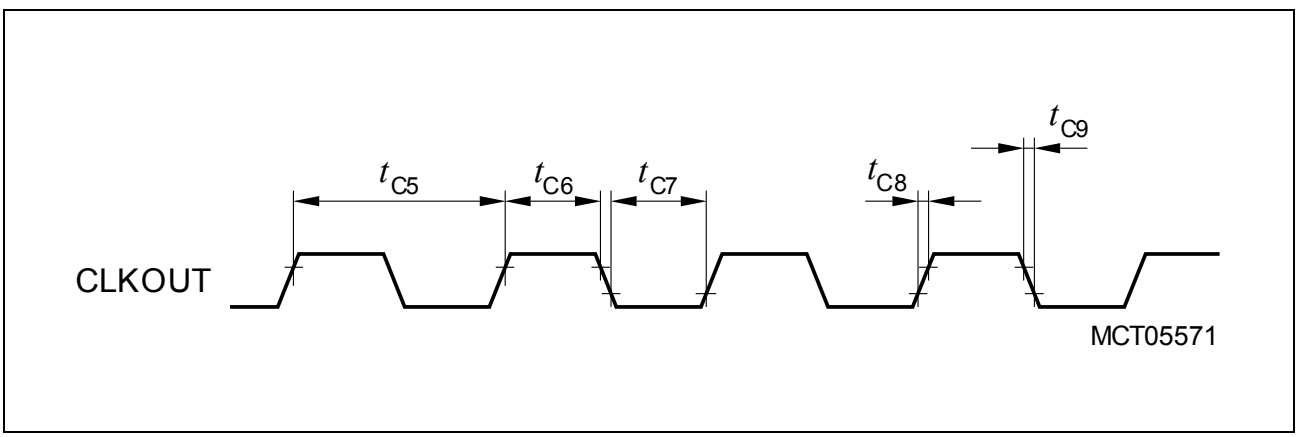

Figure 19 CLKOUT Signal Timing

Table 22 External Bus Cycle Timing (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
Output valid delay for: RD, WR(L/H)	tc_{10}	CC	1	13	ns
Output valid delay for: BHE, ALE	tc_{11}	CC	-1	7	ns
Output valid delay for: A23 … A16, A15 … A0 (on PORT1)	tc_{12}	CC	1	16	ns
Output valid delay for: A15 … A0 (on PORT0)	tc_{13}	CC	3	16	ns
Output valid delay for: CS	tc_{14}	CC	1	14	ns
Output valid delay for: D15 … D0 (write data, MUX-mode)	tc_{15}	CC	3	17	ns
Output valid delay for: D15 … D0 (write data, DEMUX-mode)	tc_{16}	CC	3	17	ns
Output hold time for: RD, WR(L/H)	tc_{20}	CC	-3	3	ns
Output hold time for: BHE, ALE	tc_{21}	CC	0	8	ns
Output hold time for: A23 … A16, A15 … A0 (on PORT0)	tc_{23}	CC	1	13	ns
Output hold time for: CS	tc_{24}	CC	-3	3	ns
Output hold time for: D15 … D0 (write data)	tc_{25}	CC	1	13	ns
Input setup time for: D15 … D0 (read data)	tc_{30}	SR	24	–	ns
Input hold time D15 … D0 (read data)[1)]	tc_{31}	SR	-5	–	ns

1) Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of RD. Therefore address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can be removed after the rising edge of RD.

Note: The shaded parameters have been verified by characterization. They are not subject to production test.

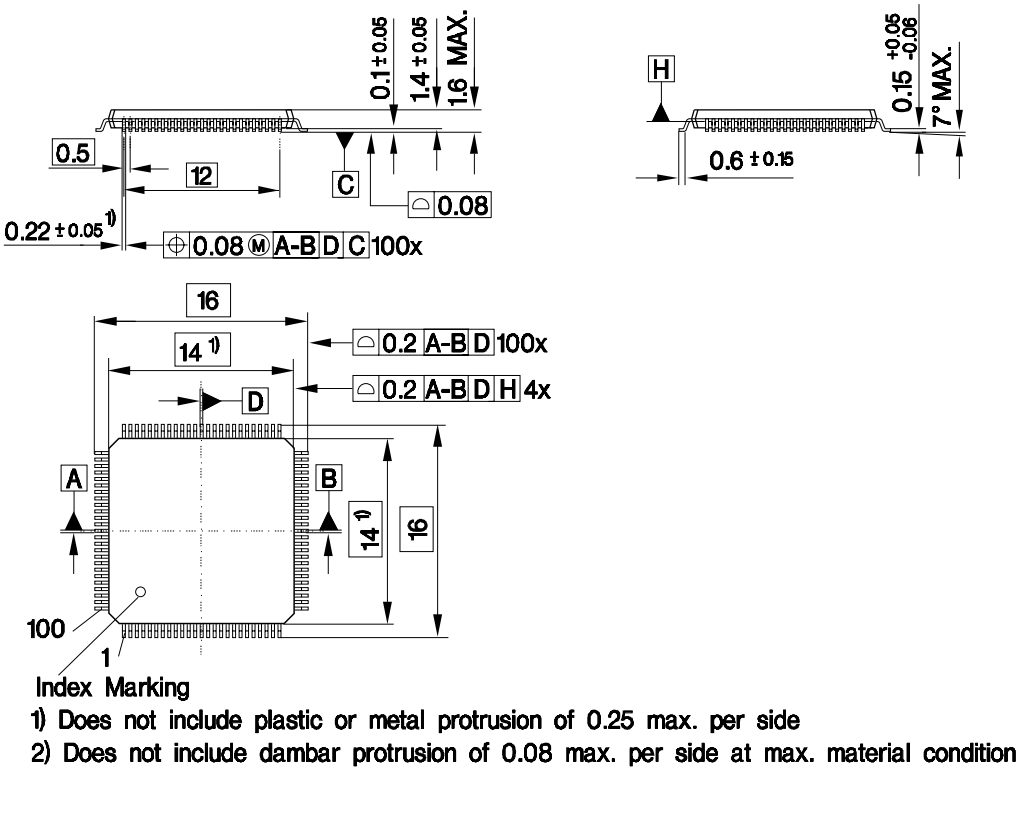

Figure 23 P-TQFP-100-16 (Plastic Thin Quad Flat Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**. Dimensions in mm