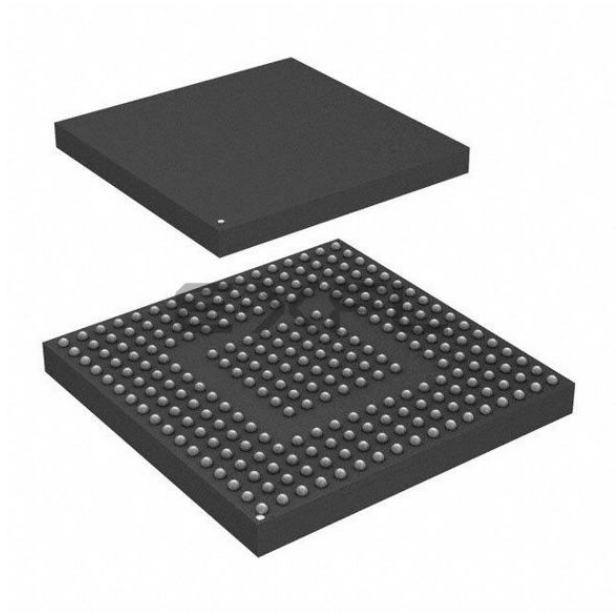

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | e200z4, e200z7 (2) |
| Core Size | 32-Bit Tri-Core |
| Speed | 180MHz, 240MHz |
| Connectivity | CANbus, FlexIO, I²C, LINbus, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | - |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 1.5M x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.19V ~ 5.5V |
| Data Converters | A/D 16x12b SAR, 4x12 Sigma; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 257-LFBGA |
| Supplier Device Package | 257-LFBGA (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32r274kbk2mmm |

    - 16 MHz Internal oscillator (IRCOSC)
    - Dual system PLL with one frequency modulated phase-locked loop (FMPLL)
    - Low-jitter PLL to ΣΔ-ADC and DAC clock generation
- Functional Safety
    - Enables up to ASIL-D applications
    - End to end ECC ensuring full protection of all data accesses throughout the system, from each of the systems masters through the crossbar and into the memories and peripherals
    - FCCU for fault collection and fault handling
    - MEMU for memory error management
    - Safe eDMA controller
    - User selectable Memory BIST (MBIST) can be enabled to run out of various reset conditions or during runtime
    - Self-Test Control Unit (STCU2)
    - Error Injection Module (EIM)
    - On-chip voltage monitoring
    - Clock Monitor Unit (CMU) to support monitoring of critical clocks
- Security
    - Cryptographic Security Engine (CSE2) enabling advanced security management
    - Supports censorship and life-cycle management via Password and Device Security (PASS) module
    - Diary control for tamper detection (TDM)
- Support Modules
    - Global Interrupt controller (INTC) capable of routing interrupts to any CPU
    - Semaphore unit to manage access to shared resources
    - Two CRC computation units with four polynomials
    - 32-channel eDMA controller with multiple transfer request sources using DMAMUX
    - Boot Assist Module (BAM) supports internal flash programming via a serial link (LIN / CAN)
- Timers
    - Two Periodic Interval Timers (PIT) with 32-bit counter resolution
    - Three System Timer Module (STM)
    - Three Software Watchdog Timers (SWT)
    - Two eTimer modules with 6 channels each
    - One FlexPWM module for 12 PWM signals
- Communication Interfaces
    - Two Serial Peripheral interface (SPI) module
    - Two inter-IC communication interface (I2C) modules
    - One LINFlexD module
    - One dual-channel FlexRay module with 128 message buffers

## Table 6. Absolute maximum ratings (continued)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{SS\_HV\_ADC}$ | 3.3 V ADC supply ground | — | –0.1 | 0.1 | V |
| $TV_{DD}$ | Supply ramp rate[6] | — | 0.00005 | 0.1 | V/µs |
| $V_{IN\_XOSC}$ | Voltage on XOSC pins with respect to ground | — | -0.3 | 1.47 | V |
| $V_{INA}$ | Voltage on SAR ADC analog pin with respect to ground ($V_{SS\_HV\_ADCREFx}$) | — | –0.3 | 6.0 | V |
| $V_{INA\_SD}$ | Voltage on Sigma-Delta ADC analog pin with respect to ground[7] | Powered up [8] | -0.3 | $V_{DD\_HV\_RAW}$ + 0.3 | V |
| | | Powered down [9] | -0.3 | 1.47 | |
| $V_{IN}$ | Voltage on any digital pin with respect to ground ($V_{SS\_HV\_IOx}$) | Relative to $V_{DD\_HV\_IOx}$ | –0.3 | $V_{DD\_HV\_IOx}$ + 0.3 [10] | V |
| $V_{DD\_LV\_DPHY}$ | MIPICSI2 DPHY voltage supply[3, 4, 5] | — | –0.3 | 1.5 | V |
| $V_{SS\_LV\_DPHY}$ | MIPICSI2 DPHY supply ground[3, 4, 5] | — | –0.3 | 0.3 | V |
| $I_{INJPAD}$[11] | Injected input current on any pin during overload condition[12] | — | –10 | 10[13] | mA |
| $I_{INJSUM}$ | Absolute sum of all injected input currents during overload condition | — | –50 | 50 | mA |
| $T_{STG}$ | Storage temperature | — | –55 | 150 | °C |

1. 5.3 V for 10 hours cumulative over lifetime of device; 3.3 V +10% for time remaining.
2. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
3. 1.45 V to 1.5 V allowed for 60 seconds cumulative time at maximum $T_J$ = 150°C; remaining time as defined in note 5 and note 6.
4. 1.375 V to 1.45 V allowed for 10 hours cumulative time at maximum $T_J$ = 150°C; remaining time as defined in note 6.
5. 1.32 V to 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum $T_J$=150°C.
6. $TV_{DD}$ is relevant for all external supplies.
7. ADC inputs include an overvoltage detect function that detects any voltage higher than 1.2 V with respect to ground on either ADC input and open circuit (disconnect) the input in order to prevent damage to the ADC internal circuitry. The ADC input remains disconnected until the inputs return to the normal operating range.
8. SDADC is powered up and overvoltage protection is ON.
9. SDADC is powered up and overvoltage protection is OFF.
10. Only when $V_{DD\_HV\_IOx}$ < 3.63 V.
11. The maximum value limits of injection current and input voltage both must be followed together for proper device operation.
12. No input current injection circuitry on AFE pins.
13. The maximum value of 10 mA applies to pulse injection only. DC current injection is limited to a maximum of 5 mA.

## Table 7. Device operating conditions (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| $T_J$[11] | Junction temperature | — | –40 | — | 150 | °C |
| $F_{XTAL}$ | XOSC Crystal Frequency[13] | — | — | 40 | — | MHz |
| **AFE Bypass Modes Only** | | | | | | |
| **Single-Ended External Clock**[14] | | | | | | |
| $EXTAL_{clk}$ | EXTAL external clock frequency | | | 40 | | MHz |
| $V_{inxoscjit}$ | EXTAL external clock Cycle to Cycle Jitter (RMS) | — | — | — | 2.5[15] | ps |
| $V_{inxoscclkvil}$ | EXTAL external clock input low voltage | — | 0 | — | 0.4 | V |
| $V_{inxoscclkvih}$ | EXTAL external clock input high voltage | — | 1 | — | 1.23 | V |
| $t_r/t_f$ | Rise/fall time of EXTAL external clock input | | | | 1 | ns |
| $t_{dc}$ | Duty Cycle of EXTAL external clock input | | 47 | 50 | 53 | % |
| **Differential LVDS External Clock** | | | | | | |
| $LVDS_{clk}$ | LVDS external clock frequency | | | 40 | | MHz |
| $LVDSV_{inxoscclk}$ | LVDS external clock input voltage | | 0 | | 1.36 | V |
| $LVDSV_{inxoscclk(p-p)}$ | LVDS external clock input voltage (peak-peak) | Voltage driven, AC coupled Differential | 0.45 | 0.70 | 1.12 | V |
| $LVDSI_{inxoscclk}$ | LVDS external clock input current | Current driven, DC coupled. | 3.0 | 3.5 | 4.0 | mA |
| $LVDSV_{inxoscjit}$ | LVDS external clock Jitter (RMS) [15] | | | | 2.5 | ps |
| $t_r/t_f$ | Rise/fall time of LVDS external clock input | 20% - 80% | | | 1.5 | ns |
| $t_{dcLVDS}$ | Duty Cycle of LVDS external clock input | | 47 | 50 | 53 | % |

1. Full functionality cannot be guaranteed when voltages are out of the recommended operating conditions.
2. Min voltage takes into account the LVD variation.
3. Max voltage takes into account HVD variation.
4. Aurora supply must connect to core supply voltage at board level.
5. The ground connection for the $V_{DD\_HV\_FLA}$ is shared with $V_{SS}$.
6. Supply range does not take into account HVD levels. Full range can be achieved after power-up, if HVD is disabled. See Voltage regulator electrical characteristics section for details.
7. Around common mode voltage of 0.7 V. Input voltage cannot exceed 1.4 V prior to AFE start-up completion (VREF and VREGs on and LVDs cleared).
8. SDADC input voltage full scale is 1.2 Vpp
9. On channels shared between ADC0 and 1, $V_{DD\_HV\_ADCREFx}$ is the lower of $V_{DD\_HV\_ADCREF0/1}$.
10. $V_{DD\_LV\_DPHY}$ supply should be shorted to core supply voltage VDD on board. Refer to AN5251. Contact your NXP sales representative for details.

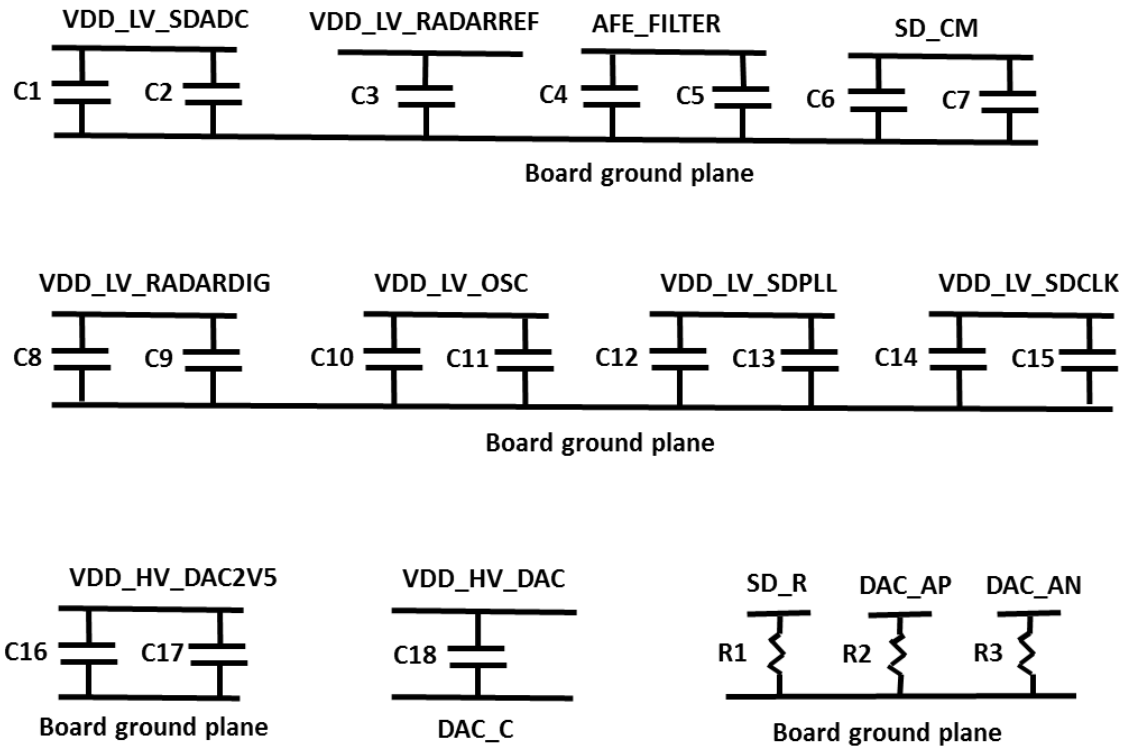


**Figure 3. Radar AFE External Components Configuration**

## Table 11. Radar AFE External Components

| Component | Component Value | Tolerance | Placement Priority of larger cap. [1] | Placement Priority of smaller cap[1] | Special notes |
|---|---|---|---|---|---|
| C1 | 0.47 µF | ±35% | 3 | — | — |
| C2 | 0.1 µF | ±35% | — | 1 | — |
| C3 | 1.0 µF | ±35% | 7 | — | — |
| C4 | 1.0 µF | ±35% | 2 | — | — |
| C5 | 0.1 µF | ±35% | — | 4 | — |
| C6 | 1.0 µF | ±35% | 8 | — | — |
| C7 | 0.1 µF | ±35% | — | 6 | — |
| C8 | 1.0 µF | ±35% | 6 | — | — |
| C9 | 0.1 µF | ±35% | — | 5 | — |
| C10 | 1.0 µF | ±35% | 4 | — | — |
| C11 | 0.1 µF | ±35% | — | 2 | — |
| C12 | 1.0 µF | ±35% | 5 | — | — |
| C13 | 0.1 µF | ±35% | — | 3 | — |
| C14 | 1.0 µF | ±35% | 10 | — | — |
| C15 | 0.1 µF | ±35% | — | 8 | — |
| C16 | 1.0 µF | ±35% | 9 | — | — |
| C17 | 0.1µF | ±35% | — | 7 | — |

*Table continues on the next page...*

**Table 11. Radar AFE External Components (continued)**

| Component | Component Value | Tolerance | Placement Priority of larger cap. [1] | Placement Priority of smaller cap[1] | Special notes |
|---|---|---|---|---|---|
| C18 | 10 µF | — | 1 | — | X7R type |
| C19 | 220 nF | — | — | — | Sigma Delta ADC input capacitor. See Figure 9 |
| C20 | 220 nF | — | — | — | Sigma Delta ADC input capacitor. See Figure 9 |
| R1 | 40.2 kΩ | ±0.1% | — | — | tempco = 25ppm/C |
| R2 | 300 Ω | — | — | — | DAC RI See Table 27 |
| R3 | 300 Ω | — | — | — | DAC RI See Table 27 |
| Crystal | 40MHz | — | — | — | Connected between XOSC_EXTAL/ XOSC_XTAL, ESR ≤ 30Ω |

1. All Radar AFE external bypass capacitors should be placed as close as possible to the associated package pin. As shown in Radar AFE External Components Configuration figure, most pins have two values of bypass capacitor. Greater than 0.1 µF is referred to as the larger cap. 0.1 µF is referred to as the smaller cap.

## 4.5 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

## 4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × ($n$ + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

**NOTE**

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table 12. ESD ratings**

| No. | Symbol | Parameter | Conditions[1] | Class | Max value[2] | Unit |
|---|---|---|---|---|---|---|
| 1 | $V_{ESD(HBM)}$ | Electrostatic discharge (Human Body Model) | $T_A$ = 25 °C | H1C | 2000 | V |

*Table continues on the next page...*

1. Measured when pad = 0 V
2. Measured when pad = $V_{DD\_HV\_IO}$
3. Measured when pad is sourcing 2 mA
4. Measured when pad is sinking 2 mA
5. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

### 5.1.1 RGMII pad DC electrical characteristics

**Table 14. RGMII pad DC electrical specifications**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Vih | CMOS Input Buffer High Voltage | 0.65 x $V_{DD\_HV\_IO}$ | $V_{DD\_HV\_IO}$ + 0.3 | V |
| Vil | CMOS Input Buffer Low Voltage | -0.3 | 0.35 x $V_{DD\_HV\_IO}$ | V |
| Pull_Ioh | Weak Pullup Current[1] | 10 | 55 | µA |
| Pull_Iol | Weak Pulldown Current[2] | 10 | 55 | µA |
| Iinact_d | Digital Pad Input Leakage Current (weak pull inactive) | -2.5 | 2.5 | µA |
| Voh | Output High Voltage[3] | 0.8 x $V_{DD\_HV\_IO}$ | — | V |
| Vol | Output Low Voltage[4] | — | 0.2 * $V_{DD\_HV\_IO}$ | V |
| Ioh_f | Full drive Ioh[5] | 8 | 26 | mA |
| Iol_f | Full drive Iol[6] | 8 | 24 | mA |

1. Measured when pad = 0 V
2. Measured when pad = $V_{DD\_HV\_IO}$
3. Measured when pad is sourcing 2 mA
4. Measured when pad is sinking 2 mA
5. Ioh_f value is measured with 0.8*VDDE applied to the pad.
6. Iol_f is measured when 0.2*VDDE is applied to the pad.

## 5.2 I/O pad AC specifications

AC Parameters are specified over the full operating junction temperature range of -40°C to +150°C and for the full operating range of the $V_{DD\_HV\_IO}$ supply defined in Table 7.

**Table 15. Functional Pad electrical characteristics**

| Symbol | Prop. Delay (ns)[1] L>H/H>L | | Rise/Fall Edge (ns)[2] | | Drive Load (pF) | SIUL2_MSCR[SRC] |
|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | MSB,LSB |
| pad_sr_hv (output) | 2.5/2.5 | 8.25/7.5 | 0.7/0.6 | 3/3 | 50 | 11 |
| | 6.4/5 | 19.5/19.5 | 2.5/2.0 | 12/12 | 200 | |
| | 2.2/2.5 | 8/8 | 0.4/0.3 | 3.5/3.5 | 25 | 10 |
| | 2.9/3.5 | 12.5/11 | 1.0/0.8 | 6.5/6.5 | 50 | |
| | 11/8 | 35/31 | 6.5/3.0 | 25/21 | 200 | |

*Table continues on the next page...*

# 6 Peripheral operating requirements and behaviours

## 6.1 Clocks and PLL Specifications

### 6.1.1 40 MHz Oscillator (XOSC) electrical characteristics

The device provides an oscillator/resonator driver.

**NOTE**

XTAL/EXTAL must not be directly used to drive external circuits.

**Table 19. XOSC electrical characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $XOSC_{fout}$ | Oscillator frequency | | | 40 | | MHz |
| $t_{stab}$ | Oscillator start-up time | | | | 2 | ms |
| $t_{jitcc}$ | Cycle to cycle jitter (peak – peak) | | | | 2.5[1] | ps |
| | Output Duty Cycle | | 45 | 50 | 55 | % |
| Cin | Input Capacitance [2] | Extal and Xtal each | 3.0 | 4.0 | 5.0 | pF |
| $R_{inLVDS}$ | LVDS bypass mode input termination[3] | Between Extal and Xtal | 75 | 100 | 125 | ohm |
| $V_{CMLVDS}$ | LVDS Common Mode Voltage | Vdda/2 | 0.60 | 0.70 | 0.80 | V |

1. The number is 3.5 ps when SD-ADC and/or DAC is not used in the device.
2. When using a 40 MHz crystal, the recommended load capacitance is 8 pF. Need quiet ground connection on the board and external crystal/load capacitor placement as close to the Extal and Xtal pins as possible to allow good jitter performance.
3. The termination resistance is only active when the AFE is powered (VDD_HV_RAW, VDD_HV_DAC and the AFE regulators are powered up) and the XOSC is powered down (default case once device is out of reset) or the XOSC is configured in differential bypass mode.

### 6.1.2 FMPLL electrical characteristics

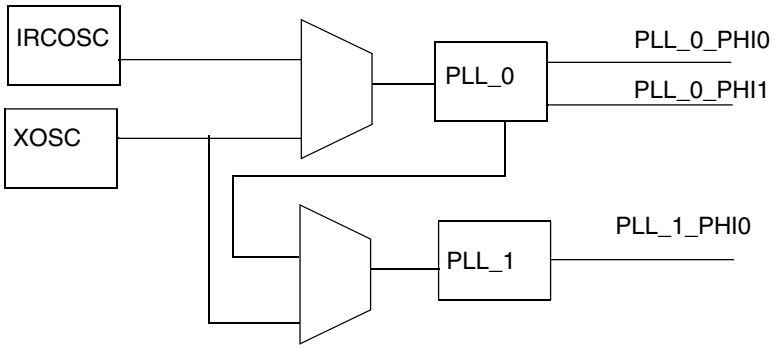


**Figure 6. PLL integration**

## Table 20. PLL0 electrical characteristics

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL0IN}$ | PLL0 input clock[2, 3] | — | 14 | — | 44 | MHz |
| $\Delta_{PLL0IN}$ | PLL0 input clock duty cycle[2] | — | 40 | — | 60 | % |
| $f_{PLL0VCO}$ | PLL0 VCO frequency | — | 600 | — | 1250 | MHz |
| $f_{PLL0PHI0}$ | PLL0 output clock PHI0 | — | 4.76 | — | 625[4] | MHz |
| $f_{PLL0PHI1}$ | PLL0 output clock PHI1 | — | 20 | — | 156 | MHz |
| $t_{PLL0LOCK}$ | PLL0 lock time | — | — | — | 100 | µs |
| $\Delta_{PLL0LTJ}$ | PLL0 long term jitter $f_{PLL0IN}$ = 8 MHz (resonator)[5] | $f_{PLL0PHI0}$ = 40 MHz, 1 µs | | | ± 1 | ns |
| | | $f_{PLL0PHI0}$ = 40 MHz, 13 µs | | | ± 1 | ns |
| $I_{PLL0}$ | PLL0 consumption | | — | — | 5 | mA |

1. $V_{DD\_LV\_PLL0}$ =1.25 V ± 5%, $T_J$ = -40 / 150 °C unless otherwise specified.
2. PLL0IN clock retrieved directly from either IRCOSC or external XOSC clock.
3. $f_{PLL0IN}$ frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure the reference clock to the PLL analog loop is in the range 8 MHz-20 MHz
4. The maximum clock outputs are limited by the design clock frequency requirements as per recommended operating conditions.
5. $V_{DD\_LV\_PLL0}$ noise due to application in the range $V_{DD\_LV\_PLL0}$ = 1.25 V±5%, with frequency below PLL bandwidth (40 KHz) will be filtered.

## Table 21. FMPLL1 electrical characteristics

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL1IN}$ | PLL1 input clock[2] | — | 38 | — | 78 | MHz |
| $\Delta_{PLL1IN}$ | PLL1 input clock duty cycle[2] | — | 35 | — | 65 | % |
| $f_{PLL1VCO}$ | PLL1 VCO frequency | — | 600 | — | 1250 | MHz |
| $f_{PLL1PHI0}$ | PLL1 output clock PHI0 | — | 4.76 | — | 625 | MHz |
| $t_{PLL1LOCK}$ | PLL1 lock time | — | — | — | 100 | µs |
| $f_{PLL1MOD}$ | PLL1 modulation frequency | — | — | — | 250 | kHz |
| $\lvert\delta_{PLL1MOD}\rvert$ | PLL1 modulation depth (when enabled) | Center spread | 0.25 | — | 2 | % |
| | | Down spread | 0.5 | — | 4 | % |
| $I_{PLL1}$ | PLL1 consumption | | — | — | 6 | mA |

1. $V_{DD\_LV\_PLL0}$ = 1.25 V ± 5%, $T_J$ = -40 / 150°C unless otherwise specified.
2. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock.

## Table 25. ADC conversion characteristics (continued)

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $TUE_{IS1WINJ}$ | Total unadjusted error for IS1WINJ | | –6 | — | 6 | LSB |
| $TUE_{IS1WWINJ}$ | Total unadjusted error for IS1WWINJ | | –6 | — | 6 | LSB |
| IS1WINJ (pad going to one ADC) | (single ADC channel) | | | | | |
| | Max leakage | 150 °C | — | — | 250 | nA |
| | Max positive/negative injection | | –3 | — | 3[8] | mA |
| IS1WWINJ (pad going to two ADCs) | (double ADC channel) | | | | | |
| | Max leakage | 150 °C | — | — | 300 | nA |
| | Max positive/negative injection [7] | \|Vref_ad0 - Vref_ad1\| < 150 mV | –3.6 | — | 3.6 | mA |
| SNR | Signal-to-noise ratio | 3.3 V reference voltage | 67 | — | — | dB |
| THD | Total harmonic distortion | @ 50 KHz | 65 | — | — | dB |
| SINAD | Signal-to-noise and distortion | Fin < 50 KHz | 6.02 x ENOB + 1.76 | | | dB |
| ENOB | Effective number of bits | Fin < 50 KHz | 10.5 | — | — | bits |

1. $V_{DD\_HV\_ADC}$ = 3.3 V -5%,+10%, $T_J$ = –40 to +150°C, unless otherwise specified and analog input voltage from $V_{AGND}$ to $V_{DD\_HV\_ADCREFx}$.
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. During the sample time the input capacitance $C_S$ can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_{sample}$. After the end of the sample time $t_{sample}$, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock $t_{sample}$ depend on programming.
4. This parameter does not include the sample time $t_{sample}$, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. SeeInput equivalent circuit figure.
6. No missing codes.
7. ADC specifications are met only if injection is within these specified limits
8. Max injection current for all ADC IOs is ± 10 mA

**NOTE**

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel. Aurora interface along with SAR-ADC would degrade SAR-ADC performance. General Purpose Input (GPI) functionality should not be used on any of the SAR-ADC channels when SARADC is functional.

## 7.2 Sigma Delta ADC electrical characteristics

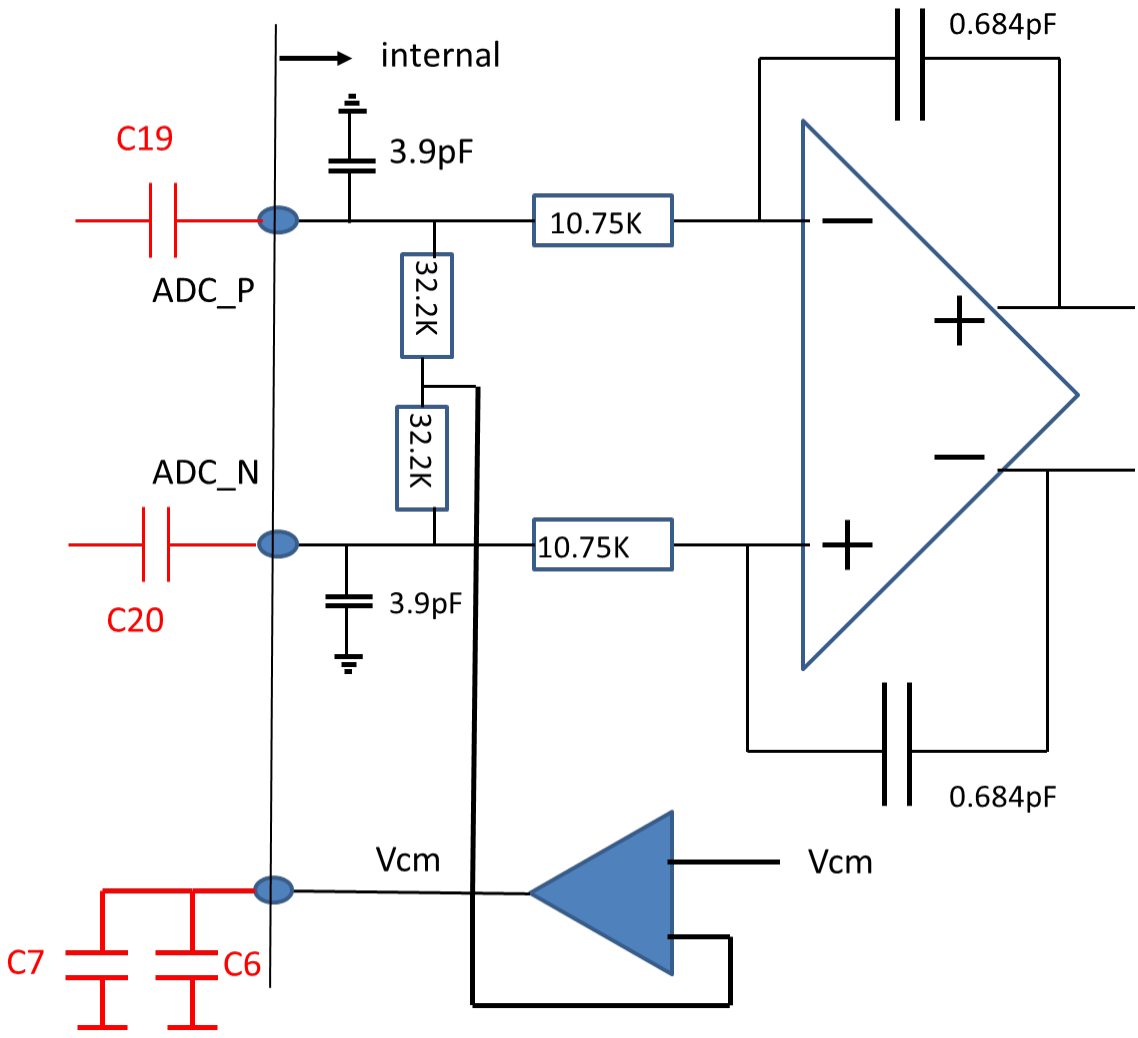


**Figure 9. ADC input equivalent circuit**

**Table 26. Sigma Delta ADC Parameters**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $SPS_{SDA}$ | Sample Rate | After Decimation Filtering | — | 10 | 10 | MS/S |
| $L_{SDA}$ | Latency | @ 10 MS/s, full step input to 50% output. Decimation filter delay not included | — | — | 0.1 | µs |
| $RT_{SDA}$ | Recovery Time | After overload condition | — | — | 0.5 | µs |
| $SNR_{SDA\_MM\_ON}$ [1] | Signal-to-Noise Ratio Mismatch Shaper on | Input Frequency Range and integration bandwidth are from 20 KHz to 5 MHz (using full-bandwidth decimation filter coefficients). Production test frequencies 449 KHz and 4 MHz. Production test amplitude is -6 dBFS = 0.6 Vpp. | 63 | 67 | — | dBFS |

*Table continues on the next page...*

## Table 26. Sigma Delta ADC Parameters (continued)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OEV | Offset Variation | t = 50 ms, T = constant, data averaged in 1 ms increments | -0.07 | — | 0.07 | mV |
| $V_{cm}$ | Common Mode Voltage[2] | SDADC switched on | — | vdda/2 – 30 mV | — | V |
| xtalk | Crosstalk (from any ADC to the other ADCs) | Processing a full scale signal. | — | — | -40 | dB |
| Zin | Input Impedance | Maximum input impedance occurs for input signals at 20 KHz and minimum input impedance occurs at input frequencies greater than 1 MHz[3] | 7.3 | — | 33.5 | kΩ |
| $R_{cm}$ | Resistance from each SDADC input to $V_{cm}$ (see Figure 9) | - | 27.3 | 32.2 | 37.0 | kΩ |
| R_SDADC | Resistance from each SDADC input pin to differential amplifier input (see Figure 9) | - | 9.0 | 10.75 | 12.5 | kΩ |
| C_SDADC | SDADC integrator capacitors (see Figure 9) | - | 0.636 | 0.684 | 0.732 | pF |
| $C_{in}$ parasitic | parasitic input capacitance from ADC input to ground | - | 2.0 | 3.9 | 4.9 | pF |
| DT | Analog Delay Variation | (ADCx to ADCy) | | — | 1 | ns |
| AA | Alias Suppression | ADC input frequency between 315 and 325 MHz | 50 | — | — | dB |
| STFoob | ADC out of band Signal Transfer Function peaking | Out of band Signal Transfer function peaking from 20 MHz to 40 MHz | 0 | 2 | 3 | dB |
| PR | passband ripple | From 20 KHz to 4 MHz (default decimation filter coefficients must be used) | -0.5 | 0.0 | 0.5 | dB |
| OOBA[4] | Out Of Band Attenuation | Default decimation filter coefficients must be used<br>5 MHz<br>6 MHz<br>7 MHz<br>10 MHz<br>15 MHz | <br>-4.5<br>-10<br>-20<br>-40<br>-60 | — | — | dB |

1. Derate specification by 2 dBFS for $T_j$ less than 0°C.
2. vdda is an internally regulated and trimmed 1.45V ± 10mV voltage.
3. The input structure of the ADC is an active RC integrator which has a frequency dependent input impedance as indicated in ADC input equivalent circuit.
4. All attenuation values are relative to 0 dB in the ADC passband.

**Table 34. RMII signal switching specifications (continued)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| RMII8 | RMII_CLK to TXD[1:0], TXEN valid | — | 15 | ns |

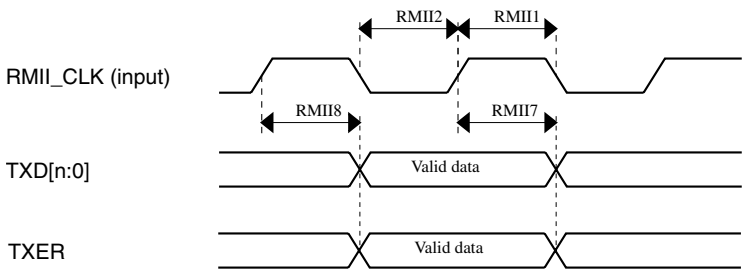


**Figure 12. RMII transmit signal timing diagram**

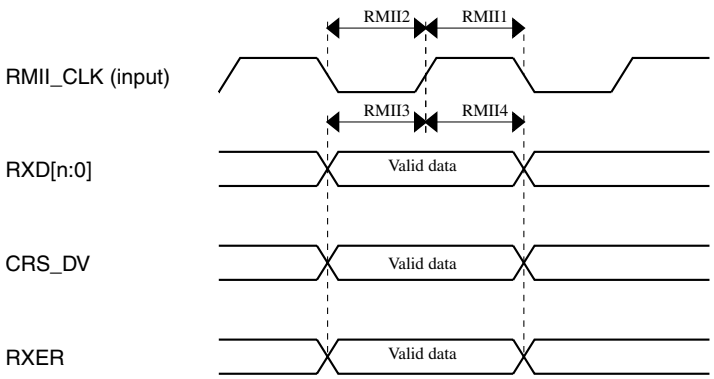


**Figure 13. RMII receive signal timing diagram**

## 9.1.3 RGMII signal switching specifications

The RGMII interface works at 3.3 V compatible levels as mentioned in RGMII pad DC electrical characteristics.

The following timing specs meet the requirements for RGMII style interfaces for a range of transceiver devices.

- Measurements are with input transition of 0.750 ns and output load of 10 pF.

**Table 35. RGMII signal switching specifications**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| — | Input Duty cycle (Clock from external PHY) | 48 | — | 52 | % | |
| Tcyc | Clock cycle duration | 7.2 | 8.0 | 8.8 | ns | 1 |
| TskewT | Data to clock output skew at transmitter | -500 | 0 | 500 | ps | 2 |
| TskewR | Data to clock input skew at receiver | 1 | 1.8 | 2.6 | ns | 2 |

*Table continues on the next page...*

### 9.1.4 MII/RMII Serial Management channel timing (MDC/MDIO)

The MDC/MDIO interface works at 3.3V compatible levels as mentioned in CMOS input (vih/vil/voh/vol/)values in I/O pad DC electrical characteristics .

Ethernet works with maximum frequency of MDC at 2.5 MHz. Output pads configured with SRC=11. MDIO pin must have external pull-up. Measurements are with input transition of 1.0 ns and output load of 50 pF.

**Table 36. Ethernet MDIO timing table**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| MDC00 | MDC clock frequency | — | 2.5 | MHz |
| MDC10 | MDC falling edge to MDIO output invalid (minimum propagation delay) | (-0.8 + (ENET_MSCR[HOLDTIME] +1)*(PBRIDGE_n_CLK period in ns)) | — | ns |
| MDC11 | MDC falling edge to MDIO output valid (maximum propagation delay) | — | (13 + (ENET_MSCR[HOLDTIME] +1)*(PBRIDGE_n_CLK period in ns)) | ns |
| MDC12 | MDIO (input) to MDC rising edge setup | 13 | — | ns |
| MDC13 | MDIO (input) to MDC rising edge hold | 0 | — | ns |
| MDC14 | MDC pulse width high | 40% | 60% | MDC Period |
| MDC15 | MDC pulse width low | 40% | 60% | MDC Period |

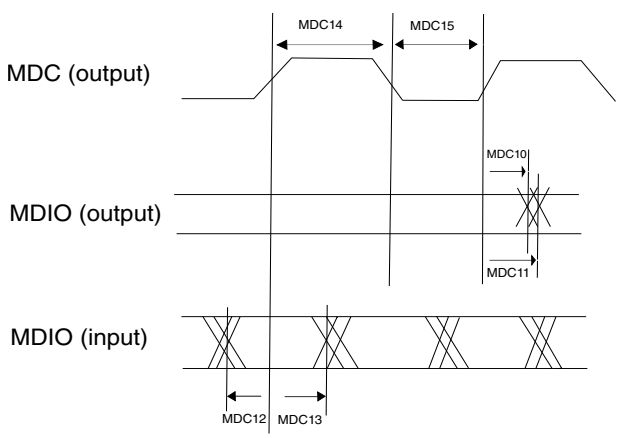


**Figure 16. RMII/MII serial management channel timing diagram**

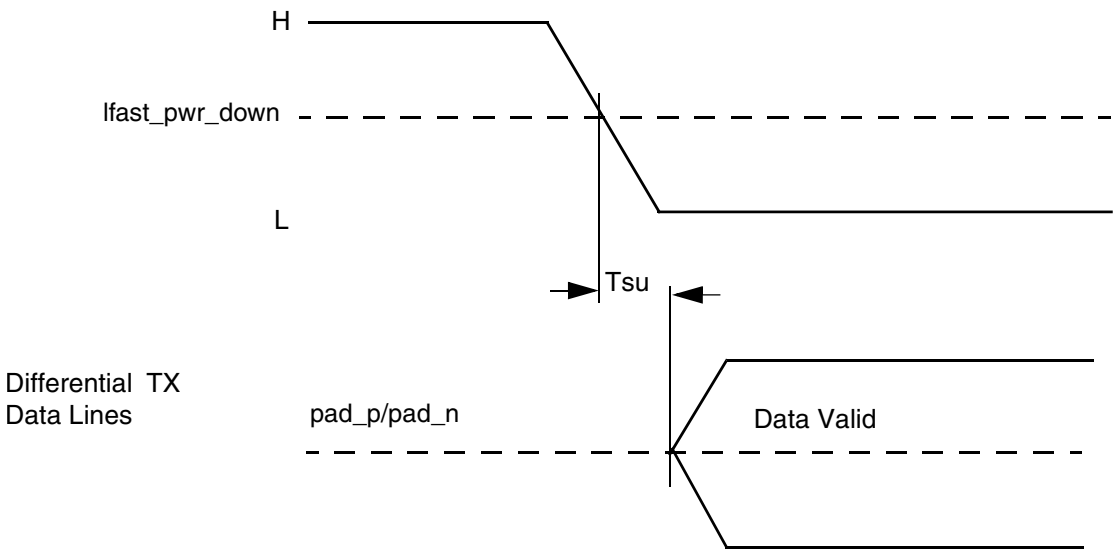


**Figure 22. Power-down exit time**

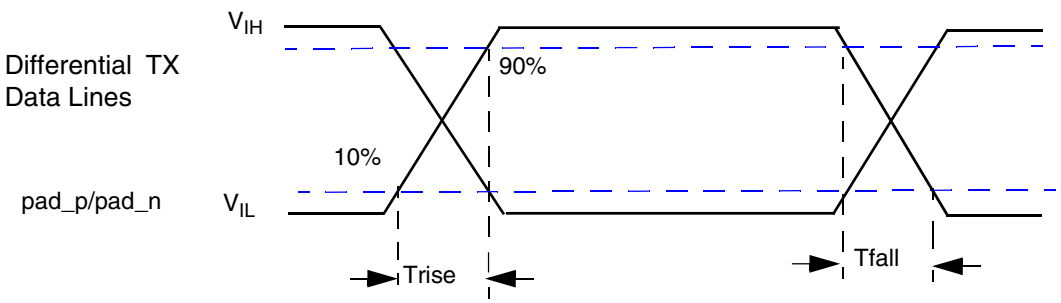


**Figure 23. Rise/fall time**

## 9.3.2 LFAST interface electrical characteristics

**NOTE**

While LFAST is operating and 'Ready' (nex_rdy_b) signal is used by the debugger on PAD_132, the recommended SRE settings are ‘00' and ‘01'. TCK should be used with low frequency (preferably less than 10 MHz).

**Table 42. LFAST electrical characteristics**

| Symbol | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Data Rate | | | | | | |
| DATARATE | Data rate | — | — | 312/320 | Typ+0.1% | Mbps |
| STARTUP | | | | | | |
| $T_{STRT\_BIAS}$ | Bias startup time[2] | — | — | 0.5 | 3 | µs |

*Table continues on the next page...*

## Table 43. SPI timing (continued)

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| | | | Master (MTFE = 1, CPHA = 0)[9] | -2 + N x SPI IPG clock period [10] | — | |
| | | | Master (MTFE = 1, CPHA = 1) | –2 | — | |
| 11 | $t_{SUO}$ | Data valid (after SCK edge) | Master (MTFE = 0) | — | 7 [11] | ns |
| | | | Slave | — | 23 | |
| | | | Master (MTFE = 1, CPHA = 0)[12] | — | 7 + SPI IPG Clock Period | |
| | | | Master (MTFE = 1, CPHA = 1) | — | 7 | |
| 12 | $t_{HO}$ | Data hold time for outputs | Master (MTFE = 0) | –4 [11] | — | ns |
| | | | Slave | 3.8 | — | |
| | | | Master (MTFE = 1, CPHA = 0) [12] | -4 + SPI IPG Clock Period | — | |
| | | | Master (MTFE = 1, CPHA = 1) | –4 | — | |

1. Slave Receive Only mode can operate at a maximum frequency of 60 MHz. In this mode, the SPI can receive data on SIN, but no valid data is transmitted on SOUT.
2. For SPI_CTARn[PCSSCK] - 'PCS to SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[CSSCK] - 'PCS to SCK Delay Scaler' configuration is '2' (0000h).
3. For SPI_CTARn[PASC] - 'After SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[ASC] - 'After SCK Delay Scaler' configuration is '2' (0000h).
4. The numbers are valid when SPI is configured for 50/50. Refer the Reference manual for the mapping of the duty cycle to each configuration. A change in duty cycle changes the parameter here. For example, a configuration providing duty cycle of 33/66 at SPI translates to min tSCK/3 - 1.5 ns and max tSCK/3 + 1.5 ns.
5. The slave mode parameters ($t_{SUI}$, $t_H$I, $t_{SUO}$ and $t_{HO}$) assume 50% duty cycle on SCK input. Any change in SCK duty cycle input must be taken care during the board design or by the master timing.
6. The slave receive only mode parameters ($t_{SUI}$ and $t_{HI}$) assume 50% duty cycle on SCK input. Any change in SCK duty cycle input must be taken care during the board design or by the master timing. However, there is additional restriction in the slave receive only mode that the duty cycle at the slave input should not go below $t_{sdc}$(min) corresponding to the $t_{sdc}$(min) for the slave receive mode.
7. In the master mode, this is governed by $t_{PCSSCK}$. Refer the SPI chapter in the Reference Manual for details. The minimum spec is valid only for SPI_CTARn[PCSSCK]= '0b01' (PCS to SCK delay prescalar of 3) or higher.
8. In the master mode, this is governed by $t_{PASC}$. Refer the SPI chapter in the Reference Manual for details. The minimum spec is valid only for SPI_CTARn[PASC]= '0b01' (after SCK delay prescalar of 3) or higher.
9. For SPI_CTARn[BR] - 'Baud Rate Scaler' configuration is >= 4.
10. N = Configured sampling point value in MTFE=1 Mode.
11. Same value is applicable for PCS timing in continuous SCK mode.
12. SPI_MCR[SMPL_PT] should be set to 1.

**NOTE**

For numbers shown in the following figures, see Table 43.

## 9.5 LINFlexD timing specifications

The maximum bit rate is 1.875 MBit/s.

## 9.6 I²C timing

**Table 44. I²C SCL and SDA input timing specifications**

| Number | Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | I_tHD:STA | Start Condition hold time | 2 | - | Peripheral clock |
| 2 | I_t_LOW | Clock low time | 8 | - | |
| 3 | I_tHD:DAT | Data hold time | 2 | - | |
| 4 | I_tHIGH | Clock high time | 4 | - | |
| 5 | I_tSU:DAT | Data setup time | 4 | - | |
| 6 | I_tSU:STA | Start condition setup time (for repeated start condition only) | 2 | - | |
| 7 | I_tSU:STOP | Stop condition setup time | 2 | - | |

**Table 45. I²C SCL and SDA output timing specifications**

| Number | Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | O_tHD:STA | Start condition hold time[1] | 6 | - | Peripheral clock |
| 2 | O_t_LOW | Clock low time[1] | 10 | - | |
| 3 | O_tHD:DAT | Data hold time[1] | 7 | - | |
| 4 | O_t_HIGH | Clock high time[1] | 10 | - | |
| 5 | O_tSU:DAT | Data setup time[1] | 2 | - | |
| 6 | O_tSU:STA | Start condition setup time (for repeated start condition only)[1] | 20 | - | |
| 7 | O_tSU:STOP | Stop condition setup time[1] | 10 | - | |
| 8 | O_tr | SCL/SDA rise time[2] | - | 99.6 | ns |
| 9 | O_tf | SCL/SDA fall time[1] | - | 99.6 | |

1. Programming IBFD (I²C Bus Frequency Divider Register) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IBDR (I²C Bus Data I/O Register).
2. Serial data (SDA) and Serial clock (SCL) reaches peak level depending upon the external signal capacitance and pull up resistor values as SDA and SCL are open-drain type outputs which are only actively driven low by the I²C module.

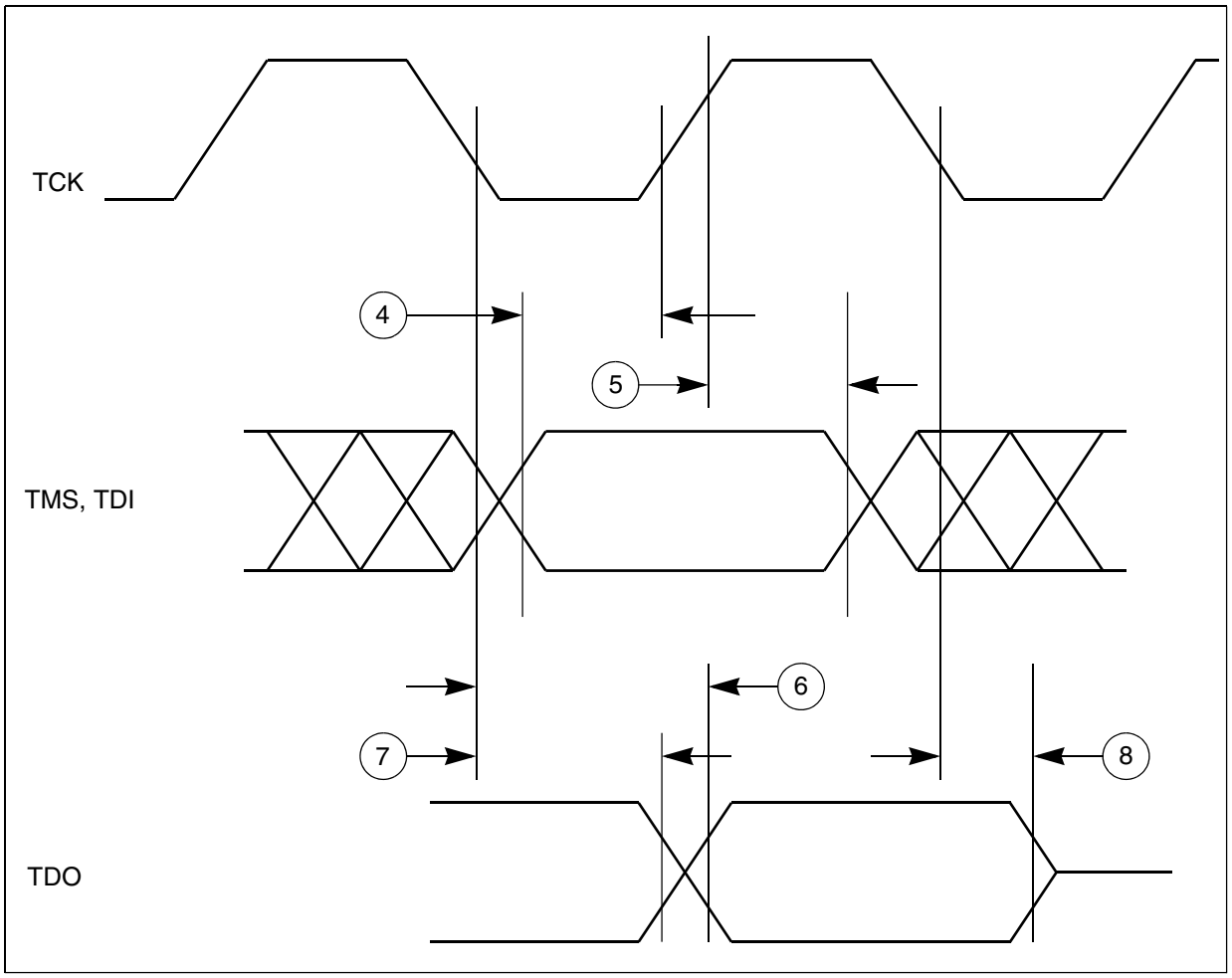


**Figure 33. JTAG test access port timing**

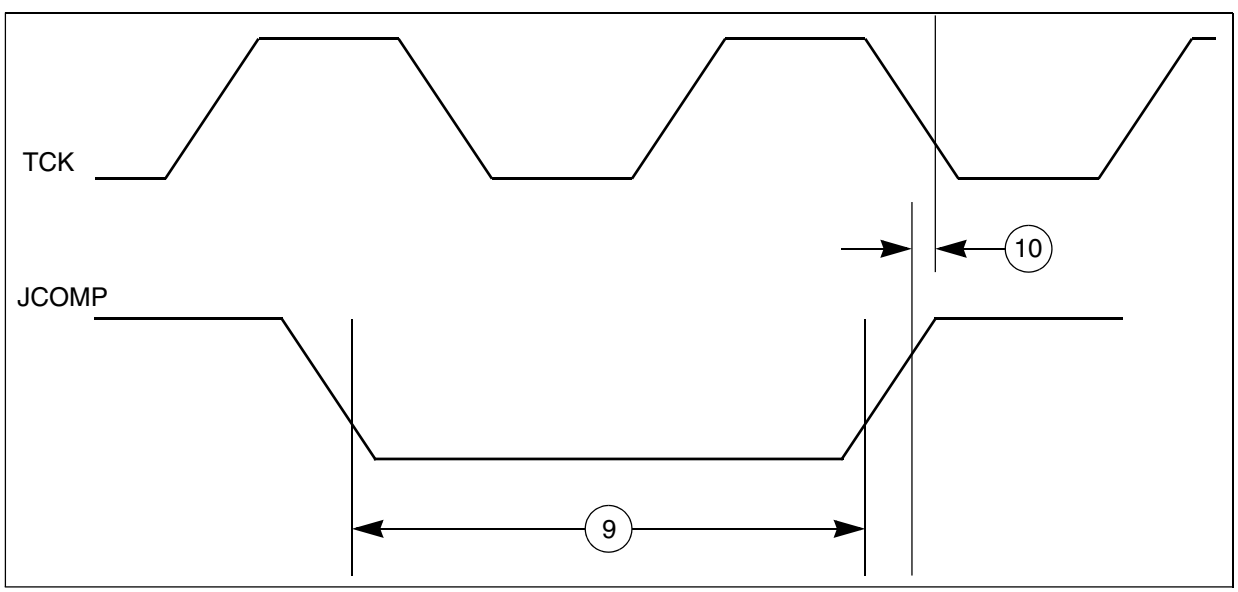


**Figure 34. JTAG JCOMP timing**

**Table 47. Nexus Aurora debug port timing (continued)**

| # | Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|---|
| 9 | $S_O$ | Differential output skew | — | 20 | ps |
| 10 | $S_{MO}$ | Lane to lane output skew | — | 1000 | ps |
| 11 | OUI | Aurora lane Unit Interval | 800 | 800 | ps |

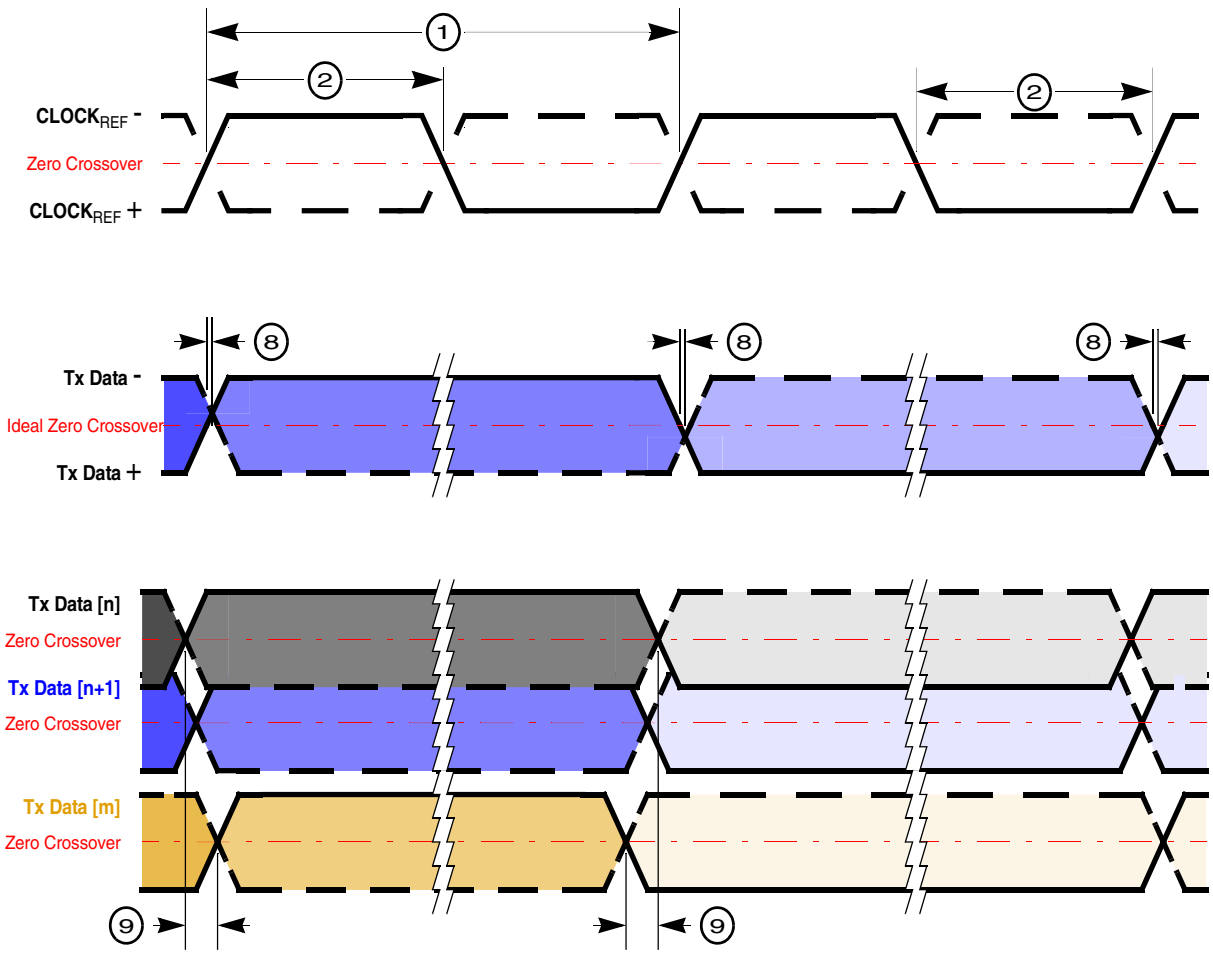


**Figure 36. Nexus Aurora timings**

# 11 WKUP/NMI timing specifications

**Table 48. WKUP/NMI glitch filter**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $W_{FNMI}$ | NMI pulse width that is rejected | — | — | 20 | ns |
| $W_{NFNMI}$ | NMI pulse width that is passed | 400 | — | — | ns |

### 14.1.5 Data to clock timing

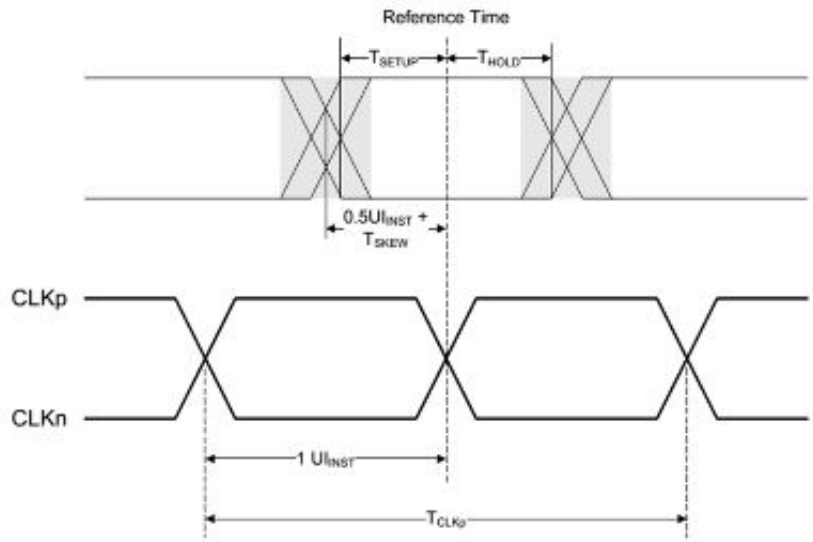


**Figure 41. Definition**

**Table 54. Data to clock timing specifications**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CLKP}$ | Clock Period | 40 | - | 500 | MHz |
| $UI_{INST}$ | UI Instantaneuous | 1 | - | 12.5 | ns |
| $T_{SETUP}$ | Data to Clock Setup Time | 0.15 | - | - | UIINST |
| $T_{HOLD}$ | Clock to Data Hold Time | 0.15 | - | - | UIINST |

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# 15 Thermal Specifications

## 15.1 Thermal characteristics

**Table 55. 257MAPBGA package thermal characteristics**

| Symbol | Parameter | Conditions | 257MAPBGA | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient natural convection [1, 2] | Single layer board - 1s | 41.8 | °C/W |
| | | Four layer board - 2s2p[3] | 22.3 | |
| $R_{\theta JMA}$ | Thermal resistance, junction-to-ambient forced convection at 200 ft/min[1, 3] | Single layer board - 1s | 29.8 | °C/W |
| | | Four layer board - 2s2p | 17.7 | |
| $R_{\theta JB}$ | Thermal resistance junction-to-board[4] | — | 7.6 | °C/W |
| $R_{\theta JC}$ | Thermal resistance junction-to-case[5] | — | 5.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-package-top natural convection[6] | — | 0.2 | °C/W |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

### 15.1.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, $T_J$, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

$$T_J = T_{BRD} + (R_{\theta JB} \times P_D)$$

where:

- $T_A$ = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JB}$ = junction to board thermal resistance (°C/W)
- $T_{\theta BRD}$ = average board temperature just outside the package periphery (°C)
- $P_D$ = power dissipation in the package (W)