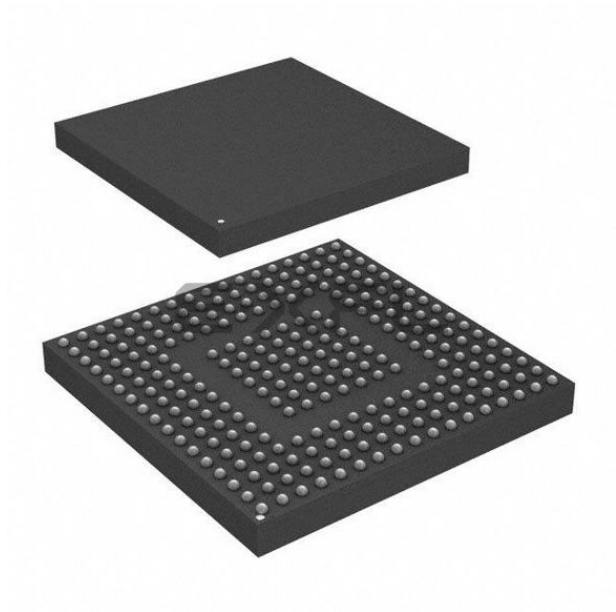

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Details	
Product Status	Obsolete
Core Processor	e200z4, e200z7 (2)
Core Size	32-Bit Tri-Core
Speed	180MHz, 240MHz
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Peripherals	POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	1.5M x 8
Voltage - Supply (Vcc/Vdd)	1.19V ~ 5.5V
Data Converters	A/D 16x12b SAR, 4x12 Sigma; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32r274kbk2mmmr

Table 5. Temperature values

Temperature	T_A
M	-40 °C to 125 °C
V	-40 °C to 105 °C

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed.

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 6. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD\_HV\_PMU}$	3.3 V PMU supply voltage	—	–0.3	4.0[1, 2]	V
$V_{DD\_HV\_REG3V8}$	REG3V8 Supply Voltage	—	–0.3	5.5	V
$V_{DD\_HV\_IO*}$	3.3 V Input/Output Supply Voltage, LFAST IO Supply, RGMII IO Supply and PWM IO Supply	—	–0.3	3.63[1, 2]	V
$V_{SS\_HV\_IOx}$	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD\_HV\_FLA}$	3.3 V flash supply voltage	—	–0.3	3.63[1, 2]	V
$V_{DD\_HV\_RAW}$	AFE RAW supply voltage	—	–0.1	4	V
$V_{DD\_HV\_DAC}$	AFE DAC supply voltage	—	–0.1	4	V
$V_{DD\_LV\_IO*}$	Aurora supply voltage	—	–0.3	1.5	V
V_{DD}	1.25 V core supply voltage[3, 4, 5]	—	–0.3	1.5	V
V_{SS}	1.25 V core supply ground[3, 4, 5]	—	–0.3	0.3	V
$V_{SS\_LV\_OSC}$	Oscillator amplifier ground	—	–0.1	0.1	V
$V_{DD\_LV\_PLL0}$	System PLL supply voltage	—	–0.3	1.5	V
$V_{DD\_LV\_LFASTPLL}$	LFAST PLL supply voltage	—	–0.3	1.5	V
$V_{DD\_HV\_ADCREF0/1}$	ADC_0 and ADC_1 high reference voltage	—	–0.3	5.5	V
$V_{SS\_HV\_ADCREF0/1}$	ADC_0 and ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADC}$	3.3 V ADC supply voltage	—	–0.3	4.0 [1, 2]	V

Table continues on the next page...

Table 6. Absolute maximum ratings (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{SS\_HV\_ADC}$	3.3 V ADC supply ground	—	–0.1	0.1	V
TV_{DD}	Supply ramp rate[6]	—	0.00005	0.1	V/µs
V_{IN_XOSC}	Voltage on XOSC pins with respect to ground	—	-0.3	1.47	V
V_{INA}	Voltage on SAR ADC analog pin with respect to ground ($V_{SS\_HV\_ADCREFx}$)	—	–0.3	6.0	V
V_{INA_SD}	Voltage on Sigma-Delta ADC analog pin with respect to ground[7]	Powered up [8]	-0.3	$V_{DD\_HV\_RAW}$ + 0.3	V
		Powered down [9]	-0.3	1.47	
V_{IN}	Voltage on any digital pin with respect to ground ($V_{SS\_HV\_IOx}$)	Relative to $V_{DD\_HV\_IOx}$	–0.3	$V_{DD\_HV\_IOx}$ + 0.3 [10]	V
$V_{DD\_LV\_DPHY}$	MIPICSI2 DPHY voltage supply[3, 4, 5]	—	–0.3	1.5	V
$V_{SS\_LV\_DPHY}$	MIPICSI2 DPHY supply ground[3, 4, 5]	—	–0.3	0.3	V
I_{INJPAD}[11]	Injected input current on any pin during overload condition[12]	—	–10	10[13]	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	Storage temperature	—	–55	150	°C

1. 5.3 V for 10 hours cumulative over lifetime of device; 3.3 V +10% for time remaining.
2. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
3. 1.45 V to 1.5 V allowed for 60 seconds cumulative time at maximum T_J = 150°C; remaining time as defined in note 5 and note 6.
4. 1.375 V to 1.45 V allowed for 10 hours cumulative time at maximum T_J = 150°C; remaining time as defined in note 6.
5. 1.32 V to 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum T_J=150°C.
6. TV_{DD} is relevant for all external supplies.
7. ADC inputs include an overvoltage detect function that detects any voltage higher than 1.2 V with respect to ground on either ADC input and open circuit (disconnect) the input in order to prevent damage to the ADC internal circuitry. The ADC input remains disconnected until the inputs return to the normal operating range.
8. SDADC is powered up and overvoltage protection is ON.
9. SDADC is powered up and overvoltage protection is OFF.
10. Only when $V_{DD\_HV\_IOx}$ < 3.63 V.
11. The maximum value limits of injection current and input voltage both must be followed together for proper device operation.
12. No input current injection circuitry on AFE pins.
13. The maximum value of 10 mA applies to pulse injection only. DC current injection is limited to a maximum of 5 mA.

4.2 Operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the datasheet are valid, except where explicitly noted. The device operating conditions must not be exceeded, or the functionality of the device is not guaranteed.

Table 7. Device operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
$V_{DD\_HV\_PMU}$	3.3V PMU Supply Voltage	—	3.13[2]	3.3	3.6	V
$V_{DD\_HV\_REG3V8}$	REG3V8 Supply Voltage	—	3.13	3.8	5.5	V
V_{DD}	Core Supply Voltage	—	1.19[2]	1.25	1.31[3]	V
$V_{DD\_HV\_IO*}$	Main GPIO 3V Supply Voltage, LFAST IO Supply, RGMII IO Supply, PWM IO Supply Voltage	—	3.13[2]	3.3	3.6	V
$V_{DD\_LV\_IO\_*}$[4]	Aurora Supply Voltage	—	1.19	1.25	1.31	V
$V_{DD\_LV\_PLL0}$	System PLL Supply Voltage	—	1.19[2]	—	1.31	V
$V_{DD\_LV\_LFASTPLL}$	LFAST PLL Supply Voltage	—	1.19	—	1.31	V
$V_{DD\_HV\_FLA}$[5]	Flash Supply Voltage	—	3.13[2]	3.3	3.6	V
$V_{DD\_HV\_ADC}$	SAR ADC Supply Voltage (HVD supervised)	—	3.13[2]	3.3	3.6[6]	V
$V_{DD\_HV\_RAW}$	3.3V AFE RAW Supply Voltage	—	3.13	3.3	3.6	V
$V_{DD\_HV\_DAC}$	3.3V AFE DAC Supply Voltage	—	3.13	3.3	3.6	V
$V_{DD\_HV\_ADCREF0/1}$	ADC_0 and ADC_1 high reference voltage	—	3.13	3.3	3.6	V
V_{IN}	Voltage on digital pin with respect to ground ($V_{SS\_HV\_IOx}$)	—	—	—	$V_{DD\_HV\_IOx}$ +0.3	V
V_{INSDPP}	Sigma-Delta ADC Input Voltage (peak-peak)[7, 8]	Differential	—	—	1.2	V
V_{INSR}	Sigma-Delta ADC Input Slew Rate[7]	—	—	—	165	V/µs
R_{TRIM_TOL}	External Trim Resistor tolerance	±0.1%	40.16	40.2	40.25	kΩ
R_{TRIM_TEMPCO}	External Trim Resistor Temperature Coefficient	—	—	—	25	ppm/°C
V_{INA}[9]	Voltage on SAR ADC analog pin with respect to ground ($V_{SS\_HV\_ADCREFx}$)	—	—	—	$V_{DD\_HV\_ADCREFx}$	V
$V_{DD\_LV\_DPHY}$	MIPICSI2 DPHY voltage supply[10]		1.19	1.25	1.31	V
T_A,[11]	Ambient temperature at full performance [12]	—	–40	—	125	°C

Table continues on the next page...

Table 7. Device operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
T_J[11]	Junction temperature	—	–40	—	150	°C
F_{XTAL}	XOSC Crystal Frequency[13]	—	—	40	—	MHz
AFE Bypass Modes Only						
Single-Ended External Clock[14]						
$EXTAL_{clk}$	EXTAL external clock frequency			40		MHz
$V_{inxoscjit}$	EXTAL external clock Cycle to Cycle Jitter (RMS)	—	—	—	2.5[15]	ps
$V_{inxoscclkvil}$	EXTAL external clock input low voltage	—	0	—	0.4	V
$V_{inxoscclkvih}$	EXTAL external clock input high voltage	—	1	—	1.23	V
t_r/t_f	Rise/fall time of EXTAL external clock input				1	ns
t_{dc}	Duty Cycle of EXTAL external clock input		47	50	53	%
Differential LVDS External Clock						
$LVDS_{clk}$	LVDS external clock frequency			40		MHz
$LVDSV_{inxoscclk}$	LVDS external clock input voltage		0		1.36	V
$LVDSV_{inxoscclk(p-p)}$	LVDS external clock input voltage (peak-peak)	Voltage driven, AC coupled Differential	0.45	0.70	1.12	V
$LVDSI_{inxoscclk}$	LVDS external clock input current	Current driven, DC coupled.	3.0	3.5	4.0	mA
$LVDSV_{inxoscjit}$	LVDS external clock Jitter (RMS) [15]				2.5	ps
t_r/t_f	Rise/fall time of LVDS external clock input	20% - 80%			1.5	ns
t_{dcLVDS}	Duty Cycle of LVDS external clock input		47	50	53	%

1. Full functionality cannot be guaranteed when voltages are out of the recommended operating conditions.
2. Min voltage takes into account the LVD variation.
3. Max voltage takes into account HVD variation.
4. Aurora supply must connect to core supply voltage at board level.
5. The ground connection for the $V_{DD\_HV\_FLA}$ is shared with V_{SS}.
6. Supply range does not take into account HVD levels. Full range can be achieved after power-up, if HVD is disabled. See Voltage regulator electrical characteristics section for details.
7. Around common mode voltage of 0.7 V. Input voltage cannot exceed 1.4 V prior to AFE start-up completion (VREF and VREGs on and LVDs cleared).
8. SDADC input voltage full scale is 1.2 Vpp
9. On channels shared between ADC0 and 1, $V_{DD\_HV\_ADCREFx}$ is the lower of $V_{DD\_HV\_ADCREF0/1}$.
10. $V_{DD\_LV\_DPHY}$ supply should be shorted to core supply voltage VDD on board. Refer to AN5251. Contact your NXP sales representative for details.

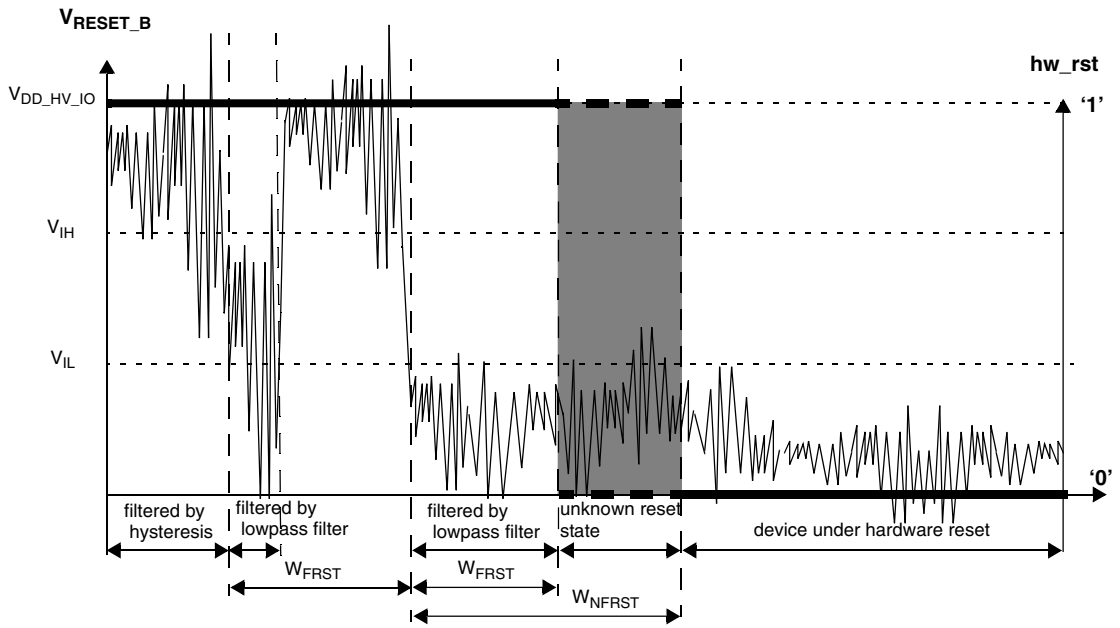


Figure 5. Noise filtering on reset signal

Table 18. RESET_B electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level TTL (Schmitt Trigger)	—	2.0	—	$V_{DD\_HV\_IOx}$ + 0.4	V
V_{IL}	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.56	V
V_{HYS}[2]	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV
I_{OL_R}	Strong pull-down current	Device under power-on reset $V_{DD\_HV\_IO}$ = 1.2 V V_{OL} = 0.35 x $V_{DD\_HV\_IO}$	0.2	—	—	mA
		Device under power-on reset $V_{DD\_HV\_IO}$=3.0 V V_{OL} = 0.35 x $V_{DD\_HV\_IO}$	15	—	—	mA
W_{FRST}	RESET_B input filtered pulse	—	—	—	500	ns
W_{NFRST}	RESET_B input not filtered pulse	—	2400	—	—	ns
$\lvert I_{WPD} \rvert$	Weak pull-down current absolute value	V_{IN} = $V_{DD\_HV\_IOx}$	30	—	100	µA

1. $V_{DD\_HV\_IOx}$ = 3.3 V -5%,+10%, T_J = –40 / 150°C, unless otherwise specified.
2. Data based on characterization results, not tested in production.

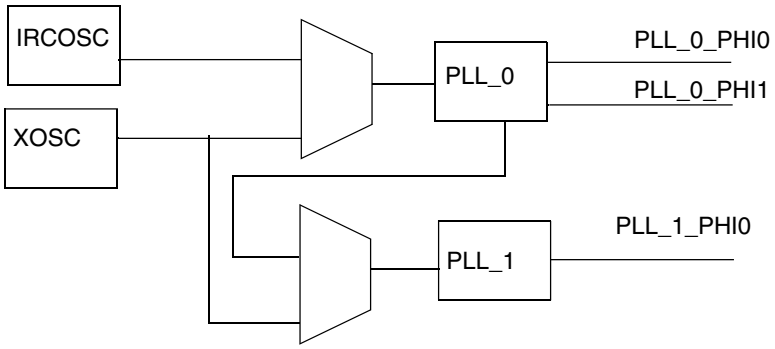


Figure 6. PLL integration

Table 20. PLL0 electrical characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{PLL0IN}	PLL0 input clock[2, 3]	—	14	—	44	MHz
Δ_{PLL0IN}	PLL0 input clock duty cycle[2]	—	40	—	60	%
$f_{PLL0VCO}$	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI0}$	PLL0 output clock PHI0	—	4.76	—	625[4]	MHz
$f_{PLL0PHI1}$	PLL0 output clock PHI1	—	20	—	156	MHz
$t_{PLL0LOCK}$	PLL0 lock time	—	—	—	100	µs
$\Delta_{PLL0LTJ}$	PLL0 long term jitter f_{PLL0IN} = 8 MHz (resonator)[5]	$f_{PLL0PHI0}$ = 40 MHz, 1 µs			± 1	ns
		$f_{PLL0PHI0}$ = 40 MHz, 13 µs			± 1	ns
I_{PLL0}	PLL0 consumption		—	—	5	mA

1. $V_{DD\_LV\_PLL0}$ =1.25 V ± 5%, T_J = -40 / 150 °C unless otherwise specified.
2. PLL0IN clock retrieved directly from either IRCOSC or external XOSC clock.
3. f_{PLL0IN} frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure the reference clock to the PLL analog loop is in the range 8 MHz-20 MHz
4. The maximum clock outputs are limited by the design clock frequency requirements as per recommended operating conditions.
5. $V_{DD\_LV\_PLL0}$ noise due to application in the range $V_{DD\_LV\_PLL0}$ = 1.25 V±5%, with frequency below PLL bandwidth (40 KHz) will be filtered.

Table 21. FMPLL1 electrical characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{PLL1IN}	PLL1 input clock[2]	—	38	—	78	MHz
Δ_{PLL1IN}	PLL1 input clock duty cycle[2]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI0}$	PLL1 output clock PHI0	—	4.76	—	625	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	µs
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
I_{PLL1}	PLL1 consumption		—	—	6	mA

1. $V_{DD\_LV\_PLL0}$ = 1.25 V ± 5%, T_J = -40 / 150°C unless otherwise specified.
2. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock.

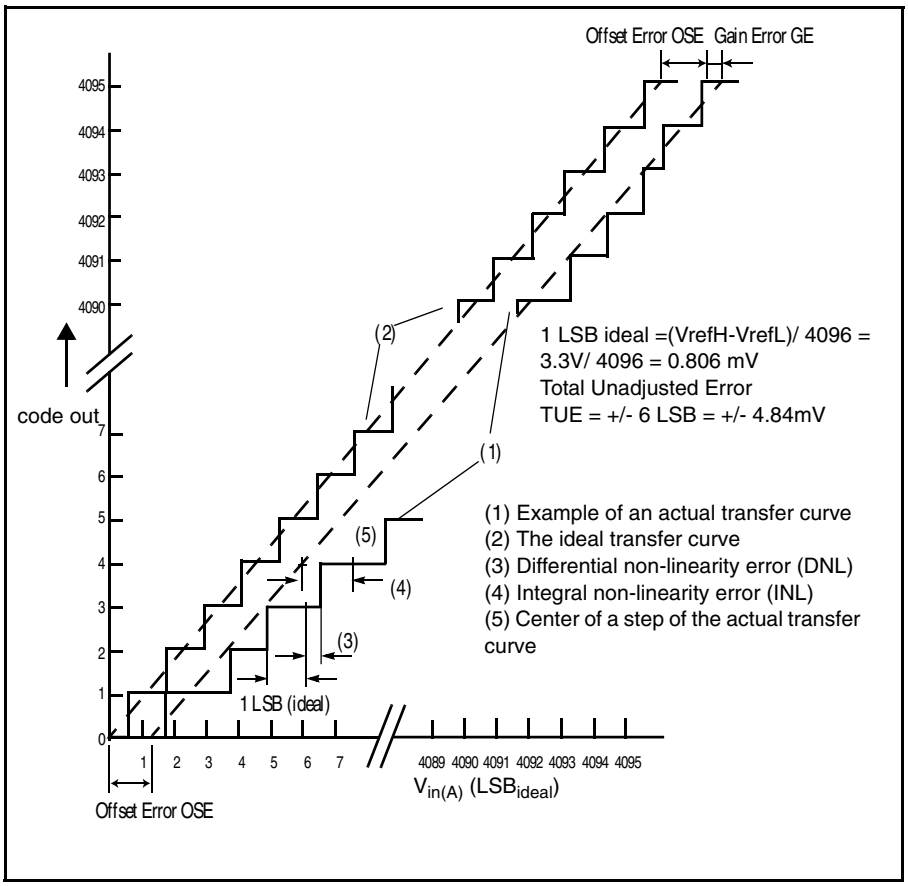


Figure 7. ADC characteristics and error definitions

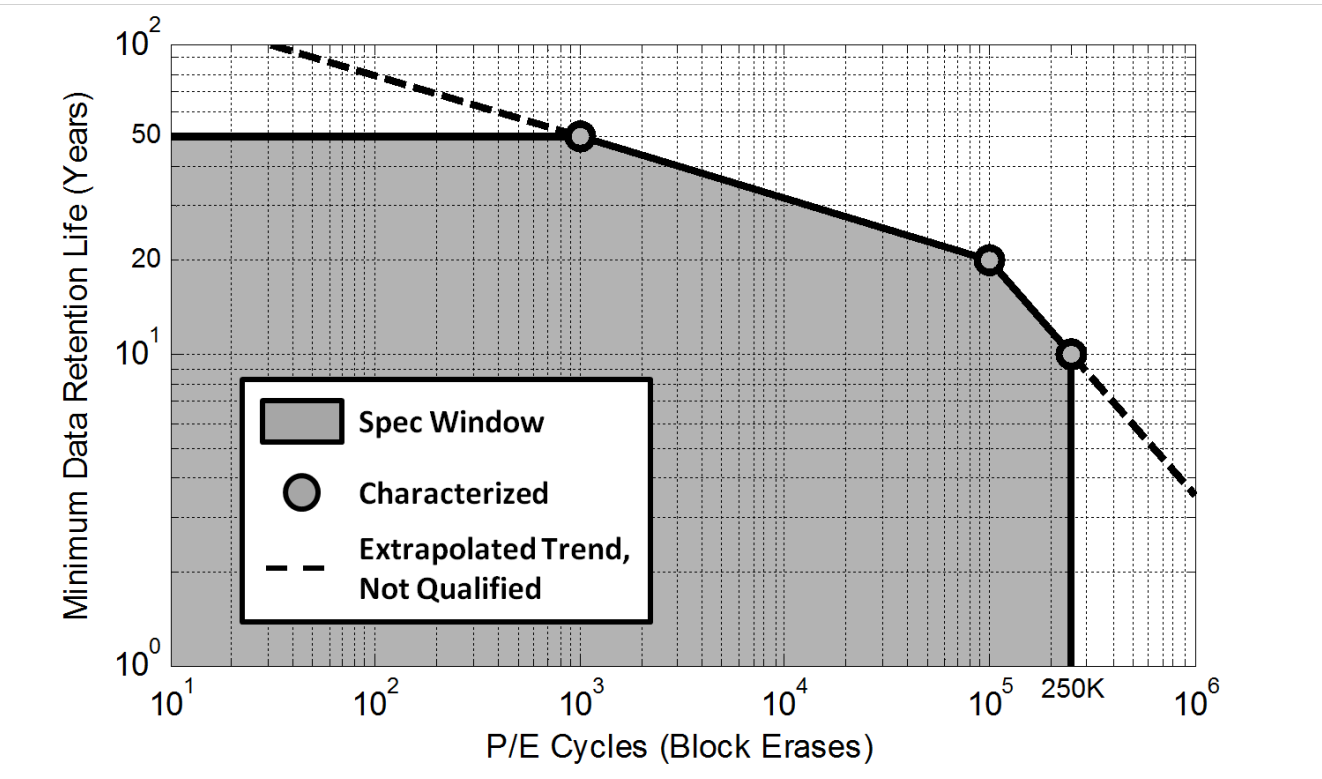
Table 26. Sigma Delta ADC Parameters (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Characterized under the following conditions: • 0.6 Vpp (i.e. -6 dBFS) input signals applied at the following frequencies one at a time: 20.77 KHz, 317.7 KHz, 857.7 KHz, 1.411 MHz, 2.95 MHz, 3.897 MHz, and 4.997 MHz and the SNR in dBFS is then calculated. • SNR at 5 MHz will be reduced by 5 dB due to decimation filter roll off. • The SNR is specified to be 67 dBFS typical for input frequencies between 20 KHz and 4 MHz. Mismatch shaper on.				
$SNR_{SDA\_MM\_OFF}$[1]	Signal-to-Noise Ratio Mismatch Shaper off	Input Frequency Range and integration bandwidth are from 20 KHz to 5 MHz. (using full-bandwidth decimation filter coefficients). Production test frequencies 449 KHz and 4 MHz. Production test amplitude is -6 dBFS = 0.6 Vpp. Characterized under the following conditions: • 0.6 Vpp (i.e. -6dBFS) input signals applied at the following frequencies one at a time: 20.77 KHz, 317.7 KHz, 857.7 KHz, 1.411 MHz, 2.95 MHz, 3.897 MHz, and 4.997 MHz and the SNR in dBFS is then calculated. • SNR at 5 MHz will be reduced by 5 dB due to decimation filter roll off. • The SNR is specified to be 67 dBFS typical for input frequencies between 20 KHz and 4 MHz. Mismatch shaper off.	65	67	—	dBFS
$SNDR_{SDA\_MM\_ON}$[1]	Signal-to-Noise-and-Distortion Ratio Mismatch Shaper on	Input Frequency Range and integration bandwidth are from 20 KHz to 5 MHz. (using full-bandwidth decimation filter coefficients). Production test frequencies 449 KHz and 4 MHz. Production test amplitude is -6 dBFS = 0.6 Vpp. Characterized under the following conditions: • 0.6 Vpp (i.e. -6 dBFS) input signals applied at the following frequencies one at a time: 20.77 KHz, 317.7 KHz, 857.7 KHz, 1.411 MHz, 2.95 MHz, 3.897 MHz, and 4.997 MHz and the SNDR in dBFS is then calculated. • SNR at 5 MHz will be reduced by 5 dB due to decimation filter roll off. • The SNR is specified to be 64 dBFS typical for input frequencies between 20 KHz and 4 MHz. Mismatch shaper on.	62	64	—	dBFS
$SNDR_{SDA\_MM\_OFF}$[1]	Signal-to-Noise-and-Distortion Ratio Mismatch Shaper off	Input Frequency Range and integration bandwidth are from 20 KHz to 5 MHz. (using full-bandwidth decimation filter coefficients)	60	62	—	dBFS

Table continues on the next page...

8.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



8.5 Flash memory AC timing specifications

Table 31. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs

Table continues on the next page...

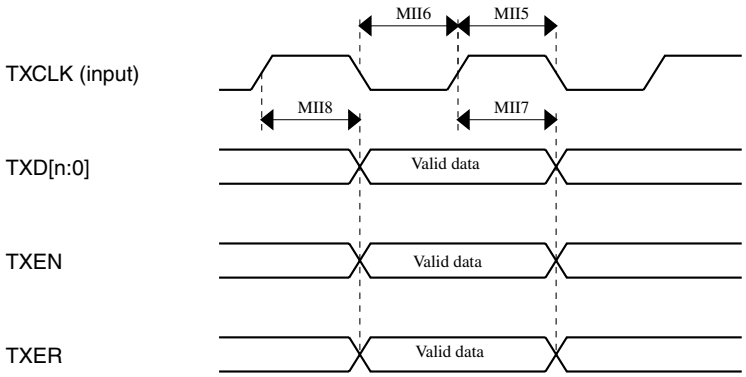


Figure 10. MII transmit signal timing diagram

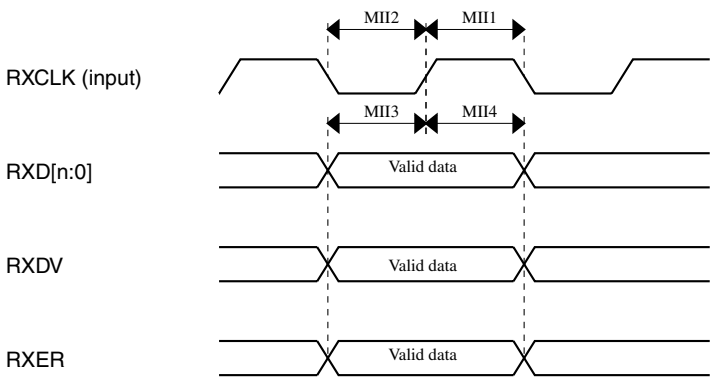


Figure 11. MII receive signal timing diagram

9.1.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

- Measurements are with input transition of 1 ns and output load of 25 pF.

Table 34. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns

Table continues on the next page...

Table 34. RMII signal switching specifications (continued)

Num	Description	Min.	Max.	Unit
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

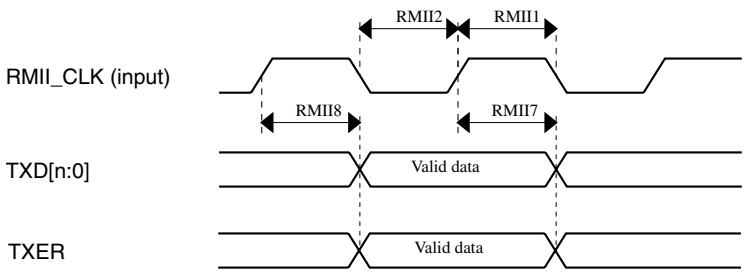


Figure 12. RMII transmit signal timing diagram

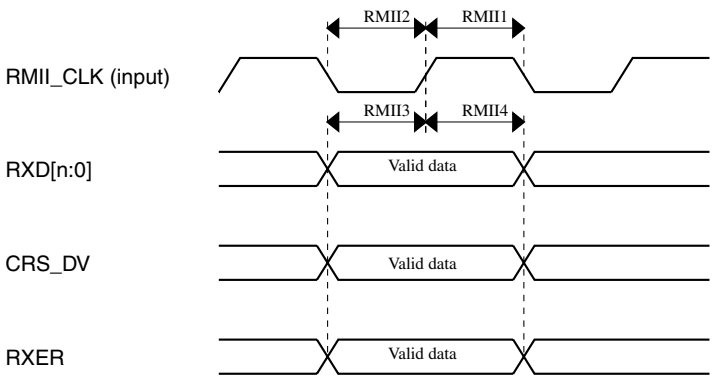


Figure 13. RMII receive signal timing diagram

9.1.3 RGMII signal switching specifications

The RGMII interface works at 3.3 V compatible levels as mentioned in RGMII pad DC electrical characteristics.

The following timing specs meet the requirements for RGMII style interfaces for a range of transceiver devices.

- Measurements are with input transition of 0.750 ns and output load of 10 pF.

Table 35. RGMII signal switching specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
—	Input Duty cycle (Clock from external PHY)	48	—	52	%	
Tcyc	Clock cycle duration	7.2	8.0	8.8	ns	1
TskewT	Data to clock output skew at transmitter	-500	0	500	ps	2
TskewR	Data to clock input skew at receiver	1	1.8	2.6	ns	2

Table continues on the next page...

6. Total lumped capacitance including silicon, package pin and bond wire. Application board simulation is needed to verify LFAST template compliancy.
7. Absolute min = 0.15 V – (285 mV / 2) = 0 V
8. Absolute max = 1.6 V + (285 mV / 2) = 1.743 V
9. Total capacitance including silicon, package pin and bond wire
10. Total inductance including silicon, package pin and bond wire

9.4 Serial Peripheral Interface (SPI) timing specifications

The following table describes the SPI electrical characteristics.

MTEF=1 Mode timing values given below are only applicable when external SPI is in classic mode. Slave mode timing values given below are applicable when device is in MTFE=0.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured as SRE = 11.

Table 43. SPI timing

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	SPI cycle time	Master (MTFE = 0)	50	—	ns
			Master (MTFE = 1)	50	—	
			Slave (MTFE = 0)	50	—	
			Slave Receive Only mode[1]	16	—	
2	t_{CSC}	PCS to SCK delay	Master	63.8[2]	—	ns
3	t_{ASC}	After SCK delay	Master	68.8[3]	—	ns
4	t_{SDC}	SCK duty cycle	Master[4]	$t_{SCK}/2 - 1$	$t_{SCK}/2 + 1$	ns
			Slave[5]	—	—	ns
			Slave Receive only mode[6]	tSCK/2 – 0.750	tSCK/2 + 0.750	ns
5	t_A	Slave access time	$\overline{SS}$ active to SOUT valid	—	25	ns
6	t_{DIS}	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	25	ns
7	t_{PCSC}	PCSx to $\overline{PCSS}$ time	—	13 [7]	—	ns
8	t_{PASC}	$\overline{PCSS}$ to PCSx time	—	13 [8]	—	ns
9	t_{SUI}	Data setup time for inputs	Master (MTFE = 0)	15	—	ns
			Slave	2	—	
			Slave Receive Mode	2	—	
			Master (MTFE = 1, CPHA = 0)[9]	15-N x SPI IPG clock period[10]	—	
			Master (MTFE = 1, CPHA = 1)	15	—	
10	t_{HI}	Data hold time for inputs	Master (MTFE = 0)	–2	—	ns
			Slave	4	—	
			Slave Receive Mode	4	—	

Table continues on the next page...

Table 43. SPI timing (continued)

No.	Symbol	Parameter	Conditions	Min	Max	Unit
			Master (MTFE = 1, CPHA = 0)[9]	-2 + N x SPI IPG clock period [10]	—	
			Master (MTFE = 1, CPHA = 1)	–2	—	
11	t_{SUO}	Data valid (after SCK edge)	Master (MTFE = 0)	—	7 [11]	ns
			Slave	—	23	
			Master (MTFE = 1, CPHA = 0)[12]	—	7 + SPI IPG Clock Period	
			Master (MTFE = 1, CPHA = 1)	—	7	
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	–4 [11]	—	ns
			Slave	3.8	—	
			Master (MTFE = 1, CPHA = 0) [12]	-4 + SPI IPG Clock Period	—	
			Master (MTFE = 1, CPHA = 1)	–4	—	

1. Slave Receive Only mode can operate at a maximum frequency of 60 MHz. In this mode, the SPI can receive data on SIN, but no valid data is transmitted on SOUT.
2. For SPI_CTARn[PCSSCK] - 'PCS to SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[CSSCK] - 'PCS to SCK Delay Scaler' configuration is '2' (0000h).
3. For SPI_CTARn[PASC] - 'After SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[ASC] - 'After SCK Delay Scaler' configuration is '2' (0000h).
4. The numbers are valid when SPI is configured for 50/50. Refer the Reference manual for the mapping of the duty cycle to each configuration. A change in duty cycle changes the parameter here. For example, a configuration providing duty cycle of 33/66 at SPI translates to min tSCK/3 - 1.5 ns and max tSCK/3 + 1.5 ns.
5. The slave mode parameters (t_{SUI}, t_HI, t_{SUO} and t_{HO}) assume 50% duty cycle on SCK input. Any change in SCK duty cycle input must be taken care during the board design or by the master timing.
6. The slave receive only mode parameters (t_{SUI} and t_{HI}) assume 50% duty cycle on SCK input. Any change in SCK duty cycle input must be taken care during the board design or by the master timing. However, there is additional restriction in the slave receive only mode that the duty cycle at the slave input should not go below t_{sdc}(min) corresponding to the t_{sdc}(min) for the slave receive mode.
7. In the master mode, this is governed by t_{PCSSCK}. Refer the SPI chapter in the Reference Manual for details. The minimum spec is valid only for SPI_CTARn[PCSSCK]= '0b01' (PCS to SCK delay prescalar of 3) or higher.
8. In the master mode, this is governed by t_{PASC}. Refer the SPI chapter in the Reference Manual for details. The minimum spec is valid only for SPI_CTARn[PASC]= '0b01' (after SCK delay prescalar of 3) or higher.
9. For SPI_CTARn[BR] - 'Baud Rate Scaler' configuration is >= 4.
10. N = Configured sampling point value in MTFE=1 Mode.
11. Same value is applicable for PCS timing in continuous SCK mode.
12. SPI_MCR[SMPL_PT] should be set to 1.

NOTE

For numbers shown in the following figures, see Table 43.

9.5 LINFlexD timing specifications

The maximum bit rate is 1.875 MBit/s.

9.6 I²C timing

Table 44. I²C SCL and SDA input timing specifications

Number	Symbol	Parameter	Value		Unit
			Min	Max	
1	I_tHD:STA	Start Condition hold time	2	-	Peripheral clock
2	I_t_LOW	Clock low time	8	-	
3	I_tHD:DAT	Data hold time	2	-	
4	I_tHIGH	Clock high time	4	-	
5	I_tSU:DAT	Data setup time	4	-	
6	I_tSU:STA	Start condition setup time (for repeated start condition only)	2	-	
7	I_tSU:STOP	Stop condition setup time	2	-	

Table 45. I²C SCL and SDA output timing specifications

Number	Symbol	Parameter	Value		Unit
			Min	Max	
1	O_tHD:STA	Start condition hold time[1]	6	-	Peripheral clock
2	O_t_LOW	Clock low time[1]	10	-	
3	O_tHD:DAT	Data hold time[1]	7	-	
4	O_t_HIGH	Clock high time[1]	10	-	
5	O_tSU:DAT	Data setup time[1]	2	-	
6	O_tSU:STA	Start condition setup time (for repeated start condition only)[1]	20	-	
7	O_tSU:STOP	Stop condition setup time[1]	10	-	
8	O_tr	SCL/SDA rise time[2]	-	99.6	ns
9	O_tf	SCL/SDA fall time[1]	-	99.6	

1. Programming IBFD (I²C Bus Frequency Divider Register) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IBDR (I²C Bus Data I/O Register).
2. Serial data (SDA) and Serial clock (SCL) reaches peak level depending upon the external signal capacitance and pull up resistor values as SDA and SCL are open-drain type outputs which are only actively driven low by the I²C module.

Table 46. JTAG/CJTAG pin AC electrical characteristics [1] (continued)

#	Symbol	Characteristic	Min	Max	Unit
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency.
3. TMS timing is applicable only in CJTAG mode
4. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
5. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

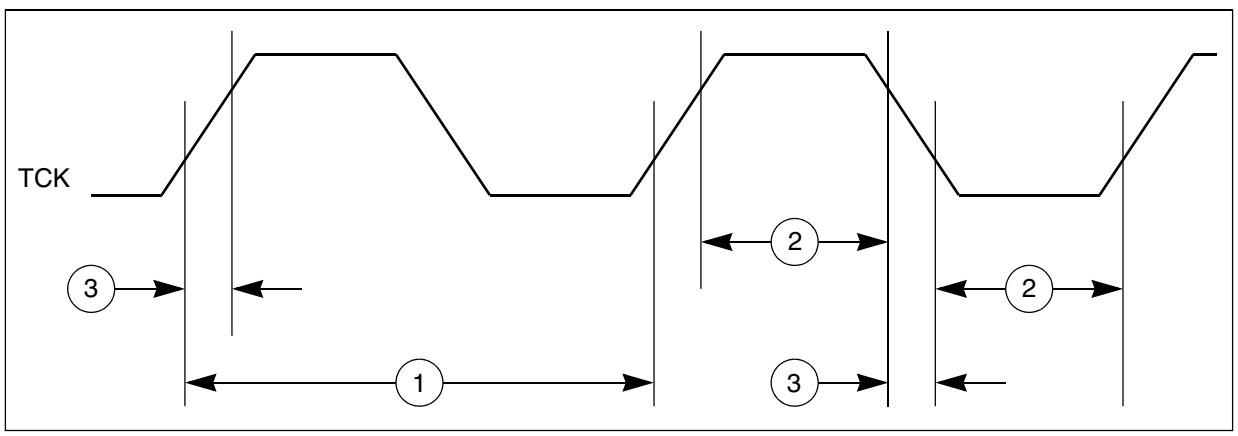


Figure 32. JTAG test clock input timing

14.1.5 Data to clock timing

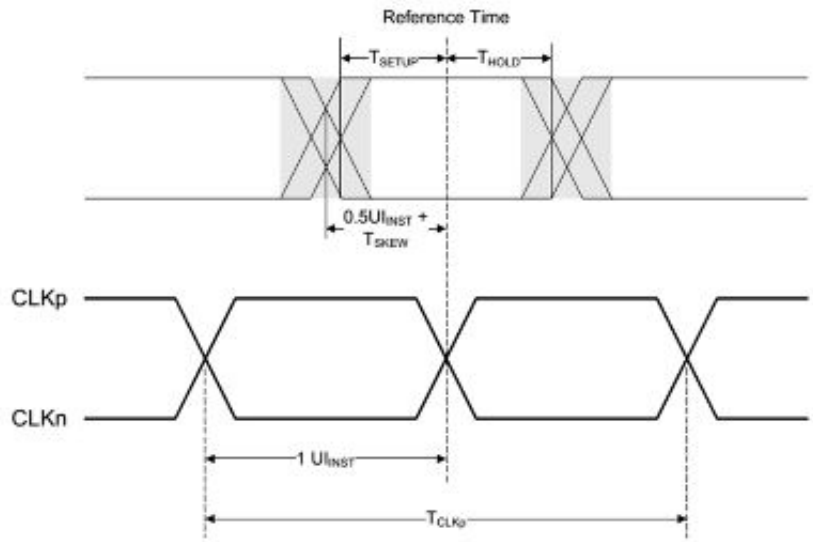


Figure 41. Definition

Table 54. Data to clock timing specifications

Symbol	Parameter	Min	Typ	Max	Unit
T_{CLKP}	Clock Period	40	-	500	MHz
UI_{INST}	UI Instantaneuous	1	-	12.5	ns
T_{SETUP}	Data to Clock Setup Time	0.15	-	-	UIINST
T_{HOLD}	Clock to Data Hold Time	0.15	-	-	UIINST

14.2 MIPICSI2 Disclaimer

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15 Thermal Specifications

15.1 Thermal characteristics

Table 55. 257MAPBGA package thermal characteristics

Symbol	Parameter	Conditions	257MAPBGA	Unit
$R_{\theta JA}$	Thermal resistance, junction-to-ambient natural convection [1, 2]	Single layer board - 1s	41.8	°C/W
		Four layer board - 2s2p[3]	22.3	
$R_{\theta JMA}$	Thermal resistance, junction-to-ambient forced convection at 200 ft/min[1, 3]	Single layer board - 1s	29.8	°C/W
		Four layer board - 2s2p	17.7	
$R_{\theta JB}$	Thermal resistance junction-to-board[4]	—	7.6	°C/W
$R_{\theta JC}$	Thermal resistance junction-to-case[5]	—	5.2	°C/W
Ψ_{JT}	Junction-to-package-top natural convection[6]	—	0.2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

15.1.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

$$T_J = T_{BRD} + (R_{\theta JB} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JB}$ = junction to board thermal resistance (°C/W)
- $T_{\theta BRD}$ = average board temperature just outside the package periphery (°C)
- P_D = power dissipation in the package (W)

package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

15.1.2 References

Semiconductor Equipment and Materials International; 3081 Zanker Road; San Jose, CA 95134 USA; (408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the Web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

16 Packaging

The S32R274 is offered in the following package types.

If you want the drawing for this package	Then use this document number
257-ball MAPBGA	98ASA00081D

NOTE

For detailed information regarding package drawings, refer to www.nxp.com.

17 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

It should be noted that LVD and HVD detectors on VDD supply are disabled by default in external regulation mode for preventing a conflict with external regulator operation but they can be enabled by software once design is powered up.

While designing the system, it is important to ensure that AFE supplies are powered up before data is sent on its input pads.

19 Pinouts

19.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

20 Revision History

Table 58. Revision History

Revision	Date	Description

Rev 4	May, 2018	• Removed section "4.1 Introduction".
		• Removed section "3.2 Format".
		• In Fields, removed figure "Commercial product code structure".
		• In Nexus Aurora debug port timing, added t_{EVTIPW} row.
		• In Ethernet switching specifications changed the following:
		  • Updated the figure RMII/MII serial management channel timing diagram.
		  • In Ethernet MDIO timing table changed MDC10 Min value and MDC11 Max value.
		• Extensively updated Table 32.
		• In Table 7, changed $V_{inxoscclkvih}$ Max value from 1.2 to 1.23.
		• In Table 25, added rows for the symbols $t_{sampleC}$, $t_{sampleS}$,$t_{sampleBG}$, and $t_{sampleTS}$.
		• In Table 6, changed V_{INA} maximum value to 6.0.
		• Added the following footnotes in Absolute maximum ratings :
		  • The maximum value limits of injection current and input voltage both must be followed together for proper device operation.
		  • The maximum value of 10 mA applies to pulse injection only. DC current injection is limited to a maximum of 5 mA.
		• In Table 7, changed V_{INA} maximum value to $V_{DD\_HV\_ADCREFx}$.
		• In Table 2 :
		  • Changed part from FS32R274KBK2MMM to FS32R274KSK2MMM and changed configuration from "B" to "S"
		  • Changed part from FS32R274KBK2VMM to FS32R274KSK2VMM and changed configuration from "B" to "S"
		  • Added "B or S" to Table 3