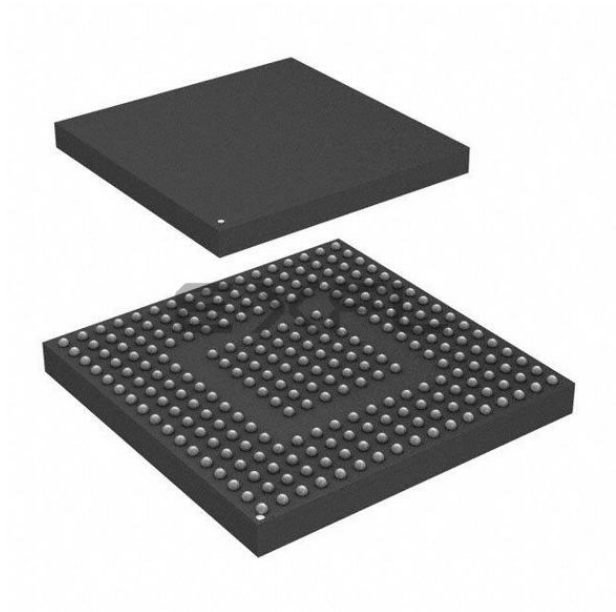

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4, e200z7 (2)
Core Size	32-Bit Tri-Core
Speed	180MHz, 240MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI, ZipWire
Peripherals	POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	1.5M x 8
Voltage - Supply (Vcc/Vdd)	1.19V ~ 5.5V
Data Converters	A/D 16x12b SAR, 4x12 Sigma; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32r274ksk2mmm

4.2 Operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the datasheet are valid, except where explicitly noted. The device operating conditions must not be exceeded, or the functionality of the device is not guaranteed.

Table 7. Device operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
$V_{DD\_HV\_PMU}$	3.3V PMU Supply Voltage	—	3.13[2]	3.3	3.6	V
$V_{DD\_HV\_REG3V8}$	REG3V8 Supply Voltage	—	3.13	3.8	5.5	V
V_{DD}	Core Supply Voltage	—	1.19[2]	1.25	1.31[3]	V
$V_{DD\_HV\_IO*}$	Main GPIO 3V Supply Voltage, LFAST IO Supply, RGMII IO Supply, PWM IO Supply Voltage	—	3.13[2]	3.3	3.6	V
$V_{DD\_LV\_IO\_*}$[4]	Aurora Supply Voltage	—	1.19	1.25	1.31	V
$V_{DD\_LV\_PLL0}$	System PLL Supply Voltage	—	1.19[2]	—	1.31	V
$V_{DD\_LV\_LFASTPLL}$	LFAST PLL Supply Voltage	—	1.19	—	1.31	V
$V_{DD\_HV\_FLA}$[5]	Flash Supply Voltage	—	3.13[2]	3.3	3.6	V
$V_{DD\_HV\_ADC}$	SAR ADC Supply Voltage (HVD supervised)	—	3.13[2]	3.3	3.6[6]	V
$V_{DD\_HV\_RAW}$	3.3V AFE RAW Supply Voltage	—	3.13	3.3	3.6	V
$V_{DD\_HV\_DAC}$	3.3V AFE DAC Supply Voltage	—	3.13	3.3	3.6	V
$V_{DD\_HV\_ADCREF0/1}$	ADC_0 and ADC_1 high reference voltage	—	3.13	3.3	3.6	V
V_{IN}	Voltage on digital pin with respect to ground ($V_{SS\_HV\_IOx}$)	—	—	—	$V_{DD\_HV\_IOx}$ +0.3	V
V_{INSDPP}	Sigma-Delta ADC Input Voltage (peak-peak)[7, 8]	Differential	—	—	1.2	V
V_{INSR}	Sigma-Delta ADC Input Slew Rate[7]	—	—	—	165	V/µs
R_{TRIM_TOL}	External Trim Resistor tolerance	±0.1%	40.16	40.2	40.25	kΩ
R_{TRIM_TEMPCO}	External Trim Resistor Temperature Coefficient	—	—	—	25	ppm/°C
V_{INA}[9]	Voltage on SAR ADC analog pin with respect to ground ($V_{SS\_HV\_ADCREFx}$)	—	—	—	$V_{DD\_HV\_ADCREFx}$	V
$V_{DD\_LV\_DPHY}$	MIPICSI2 DPHY voltage supply[10]		1.19	1.25	1.31	V
T_A,[11]	Ambient temperature at full performance [12]	—	–40	—	125	°C

Table continues on the next page...

Table 7. Device operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
T_J[11]	Junction temperature	—	–40	—	150	°C
F_{XTAL}	XOSC Crystal Frequency[13]	—	—	40	—	MHz
AFE Bypass Modes Only						
Single-Ended External Clock[14]						
$EXTAL_{clk}$	EXTAL external clock frequency			40		MHz
$V_{inxoscjit}$	EXTAL external clock Cycle to Cycle Jitter (RMS)	—	—	—	2.5[15]	ps
$V_{inxoscclkvil}$	EXTAL external clock input low voltage	—	0	—	0.4	V
$V_{inxoscclkvih}$	EXTAL external clock input high voltage	—	1	—	1.23	V
t_r/t_f	Rise/fall time of EXTAL external clock input				1	ns
t_{dc}	Duty Cycle of EXTAL external clock input		47	50	53	%
Differential LVDS External Clock						
$LVDS_{clk}$	LVDS external clock frequency			40		MHz
$LVDSV_{inxoscclk}$	LVDS external clock input voltage		0		1.36	V
$LVDSV_{inxoscclk(p-p)}$	LVDS external clock input voltage (peak-peak)	Voltage driven, AC coupled Differential	0.45	0.70	1.12	V
$LVDSI_{inxoscclk}$	LVDS external clock input current	Current driven, DC coupled.	3.0	3.5	4.0	mA
$LVDSV_{inxoscjit}$	LVDS external clock Jitter (RMS) [15]				2.5	ps
t_r/t_f	Rise/fall time of LVDS external clock input	20% - 80%			1.5	ns
t_{dcLVDS}	Duty Cycle of LVDS external clock input		47	50	53	%

1. Full functionality cannot be guaranteed when voltages are out of the recommended operating conditions.
2. Min voltage takes into account the LVD variation.
3. Max voltage takes into account HVD variation.
4. Aurora supply must connect to core supply voltage at board level.
5. The ground connection for the $V_{DD\_HV\_FLA}$ is shared with V_{SS}.
6. Supply range does not take into account HVD levels. Full range can be achieved after power-up, if HVD is disabled. See Voltage regulator electrical characteristics section for details.
7. Around common mode voltage of 0.7 V. Input voltage cannot exceed 1.4 V prior to AFE start-up completion (VREF and VREGs on and LVDs cleared).
8. SDADC input voltage full scale is 1.2 Vpp
9. On channels shared between ADC0 and 1, $V_{DD\_HV\_ADCREFx}$ is the lower of $V_{DD\_HV\_ADCREF0/1}$.
10. $V_{DD\_LV\_DPHY}$ supply should be shorted to core supply voltage VDD on board. Refer to AN5251. Contact your NXP sales representative for details.

11. While determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is critical that the junction temperature specification is not exceeded under any condition.
12. Full performance means Core0 running @ 120 MHz, Core1/2 running @ 240 MHz, SPT running @ 200 MHz, rich set of peripherals used.
13. Recommended Crystal 40 MHz (ESR≤30 Ω), 8 pF load capacitance.
14. External mode can be used as differential input with EXTAL and XTAL
15. The number is 3.5 ps when SD-ADC and/or DAC is not used in the device.

4.3 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

Table 8. Current consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD_CORE}	Core current in run mode	All cores at max frequency. 1.31 V. Tj = 150°C	-	-	1480[1]	mA
$I_{DD\_HV\_FLA}$	Flash operating current	Tj = 150°C. $V_{DD\_HV\_FLA}$ = 3.6 V	-	3[2]	40[3]	mA
$I_{DD\_LV\_AURORA}$	Aurora operating current	Tj = 150°C. $V_{DD\_LV\_AURORA}$ = 1.31 V. 4 TX lanes enabled.	-	-	60	mA
$I_{DD\_HV\_ADC}$	ADC operating current	Tj = 150°C. $V_{DD\_HV\_ADC}$ = 3.6 V. 2 ADCs operating at 80 MHz.	-	2	5	mA
$I_{DD\_HV\_ADCREF}$	Reference current per ADC[4] Reference current per temp sensor[5]	Tj = 150°C. $V_{DD\_HV\_ADCREFx}$ = 3.6 V. ADC operating at 80 MHz.	- -	- -	1.5 0.75	mA
$I_{DD\_HV\_RAW}$	AFE SD and regulator operating current	Tj = 150°C. $V_{DD\_HV\_RAW}$ = 3.6 V. SD-PLL, AFE regulators and 4 SD enabled.	-	70[6]	75	mA
$I_{DD\_HV\_DAC}$	AFE DAC operating current	Tj = 150°C. $V_{DD\_HV\_DAC}$ = 3.6 V. DAC enabled.	-	10	15	mA
$I_{DD\_HV\_PMU}$	PMU operating current	Tj = 150°C. VDD_HV_PMU = 3.6 V. Internal regulation enabled.	-	2	10	mA
$I_{DD\_LV\_DPHY}$	MIPICSI2 DPHY operating current in HS-RX mode	Tj = 150°C, $V_{DD\_LV\_DPHY}$ =1.31 V	-	14.9	23.2	mA

1. Strong dependence on use case, cache usage.
2. Measured during flash read.
3. Peak Flash current measured during read while write (RWW) operation.
4. ADC0 and 1 on ADCREF0/1.
5. Temp sensor current when PMC_CTL_TD[TSx_AOUT_EN] = 1. TS0 on ADCREF0/1.
6. Typical number is approximately 10 mA per each SD-ADC enabled, 12 mA for SD-PLL and 15 mA for the AFE regulators.

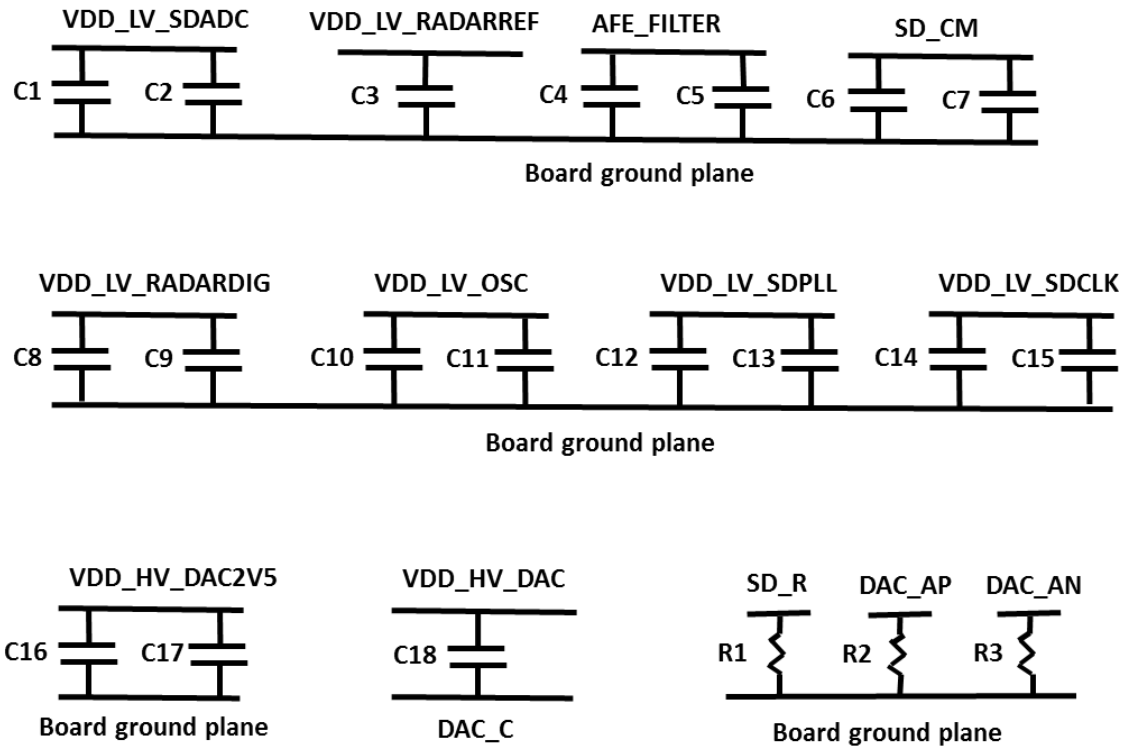

Figure 3. Radar AFE External Components Configuration

Table 11. Radar AFE External Components

Component	Component Value	Tolerance	Placement Priority of larger cap. [1]	Placement Priority of smaller cap[1]	Special notes
C1	0.47 µF	±35%	3	—	—
C2	0.1 µF	±35%	—	1	—
C3	1.0 µF	±35%	7	—	—
C4	1.0 µF	±35%	2	—	—
C5	0.1 µF	±35%	—	4	—
C6	1.0 µF	±35%	8	—	—
C7	0.1 µF	±35%	—	6	—
C8	1.0 µF	±35%	6	—	—
C9	0.1 µF	±35%	—	5	—
C10	1.0 µF	±35%	4	—	—
C11	0.1 µF	±35%	—	2	—
C12	1.0 µF	±35%	5	—	—
C13	0.1 µF	±35%	—	3	—
C14	1.0 µF	±35%	10	—	—
C15	0.1 µF	±35%	—	8	—
C16	1.0 µF	±35%	9	—	—
C17	0.1µF	±35%	—	7	—

Table continues on the next page...

Table 12. ESD ratings (continued)

No.	Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
			conforming to AEC-Q100-002			
2	$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500[3] 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.
3. 500 V for non-AFE pins, 250 V for AFE pins.

5 I/O Parameters

5.1 I/O pad DC electrical characteristics

NMI, TCK, TMS, JCOMP are treated as GPIO.

Table 13. I/O pad DC electrical specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65*$V_{DD\_HV\_IO}$	$V_{DD\_HV\_IO}$ + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	-0.3	0.35*$V_{DD\_HV\_IO}$	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 * $V_{DD\_HV\_IO}$	$V_{DD\_HV\_IO}$ + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	-0.3	0.40 * $V_{DD\_HV\_IO}$	V
Vhys	CMOS Input Buffer Hysteresis	0.1 * $V_{DD\_HV\_IO}$	—	V
Vih_{TTL}	TTL Input high level voltage (All SAR_ADC input pins)	2	$V_{DD\_HV\_ADCREFx}$ + 0.3	V
Vil_{TTL}	TTL Input low level voltage (All SAR_ADC input pins)	-0.3	0.56	V
$Vhyst_{TTL}$	TTL Input hysteresis voltage (All SAR_ADC input pins)	0.3	—	V
Pull_Ioh	Weak Pullup Current[1]	10	55	µA
Pull_Iol	Weak Pulldown Current[2]	10	55	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[3]	0.8 * $V_{DD\_HV\_IO}$	—	V
Vol	Output Low Voltage[4]	—	0.2 * $V_{DD\_HV\_IO}$	V
Ioh_f	Full drive Ioh[5] (ipp_sre[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol[5] (ipp_sre[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh[5] (ipp_sre[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol[5] (ipp_sre[1:0] = 10)	10.5	60	mA

Table 17. Aurora LVDS driver electrical characteristics (continued)

Symbol	Parameter[1]	Value			Unit
		Min	Typ	Max	
R_{V_L}	Terminating Resistance (external)	99	100	101	Ohms
C_P	Parasitic Capacitance (pad + bondwire + pin)			1	pF
L_P	Parasitic Inductance			7	nH
STARTUP					
T_{STRT_BIAS}	Bias startup time	—	—	5	µs
T_{STRT_TX}	Transmitter startup time[2]	—	—	5	µs
T_{STRT_RX}	Receiver startup time[2]	—	—	5	µs
LVDS_RXOUT[3]	Receiver o/p duty cycle	30		70	%

1. Conditions for these values are $V_{DD\_LV\_IO\_AURORA}$ = 1.19V to 1.32V, T_J = –40 / 150 °C
2. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
3. Receiver o/p duty cycle is measured with 1.25 Gbps, 50% duty cycle, max 1 ns rise/fall time, 100 mV voltage swing signal applied at the receiver input.

5.4 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET_B pin.

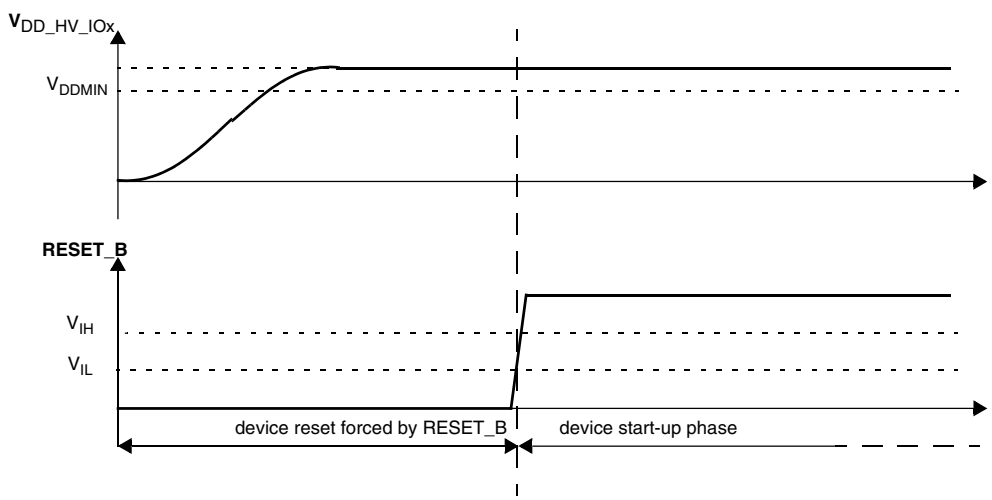

Figure 4. Start-up reset requirements

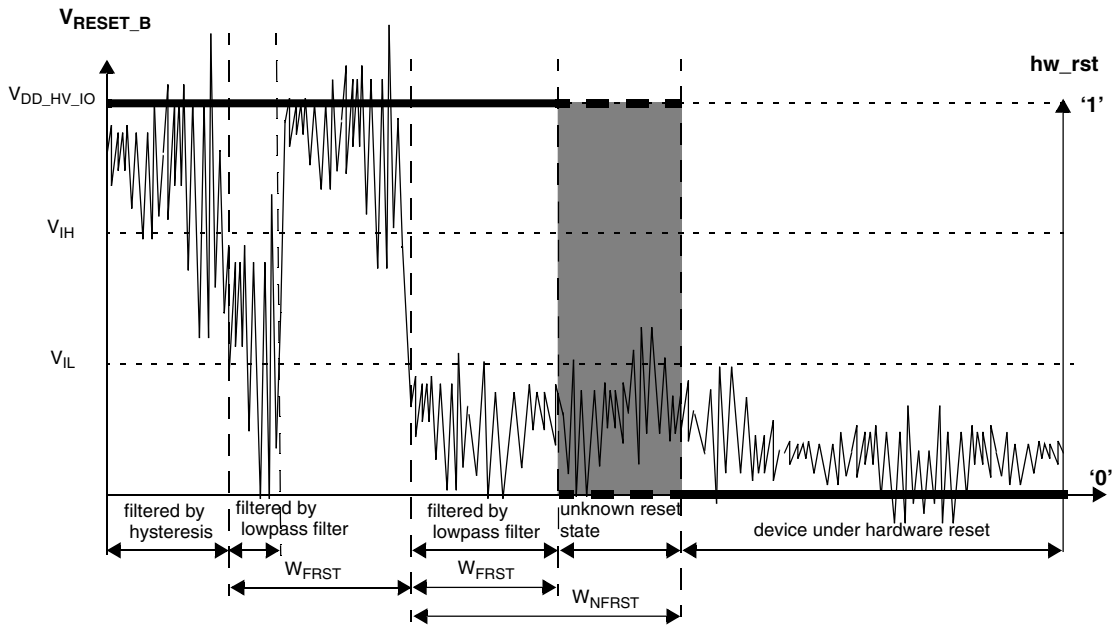

Figure 5. Noise filtering on reset signal

Table 18. RESET_B electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level TTL (Schmitt Trigger)	—	2.0	—	$V_{DD\_HV\_IOx}$ + 0.4	V
V_{IL}	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.56	V
V_{HYS}[2]	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV
I_{OL_R}	Strong pull-down current	Device under power-on reset $V_{DD\_HV\_IO}$ = 1.2 V V_{OL} = 0.35 x $V_{DD\_HV\_IO}$	0.2	—	—	mA
		Device under power-on reset $V_{DD\_HV\_IO}$=3.0 V V_{OL} = 0.35 x $V_{DD\_HV\_IO}$	15	—	—	mA
W_{FRST}	RESET_B input filtered pulse	—	—	—	500	ns
W_{NFRST}	RESET_B input not filtered pulse	—	2400	—	—	ns
$\lvert I_{WPD} \rvert$	Weak pull-down current absolute value	V_{IN} = $V_{DD\_HV\_IOx}$	30	—	100	µA

1. $V_{DD\_HV\_IOx}$ = 3.3 V -5%,+10%, T_J = –40 / 150°C, unless otherwise specified.
2. Data based on characterization results, not tested in production.

7. DAC PSRR is 30 dB minimum for DAC output levels of 1/3 of full-scale or less. DAC PSRR is 24 dB minimum with the DAC output at full-scale.

8 Memory modules

8.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 28 shows the estimated Program/Erase times.

Table 28. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

Table 32. Flash read wait state and address pipeline control guidelines (continued)

Operating Frequency (fsys = SYS_CLK)	RWSC	APC	Flash read latency on min-cache miss (# of fcpu clock periods)	Flash read latency on mini-cache hit (# of fcpu clock periods)
33 MHz < fsys <= 100 MHz	2	1	5	1
100 MHz < fsys <= 120 MHz	3	1	6	1

9 Communication modules

9.1 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

9.1.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

- Measurements are with input transition of 1 ns and output load of 25 pF.

Table 33. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

9.2.4 Receiver asymmetry

Table 40. Receiver asymmetry

Name	Description	Min	Max	Unit
$dCCRxAsymAccept_{15}$	Acceptance of asymmetry at receiving CC with 15 pF load (*)	–31.5	+44.0	ns
$dCCRxAsymAccept_{25}$	Acceptance of asymmetry at receiving CC with 25 pF load (*)	–30.5	+43.0	ns

9.3 LVDS Fast Asynchronous Transmission (LFAST) electrical characteristics

The following table provides output driver characteristics for LFAST I/Os.

Table 41. LFAST output buffer electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
$\lvert\Delta_{VO\_L}\rvert$	Absolute value for differential output voltage swing (terminated)	—	100	200	285	mV
V_{ICOM_L}	Common mode voltage	—	1.08	1.2	1.32	V
T_{tr_L}	Transition time output pin LVDS configuration	—	0.2	—	1.5	ns

1. $V_{DD\_HV\_IOx}$ = 3.3 V (–5%, +10%), T_J = –40 / 150 °C, unless otherwise specified.

NOTE

Fast IOs must be specified only as fast (and not as high current). See GPIO DC electrical specification.

9.3.1 LFAST interface timing diagrams

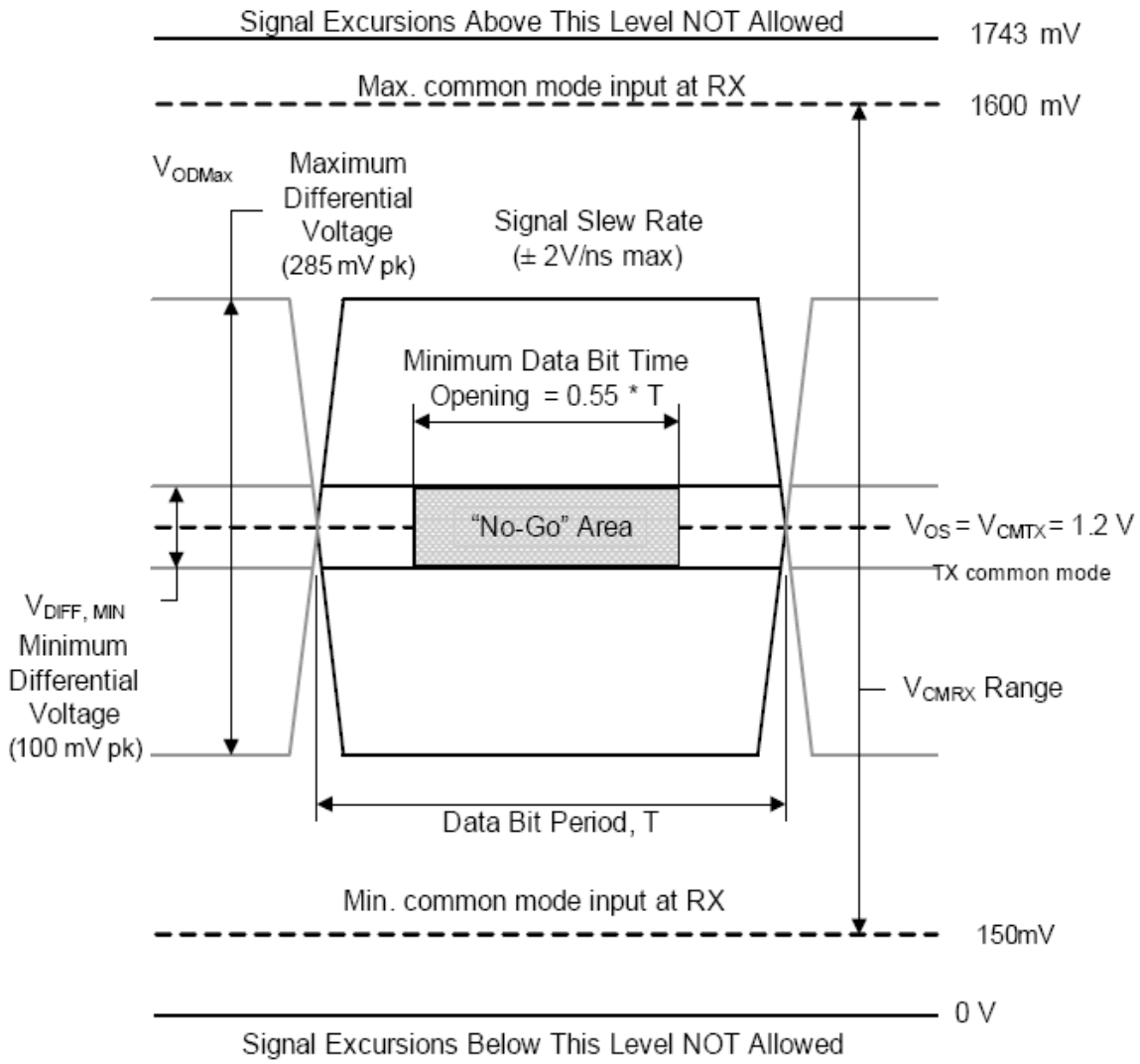

Figure 21. LFAST timing definition

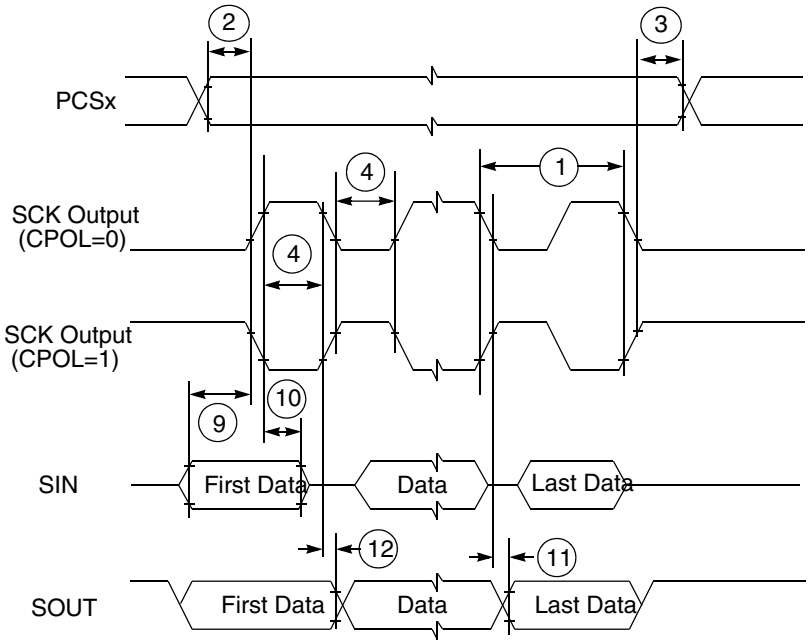

Figure 24. SPI classic SPI timing — master, CPHA = 0

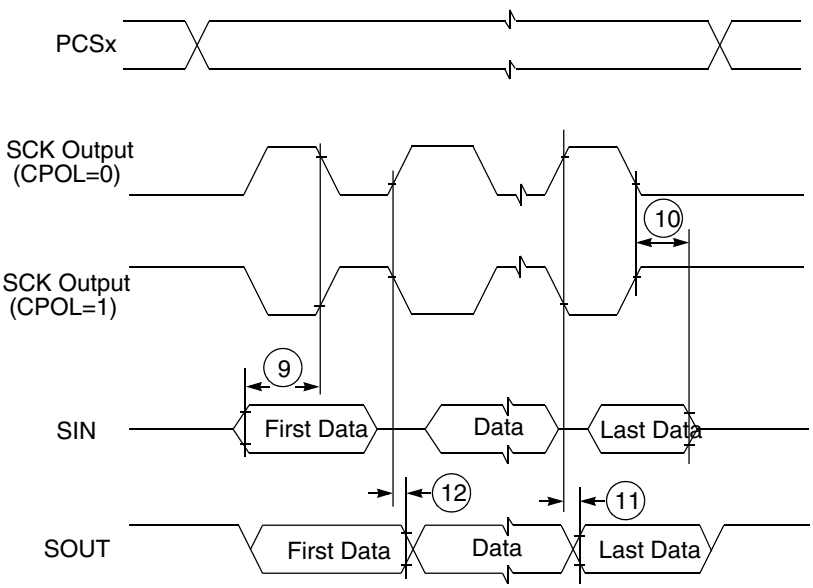

Figure 25. SPI classic SPI timing — master, CPHA = 1

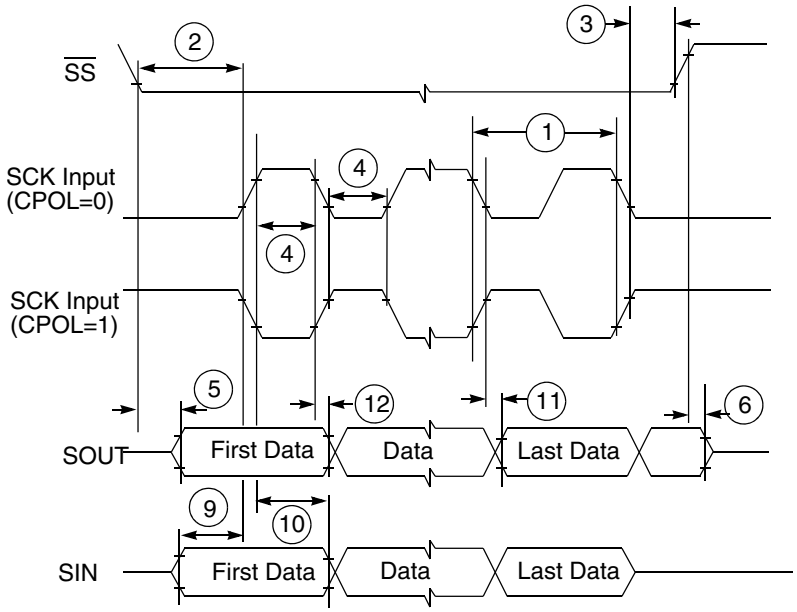

Figure 26. SPI classic SPI timing — slave, CPHA = 0

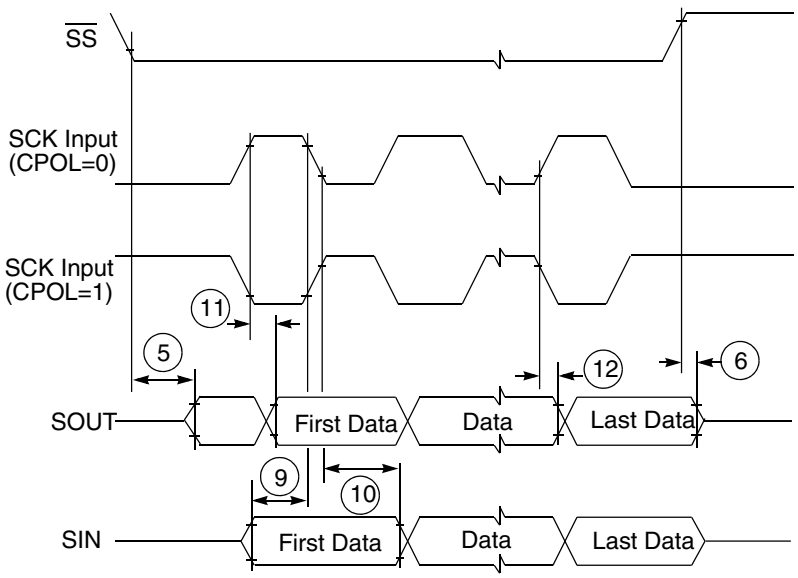

Figure 27. SPI classic SPI timing — slave, CPHA = 1

9.5 LINFlexD timing specifications

The maximum bit rate is 1.875 MBit/s.

9.6 I²C timing

Table 44. I²C SCL and SDA input timing specifications

Number	Symbol	Parameter	Value		Unit
			Min	Max	
1	I_tHD:STA	Start Condition hold time	2	-	Peripheral clock
2	I_t_LOW	Clock low time	8	-	
3	I_tHD:DAT	Data hold time	2	-	
4	I_tHIGH	Clock high time	4	-	
5	I_tSU:DAT	Data setup time	4	-	
6	I_tSU:STA	Start condition setup time (for repeated start condition only)	2	-	
7	I_tSU:STOP	Stop condition setup time	2	-	

Table 45. I²C SCL and SDA output timing specifications

Number	Symbol	Parameter	Value		Unit
			Min	Max	
1	O_tHD:STA	Start condition hold time[1]	6	-	Peripheral clock
2	O_t_LOW	Clock low time[1]	10	-	
3	O_tHD:DAT	Data hold time[1]	7	-	
4	O_t_HIGH	Clock high time[1]	10	-	
5	O_tSU:DAT	Data setup time[1]	2	-	
6	O_tSU:STA	Start condition setup time (for repeated start condition only)[1]	20	-	
7	O_tSU:STOP	Stop condition setup time[1]	10	-	
8	O_tr	SCL/SDA rise time[2]	-	99.6	ns
9	O_tf	SCL/SDA fall time[1]	-	99.6	

1. Programming IBFD (I²C Bus Frequency Divider Register) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IBDR (I²C Bus Data I/O Register).
2. Serial data (SDA) and Serial clock (SCL) reaches peak level depending upon the external signal capacitance and pull up resistor values as SDA and SCL are open-drain type outputs which are only actively driven low by the I²C module.

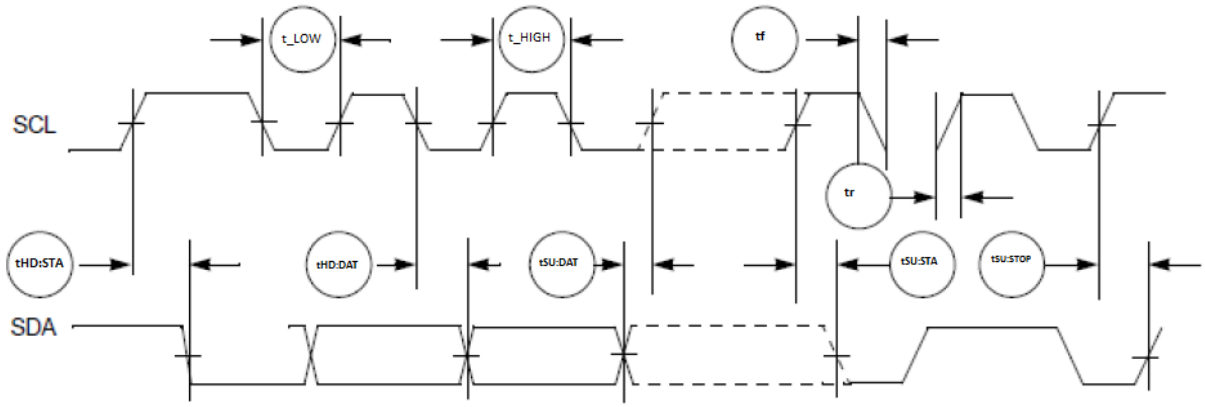

Figure 31. I²C input/output timing

10 Debug modules

10.1 JTAG/CJTAG interface timing

The following table lists JTAGC/CJTAG electrical characteristics.

- Measurements are with input transition of 1 ns, output load of 50 pF and pads configured with SRE=11.

Table 46. JTAG/CJTAG pin AC electrical characteristics [1]

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}[2]	TCK Cycle Time (JTAG)	36	—	ns
		TCK Cycle Time (CJTAG)	50		
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO/TMS Data Valid [3]	—	15[4]	ns
7	t_{TDOI}	TCK Low to TDO/TMS Data Invalid[3]	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO/TMS High Impedance[3]	—	22	ns
9	t_{JCMPPW}	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600[5]	ns
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns

Table continues on the next page...

12 External interrupt timing (IRQ pin)

Table 49. External interrupt timing

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time[1]	—	6	—	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both

NOTE

tCYC is equivalent to TCK (prescaled filter clock period) which is the IRC clock prescaled to the Interrupt Filter Clock Prescaler (IFCP) value. TCK = T(IRC) x (IFCP + 1) where T(IRC) is the internal oscillator period. Refer SIUL2 chapter of the device reference manual for details.

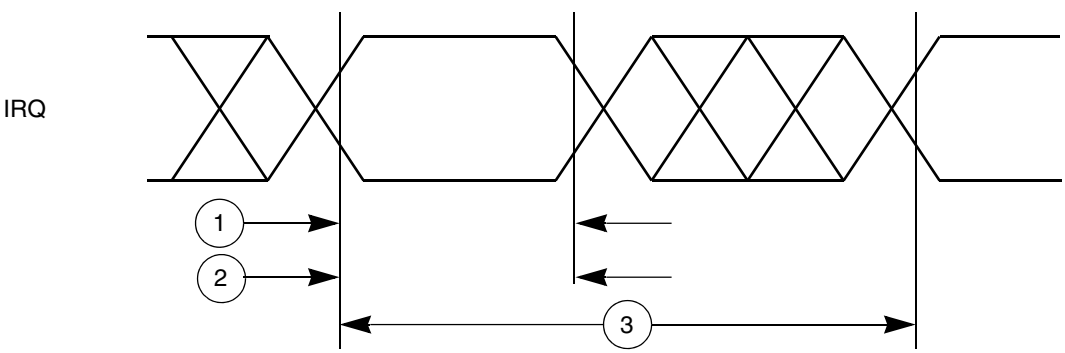

Figure 37. External interrupt timing

13 Temperature sensor electrical characteristics

The following table describes the temperature sensor electrical characteristics.

Table 50. Temperature sensor electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
—	Temperature monitoring range		-40	—	150	°C
T_{SENS}	Sensitivity		—	5.18	—	mV/°C
T_{ACC}	Accuracy	T_J = -40 to 150°C	5	—	5	°C

Table 53. D-PHY switching characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔVCMRX(HF)	Common mode interference beyond 450 MHz		-	-	100	mVpp
ΔVCMRX(LF)	Common mode interference between 50 MHz and 450 MHz		-50	-	50	mVpp
CCM	Common mode termination		-	-	60	pF
LP Line Receiver AC Specification						
e_{SPIKE}	Input pulse rejection		-	-	300	Vps
T_{MIN}	Minimum pulse response		20	-	-	ns
V_{INT}	Pk-to-Pk interference voltage		-	-	200	mV
f_{INT}	Interference frequency		450	-	-	MHz

14.1.4 Low-power receiver timing

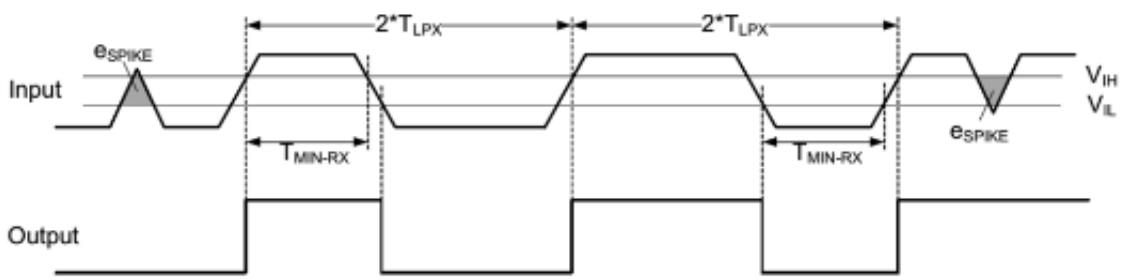

Figure 40. Input Glitch Rejection of Low-Power Receivers

15 Thermal Specifications

15.1 Thermal characteristics

Table 55. 257MAPBGA package thermal characteristics

Symbol	Parameter	Conditions	257MAPBGA	Unit
$R_{\theta JA}$	Thermal resistance, junction-to-ambient natural convection [1, 2]	Single layer board - 1s	41.8	°C/W
		Four layer board - 2s2p[3]	22.3	
$R_{\theta JMA}$	Thermal resistance, junction-to-ambient forced convection at 200 ft/min[1, 3]	Single layer board - 1s	29.8	°C/W
		Four layer board - 2s2p	17.7	
$R_{\theta JB}$	Thermal resistance junction-to-board[4]	—	7.6	°C/W
$R_{\theta JC}$	Thermal resistance junction-to-case[5]	—	5.2	°C/W
Ψ_{JT}	Junction-to-package-top natural convection[6]	—	0.2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

15.1.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

$$T_J = T_{BRD} + (R_{\theta JB} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JB}$ = junction to board thermal resistance (°C/W)
- $T_{\theta BRD}$ = average board temperature just outside the package periphery (°C)
- P_D = power dissipation in the package (W)

be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in Table 57 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

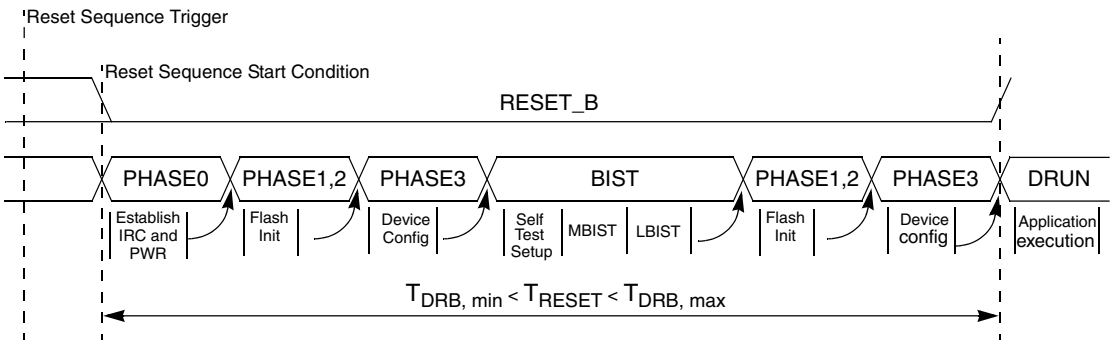

Figure 42. Destructive reset sequence, BIST enabled

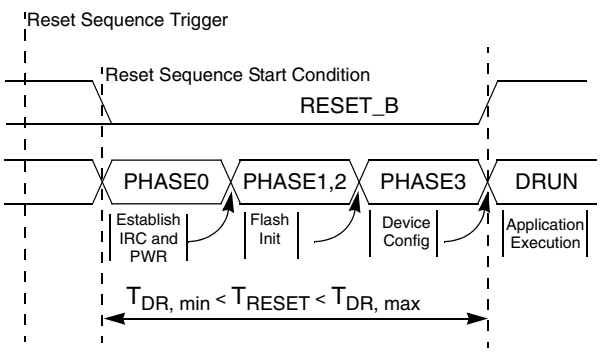

Figure 43. Destructive reset sequence, BIST disabled

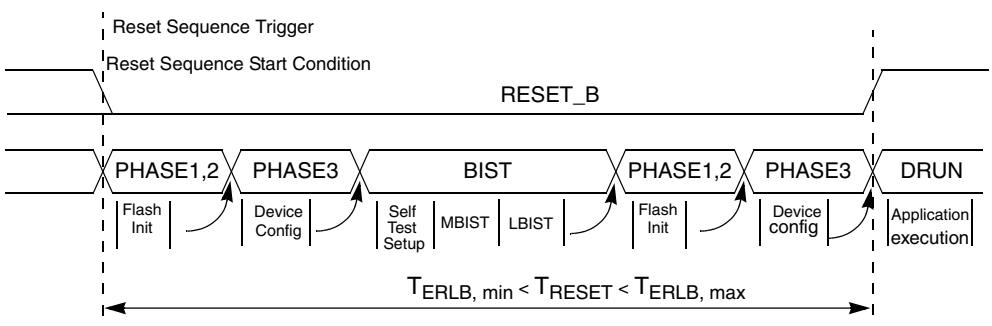

Figure 44. External reset sequence long, BIST enabled

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