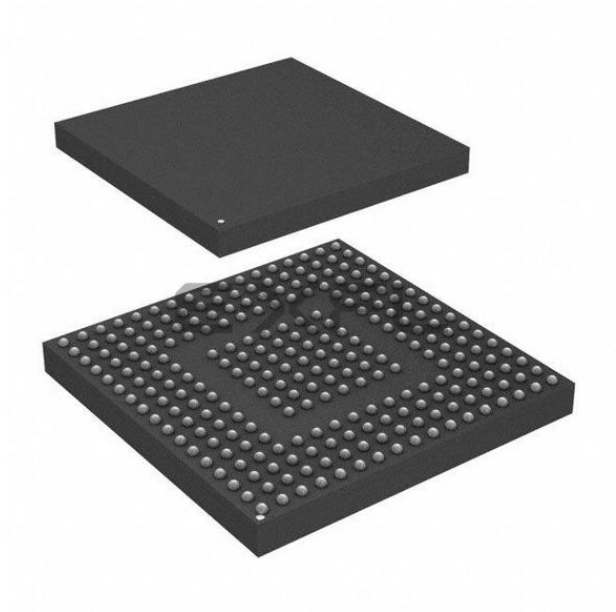

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4, e200z7 (2)
Core Size	32-Bit Tri-Core
Speed	180MHz, 240MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI, ZipWire
Peripherals	POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	1.5M x 8
Voltage - Supply (Vcc/Vdd)	1.19V ~ 5.5V
Data Converters	A/D 16x12b SAR, 4x12 Sigma; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32r274ksk2mmmr

    - 16 MHz Internal oscillator (IRCOSC)
    - Dual system PLL with one frequency modulated phase-locked loop (FMPLL)
    - Low-jitter PLL to ΣΔ-ADC and DAC clock generation
- Functional Safety
    - Enables up to ASIL-D applications
    - End to end ECC ensuring full protection of all data accesses throughout the system, from each of the systems masters through the crossbar and into the memories and peripherals
    - FCCU for fault collection and fault handling
    - MEMU for memory error management
    - Safe eDMA controller
    - User selectable Memory BIST (MBIST) can be enabled to run out of various reset conditions or during runtime
    - Self-Test Control Unit (STCU2)
    - Error Injection Module (EIM)
    - On-chip voltage monitoring
    - Clock Monitor Unit (CMU) to support monitoring of critical clocks
- Security
    - Cryptographic Security Engine (CSE2) enabling advanced security management
    - Supports censorship and life-cycle management via Password and Device Security (PASS) module
    - Diary control for tamper detection (TDM)
- Support Modules
    - Global Interrupt controller (INTC) capable of routing interrupts to any CPU
    - Semaphore unit to manage access to shared resources
    - Two CRC computation units with four polynomials
    - 32-channel eDMA controller with multiple transfer request sources using DMAMUX
    - Boot Assist Module (BAM) supports internal flash programming via a serial link (LIN / CAN)
- Timers
    - Two Periodic Interval Timers (PIT) with 32-bit counter resolution
    - Three System Timer Module (STM)
    - Three Software Watchdog Timers (SWT)
    - Two eTimer modules with 6 channels each
    - One FlexPWM module for 12 PWM signals
- Communication Interfaces
    - Two Serial Peripheral interface (SPI) module
    - Two inter-IC communication interface (I2C) modules
    - One LINFlexD module
    - One dual-channel FlexRay module with 128 message buffers

11. While determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is critical that the junction temperature specification is not exceeded under any condition.
12. Full performance means Core0 running @ 120 MHz, Core1/2 running @ 240 MHz, SPT running @ 200 MHz, rich set of peripherals used.
13. Recommended Crystal 40 MHz (ESR≤30 Ω), 8 pF load capacitance.
14. External mode can be used as differential input with EXTAL and XTAL
15. The number is 3.5 ps when SD-ADC and/or DAC is not used in the device.

4.3 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

Table 8. Current consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD_CORE}	Core current in run mode	All cores at max frequency. 1.31 V. Tj = 150°C	-	-	1480[1]	mA
$I_{DD\_HV\_FLA}$	Flash operating current	Tj = 150°C. $V_{DD\_HV\_FLA}$ = 3.6 V	-	3[2]	40[3]	mA
$I_{DD\_LV\_AURORA}$	Aurora operating current	Tj = 150°C. $V_{DD\_LV\_AURORA}$ = 1.31 V. 4 TX lanes enabled.	-	-	60	mA
$I_{DD\_HV\_ADC}$	ADC operating current	Tj = 150°C. $V_{DD\_HV\_ADC}$ = 3.6 V. 2 ADCs operating at 80 MHz.	-	2	5	mA
$I_{DD\_HV\_ADCREF}$	Reference current per ADC[4] Reference current per temp sensor[5]	Tj = 150°C. $V_{DD\_HV\_ADCREFx}$ = 3.6 V. ADC operating at 80 MHz.	- -	- -	1.5 0.75	mA
$I_{DD\_HV\_RAW}$	AFE SD and regulator operating current	Tj = 150°C. $V_{DD\_HV\_RAW}$ = 3.6 V. SD-PLL, AFE regulators and 4 SD enabled.	-	70[6]	75	mA
$I_{DD\_HV\_DAC}$	AFE DAC operating current	Tj = 150°C. $V_{DD\_HV\_DAC}$ = 3.6 V. DAC enabled.	-	10	15	mA
$I_{DD\_HV\_PMU}$	PMU operating current	Tj = 150°C. VDD_HV_PMU = 3.6 V. Internal regulation enabled.	-	2	10	mA
$I_{DD\_LV\_DPHY}$	MIPICSI2 DPHY operating current in HS-RX mode	Tj = 150°C, $V_{DD\_LV\_DPHY}$ =1.31 V	-	14.9	23.2	mA

1. Strong dependence on use case, cache usage.
2. Measured during flash read.
3. Peak Flash current measured during read while write (RWW) operation.
4. ADC0 and 1 on ADCREF0/1.
5. Temp sensor current when PMC_CTL_TD[TSx_AOUT_EN] = 1. TS0 on ADCREF0/1.
6. Typical number is approximately 10 mA per each SD-ADC enabled, 12 mA for SD-PLL and 15 mA for the AFE regulators.

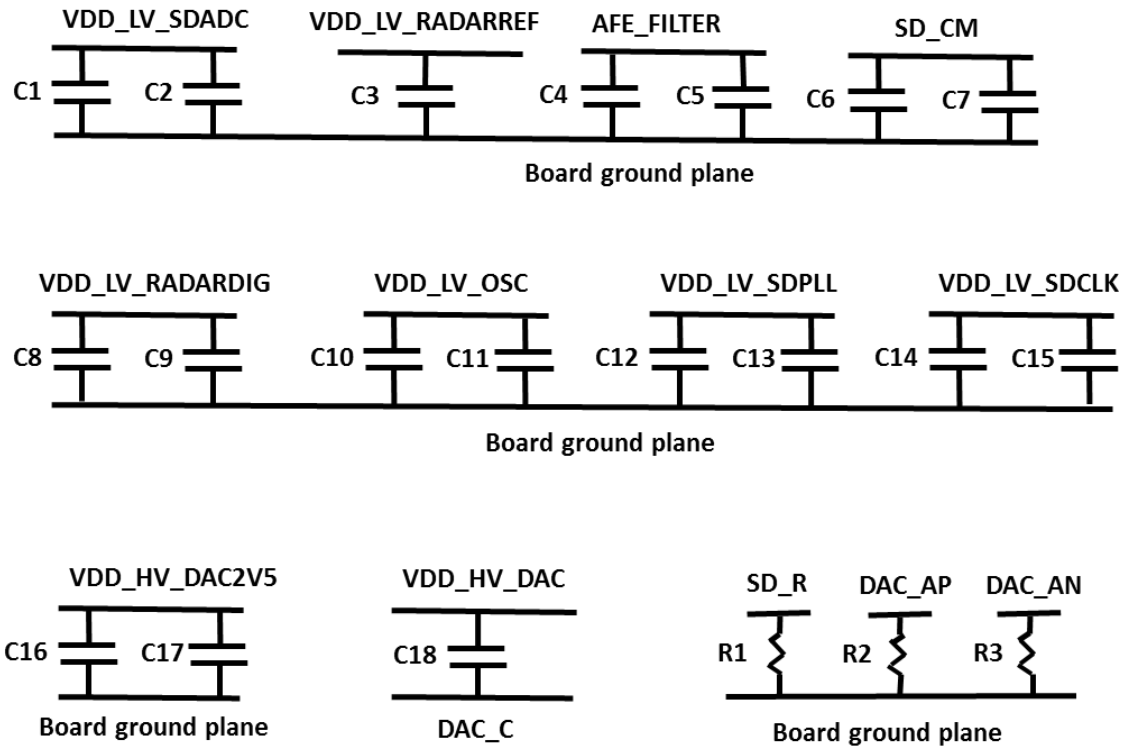

Figure 3. Radar AFE External Components Configuration

Table 11. Radar AFE External Components

Component	Component Value	Tolerance	Placement Priority of larger cap. [1]	Placement Priority of smaller cap[1]	Special notes
C1	0.47 µF	±35%	3	—	—
C2	0.1 µF	±35%	—	1	—
C3	1.0 µF	±35%	7	—	—
C4	1.0 µF	±35%	2	—	—
C5	0.1 µF	±35%	—	4	—
C6	1.0 µF	±35%	8	—	—
C7	0.1 µF	±35%	—	6	—
C8	1.0 µF	±35%	6	—	—
C9	0.1 µF	±35%	—	5	—
C10	1.0 µF	±35%	4	—	—
C11	0.1 µF	±35%	—	2	—
C12	1.0 µF	±35%	5	—	—
C13	0.1 µF	±35%	—	3	—
C14	1.0 µF	±35%	10	—	—
C15	0.1 µF	±35%	—	8	—
C16	1.0 µF	±35%	9	—	—
C17	0.1µF	±35%	—	7	—

Table continues on the next page...

Table 12. ESD ratings (continued)

No.	Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
			conforming to AEC-Q100-002			
2	$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500[3] 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.
3. 500 V for non-AFE pins, 250 V for AFE pins.

5 I/O Parameters

5.1 I/O pad DC electrical characteristics

NMI, TCK, TMS, JCOMP are treated as GPIO.

Table 13. I/O pad DC electrical specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65*$V_{DD\_HV\_IO}$	$V_{DD\_HV\_IO}$ + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	-0.3	0.35*$V_{DD\_HV\_IO}$	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 * $V_{DD\_HV\_IO}$	$V_{DD\_HV\_IO}$ + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	-0.3	0.40 * $V_{DD\_HV\_IO}$	V
Vhys	CMOS Input Buffer Hysteresis	0.1 * $V_{DD\_HV\_IO}$	—	V
Vih_{TTL}	TTL Input high level voltage (All SAR_ADC input pins)	2	$V_{DD\_HV\_ADCREFx}$ + 0.3	V
Vil_{TTL}	TTL Input low level voltage (All SAR_ADC input pins)	-0.3	0.56	V
$Vhyst_{TTL}$	TTL Input hysteresis voltage (All SAR_ADC input pins)	0.3	—	V
Pull_Ioh	Weak Pullup Current[1]	10	55	µA
Pull_Iol	Weak Pulldown Current[2]	10	55	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[3]	0.8 * $V_{DD\_HV\_IO}$	—	V
Vol	Output Low Voltage[4]	—	0.2 * $V_{DD\_HV\_IO}$	V
Ioh_f	Full drive Ioh[5] (ipp_sre[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol[5] (ipp_sre[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh[5] (ipp_sre[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol[5] (ipp_sre[1:0] = 10)	10.5	60	mA

6.1.3 16 MHz Internal RC Oscillator (IRCOSC) electrical specifications

Table 22. Internal RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{Target}	IRC target frequency	—	—	16	—	MHz
$F_{untrimmed}$	IRC frequency (untrimmed)	—	9.6	—	24	MHz
δF_{var}	IRC trimmed frequency variation [1]	—	-8	—	8	%
$T_{startup}$	Startup time		—	—	5	µs

1. The typical user trim step size (δf_{TRIM}) is 0.3% of current frequency for application of positive trim and 0.26% of current frequency for application of negative trim, based on characterization results.

6.1.4 320 MHz AFE PLL electrical characteristics

Table 23. 320 MHz AFE PLL parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLL_{fout}	Output Frequency	—	—	320	—	MHz
PLL_{fin}	Input Frequency	—	—	—	40	MHz
t_{cal}	Calibration Time [1]	LW64 = 1 LW64 = 0	—	—	150 500	µs
t_{lock}	Lock Time	after calibration	—	—	75	µs
t_{jitcck}	Cycle to cycle jitter (peak – peak)	—	—	—	10	ps
—	Output duty cycle	—	48	50	52	%

1. The LW64 bit sets the wait time before the PLL frequency is measured after each calibration step to allow for stabilization. If LW64 is '0', wait time of 256 reference clock cycles is used. If LW64 is'1', wait time of 64 reference clock cycles is used.

6.1.5 LFAST PLL electrical characteristics

The specifications in the following table apply to the interprocessor bus LFAST interface.

Table 24. LFAST PLL electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{RF_REF}	PLL reference clock frequency	—	10	—	26	MHz
ERR_{REF}	PLL reference clock frequency error	—	–1	—	1	%
DC_{REF}	PLL reference clock duty cycle	—	45	—	55	%
f_{VCO}	PLL VCO frequency	—	—	640[1]	—	MHz
t_{LOCK}	PLL phase lock[2]	—	—	—	40	µs
ΔPER_{REF}	Input reference clock jitter (peak to peak)	Single period, f_{RF_REF} = 10 MHz	—	—	300	ps

Table continues on the next page...

Table 25. ADC conversion characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$TUE_{IS1WINJ}$	Total unadjusted error for IS1WINJ		–6	—	6	LSB
$TUE_{IS1WWINJ}$	Total unadjusted error for IS1WWINJ		–6	—	6	LSB
IS1WINJ (pad going to one ADC)	(single ADC channel)					
	Max leakage	150 °C	—	—	250	nA
	Max positive/negative injection		–3	—	3[8]	mA
IS1WWINJ (pad going to two ADCs)	(double ADC channel)					
	Max leakage	150 °C	—	—	300	nA
	Max positive/negative injection [7]	|Vref_ad0 - Vref_ad1| < 150 mV	–3.6	—	3.6	mA
SNR	Signal-to-noise ratio	3.3 V reference voltage	67	—	—	dB
THD	Total harmonic distortion	@ 50 KHz	65	—	—	dB
SINAD	Signal-to-noise and distortion	Fin < 50 KHz	6.02 x ENOB + 1.76			dB
ENOB	Effective number of bits	Fin < 50 KHz	10.5	—	—	bits

1. $V_{DD\_HV\_ADC}$ = 3.3 V -5%,+10%, T_J = –40 to +150°C, unless otherwise specified and analog input voltage from V_{AGND} to $V_{DD\_HV\_ADCREFx}$.
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. SeeInput equivalent circuit figure.
6. No missing codes.
7. ADC specifications are met only if injection is within these specified limits
8. Max injection current for all ADC IOs is ± 10 mA

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel. Aurora interface along with SAR-ADC would degrade SAR-ADC performance. General Purpose Input (GPI) functionality should not be used on any of the SAR-ADC channels when SARADC is functional.

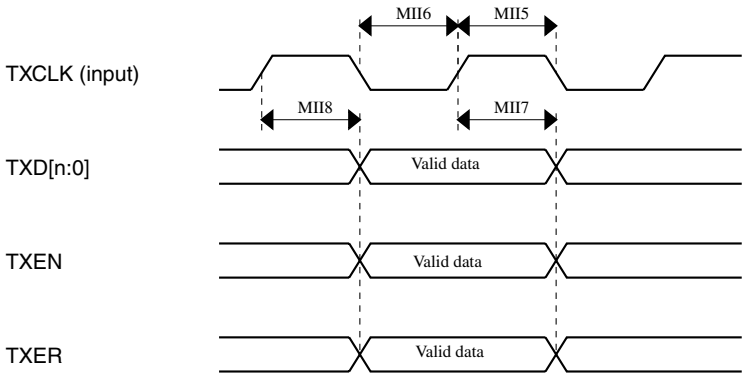

Figure 10. MII transmit signal timing diagram

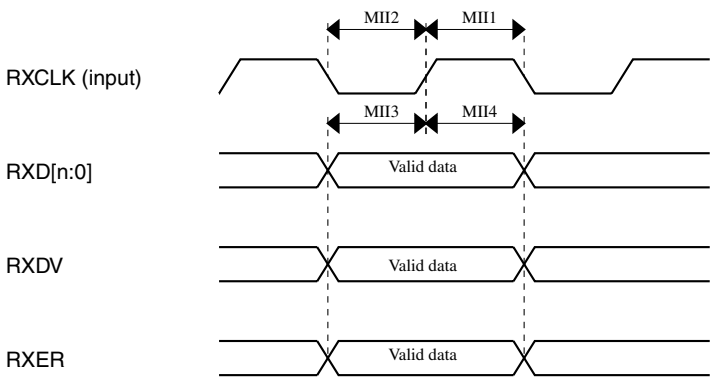

Figure 11. MII receive signal timing diagram

9.1.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

- Measurements are with input transition of 1 ns and output load of 25 pF.

Table 34. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns

Table continues on the next page...

9.1.4 MII/RMII Serial Management channel timing (MDC/MDIO)

The MDC/MDIO interface works at 3.3V compatible levels as mentioned in CMOS input (vih/vil/voh/vol/)values in I/O pad DC electrical characteristics .

Ethernet works with maximum frequency of MDC at 2.5 MHz. Output pads configured with SRC=11. MDIO pin must have external pull-up. Measurements are with input transition of 1.0 ns and output load of 50 pF.

Table 36. Ethernet MDIO timing table

Num	Description	Min.	Max.	Unit
MDC00	MDC clock frequency	—	2.5	MHz
MDC10	MDC falling edge to MDIO output invalid (minimum propagation delay)	(-0.8 + (ENET_MSCR[HOLDTIME] +1)*(PBRIDGE_n_CLK period in ns))	—	ns
MDC11	MDC falling edge to MDIO output valid (maximum propagation delay)	—	(13 + (ENET_MSCR[HOLDTIME] +1)*(PBRIDGE_n_CLK period in ns))	ns
MDC12	MDIO (input) to MDC rising edge setup	13	—	ns
MDC13	MDIO (input) to MDC rising edge hold	0	—	ns
MDC14	MDC pulse width high	40%	60%	MDC Period
MDC15	MDC pulse width low	40%	60%	MDC Period

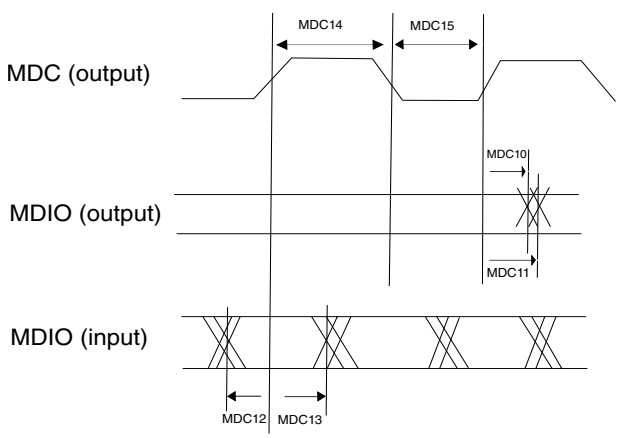

Figure 16. RMII/MII serial management channel timing diagram

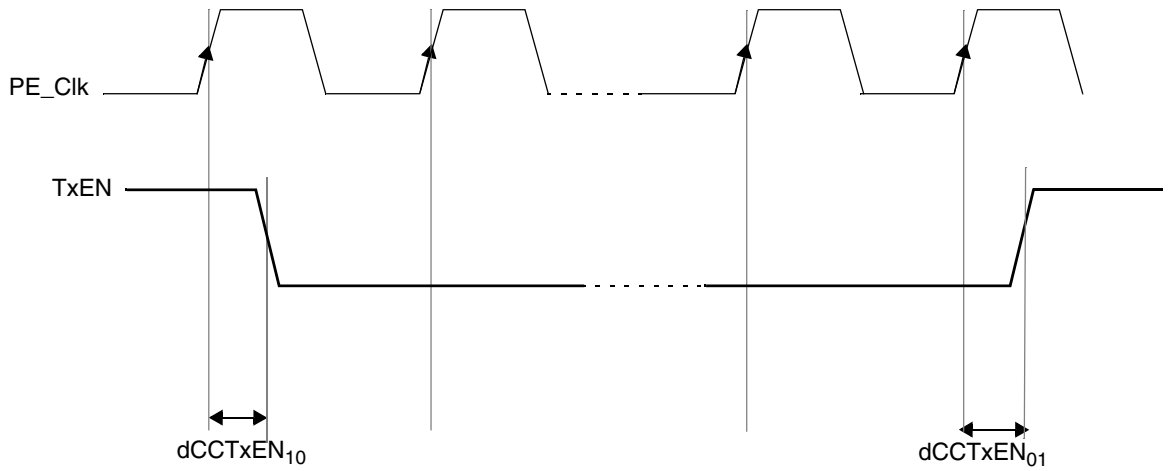

Figure 18. FlexRay TxEN signal propagation delays

9.2.2 TxD

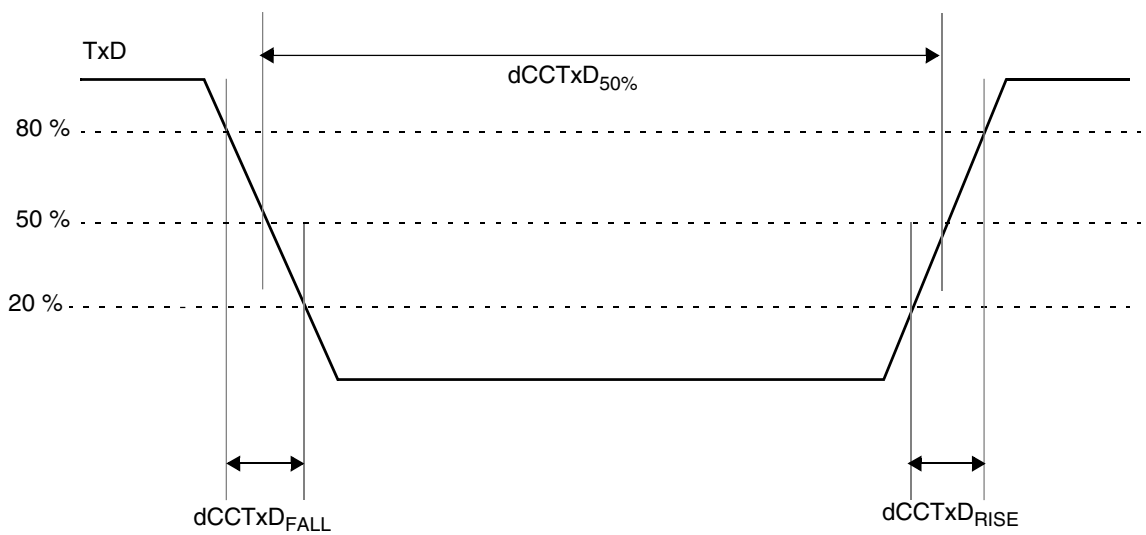

Figure 19. FlexRay TxD signal

- Measurements are with output load of 25 pF and pad configured as SRE =11.

Table 38. TxD output characteristics

Name	Description[1]	Min	Max	Unit
$dCCT_{xAsym}$	Asymmetry of sending CC @ 25 pF load	–2.45	2.45	ns

Table continues on the next page...

9.3.1 LFAST interface timing diagrams

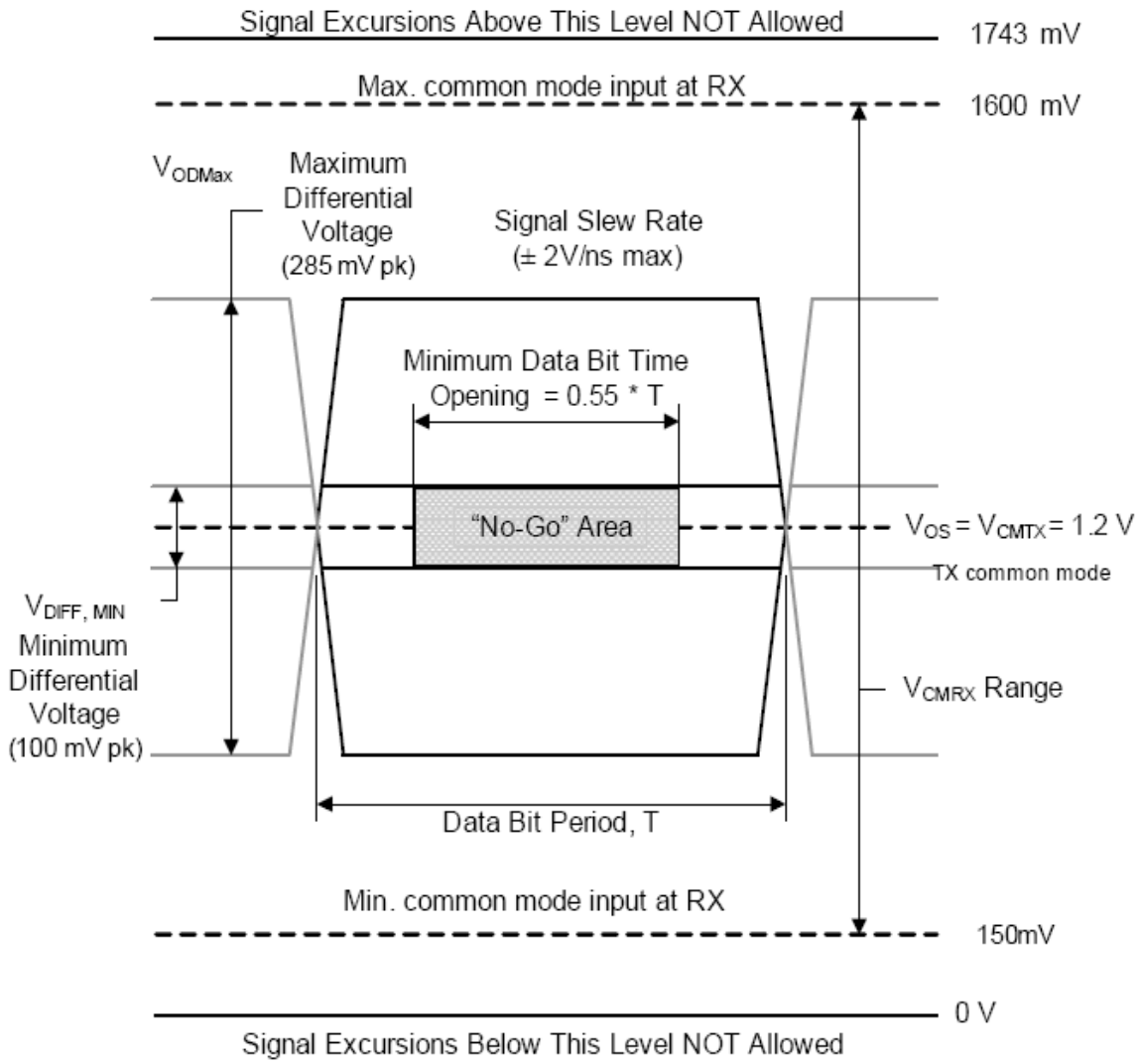

Figure 21. LFAST timing definition

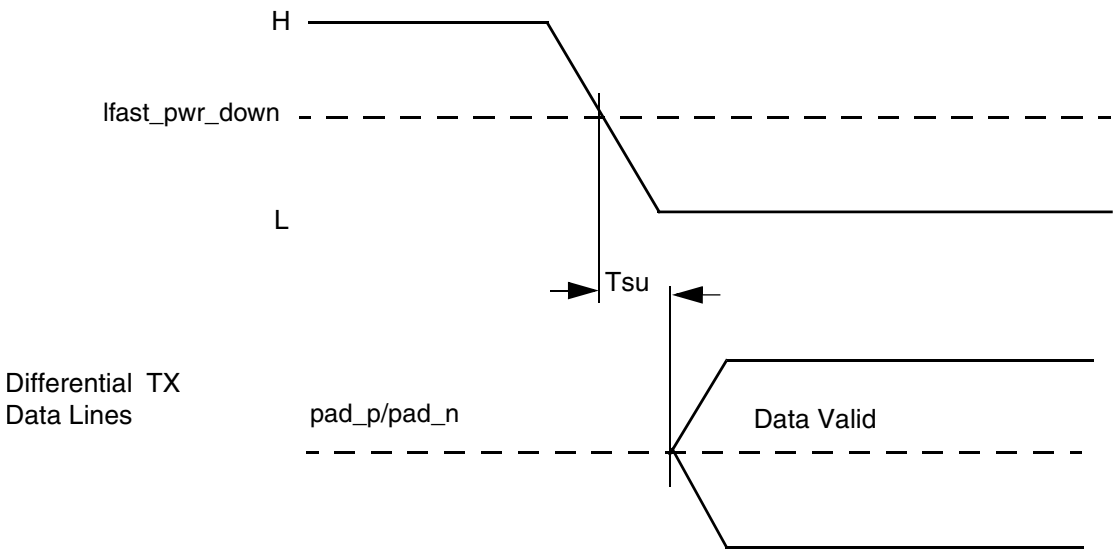

Figure 22. Power-down exit time

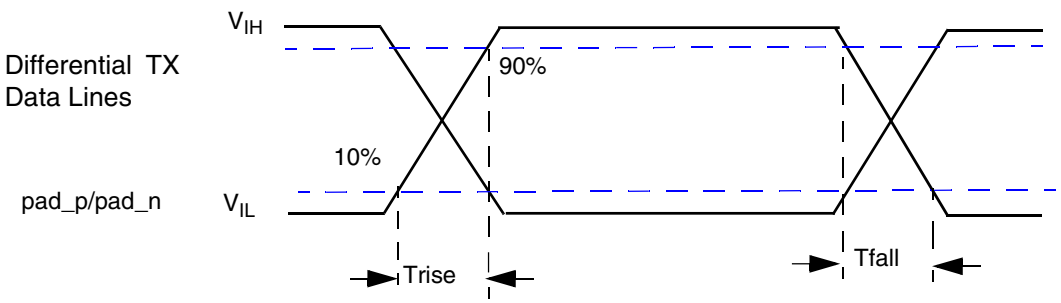

Figure 23. Rise/fall time

9.3.2 LFAST interface electrical characteristics

NOTE

While LFAST is operating and 'Ready' (nex_rdy_b) signal is used by the debugger on PAD_132, the recommended SRE settings are ‘00' and ‘01'. TCK should be used with low frequency (preferably less than 10 MHz).

Table 42. LFAST electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
Data Rate						
DATARATE	Data rate	—	—	312/320	Typ+0.1%	Mbps
STARTUP						
T_{STRT_BIAS}	Bias startup time[2]	—	—	0.5	3	µs

Table continues on the next page...

Table 43. SPI timing (continued)

No.	Symbol	Parameter	Conditions	Min	Max	Unit
			Master (MTFE = 1, CPHA = 0)[9]	-2 + N x SPI IPG clock period [10]	—	
			Master (MTFE = 1, CPHA = 1)	–2	—	
11	t_{SUO}	Data valid (after SCK edge)	Master (MTFE = 0)	—	7 [11]	ns
			Slave	—	23	
			Master (MTFE = 1, CPHA = 0)[12]	—	7 + SPI IPG Clock Period	
			Master (MTFE = 1, CPHA = 1)	—	7	
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	–4 [11]	—	ns
			Slave	3.8	—	
			Master (MTFE = 1, CPHA = 0) [12]	-4 + SPI IPG Clock Period	—	
			Master (MTFE = 1, CPHA = 1)	–4	—	

1. Slave Receive Only mode can operate at a maximum frequency of 60 MHz. In this mode, the SPI can receive data on SIN, but no valid data is transmitted on SOUT.
2. For SPI_CTARn[PCSSCK] - 'PCS to SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[CSSCK] - 'PCS to SCK Delay Scaler' configuration is '2' (0000h).
3. For SPI_CTARn[PASC] - 'After SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[ASC] - 'After SCK Delay Scaler' configuration is '2' (0000h).
4. The numbers are valid when SPI is configured for 50/50. Refer the Reference manual for the mapping of the duty cycle to each configuration. A change in duty cycle changes the parameter here. For example, a configuration providing duty cycle of 33/66 at SPI translates to min tSCK/3 - 1.5 ns and max tSCK/3 + 1.5 ns.
5. The slave mode parameters (t_{SUI}, t_HI, t_{SUO} and t_{HO}) assume 50% duty cycle on SCK input. Any change in SCK duty cycle input must be taken care during the board design or by the master timing.
6. The slave receive only mode parameters (t_{SUI} and t_{HI}) assume 50% duty cycle on SCK input. Any change in SCK duty cycle input must be taken care during the board design or by the master timing. However, there is additional restriction in the slave receive only mode that the duty cycle at the slave input should not go below t_{sdc}(min) corresponding to the t_{sdc}(min) for the slave receive mode.
7. In the master mode, this is governed by t_{PCSSCK}. Refer the SPI chapter in the Reference Manual for details. The minimum spec is valid only for SPI_CTARn[PCSSCK]= '0b01' (PCS to SCK delay prescalar of 3) or higher.
8. In the master mode, this is governed by t_{PASC}. Refer the SPI chapter in the Reference Manual for details. The minimum spec is valid only for SPI_CTARn[PASC]= '0b01' (after SCK delay prescalar of 3) or higher.
9. For SPI_CTARn[BR] - 'Baud Rate Scaler' configuration is >= 4.
10. N = Configured sampling point value in MTFE=1 Mode.
11. Same value is applicable for PCS timing in continuous SCK mode.
12. SPI_MCR[SMPL_PT] should be set to 1.

NOTE

For numbers shown in the following figures, see Table 43.

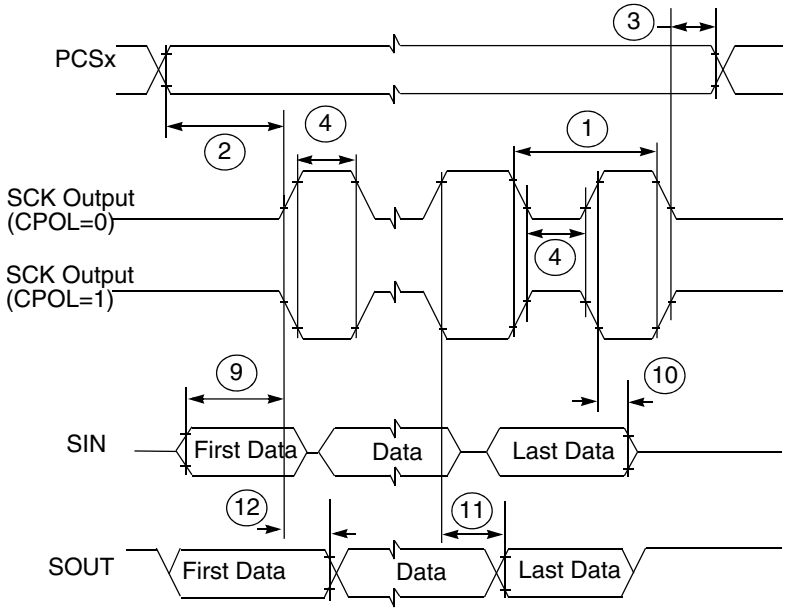

Figure 28. SPI modified transfer format timing — master, CPHA = 0

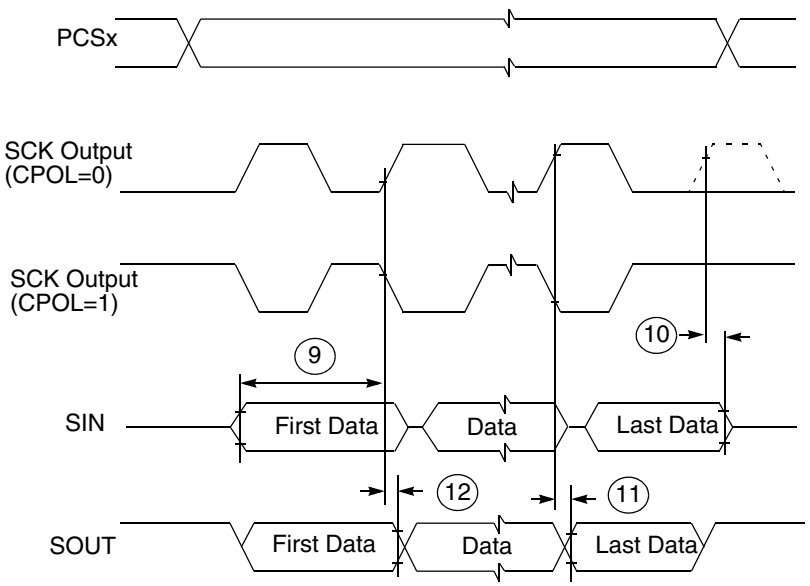

Figure 29. SPI modified transfer format timing — master, CPHA = 1

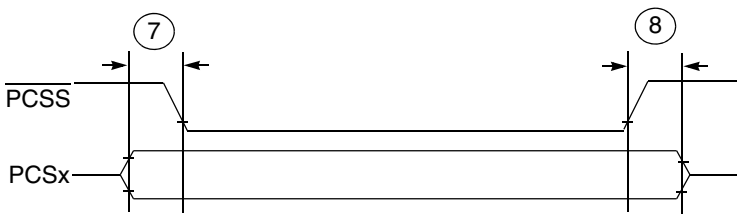

Figure 30. SPI PCS strobe (PCSS) timing

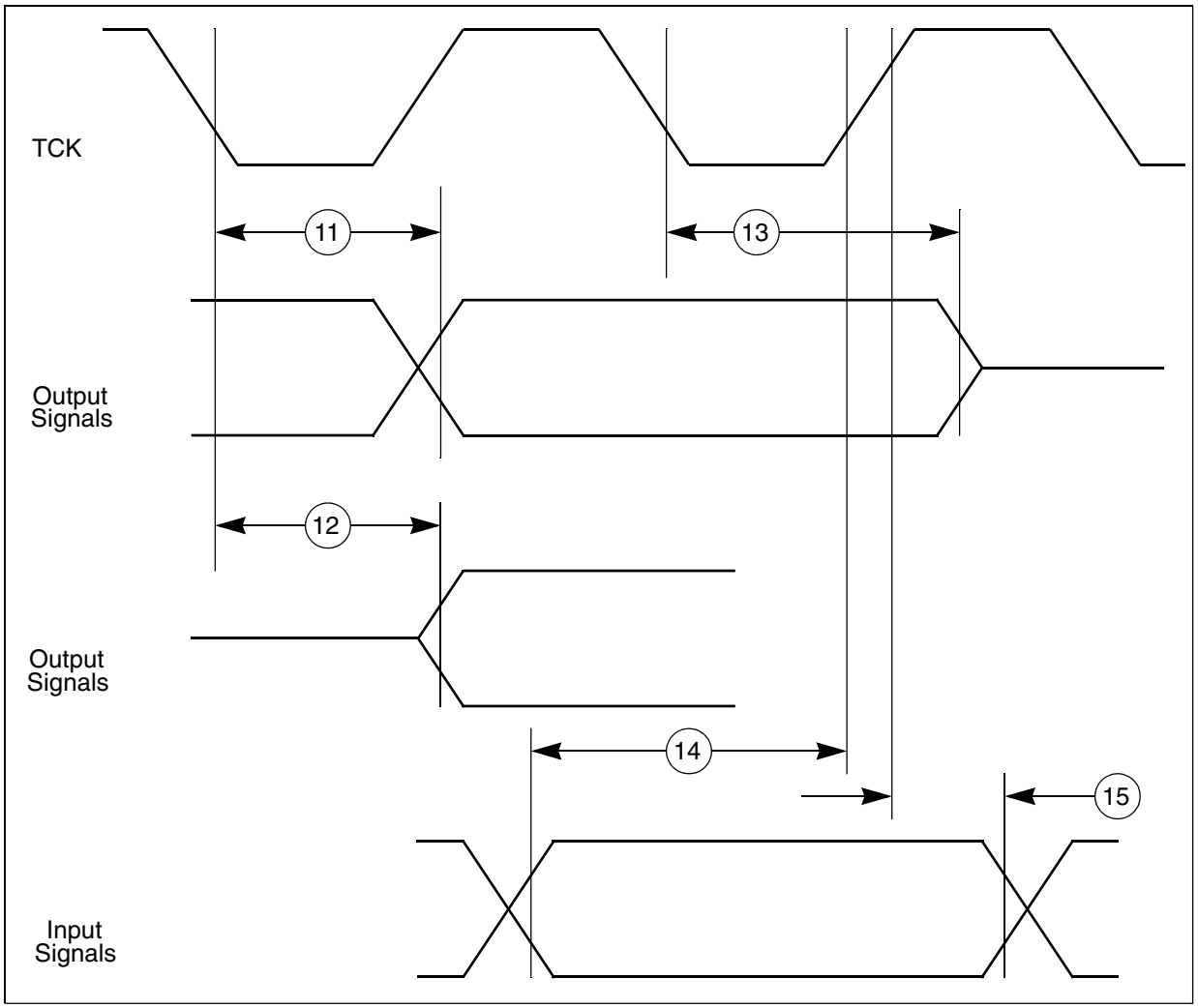

Figure 35. JTAG boundary scan timing

10.2 Nexus Aurora debug port timing

Table 47. Nexus Aurora debug port timing

#	Symbol	Characteristic	Min	Max	Unit
1	t_{REFCLK}	Reference clock frequency	625	1250	MHz
1a	t_{MCYC}	Reference Clock rise/fall time	—	400	ps
2	t_{RCDC}	Reference Clock Duty Cycle	45	55	%
3	J_{RC}	Reference Clock jitter	—	40	ps
4	$t_{STABILITY}$	Reference Clock Stability	50	—	PPM
5	BER	Bit Error Rate	—	10^{-12}	—
6	t_{EVTIPW}	$\overline{EVTI}$ Pulse Width	4.0	—	t_{TCYC}
7	J_D	Transmit lane Deterministic Jitter	—	0.17	OUI
8	J_T	Transmit lane Total Jitter	—	0.35	OUI

Table continues on the next page...

12 External interrupt timing (IRQ pin)

Table 49. External interrupt timing

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time[1]	—	6	—	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both

NOTE

tCYC is equivalent to TCK (prescaled filter clock period) which is the IRC clock prescaled to the Interrupt Filter Clock Prescaler (IFCP) value. TCK = T(IRC) x (IFCP + 1) where T(IRC) is the internal oscillator period. Refer SIUL2 chapter of the device reference manual for details.

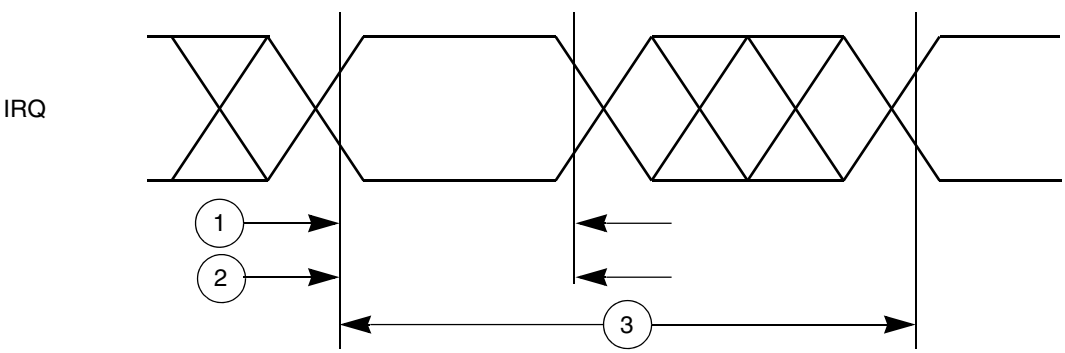

Figure 37. External interrupt timing

13 Temperature sensor electrical characteristics

The following table describes the temperature sensor electrical characteristics.

Table 50. Temperature sensor electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
—	Temperature monitoring range		-40	—	150	°C
T_{SENS}	Sensitivity		—	5.18	—	mV/°C
T_{ACC}	Accuracy	T_J = -40 to 150°C	5	—	5	°C

14 Radar module

14.1 MIPICSI2 D-PHY electrical and timing specifications

This section describes MIPICSI2[1] D-PHY electrical specifications, compliant with MIPICSI2 version 1.1, D-PHY specification Rev. 1.0 (for MIPI sensor port x4 lanes).

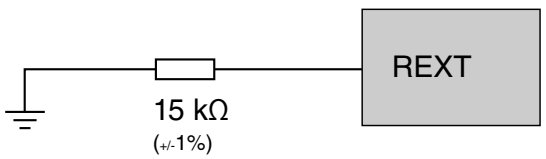

Figure 38. MIPICSI2 circuit

Table 51. Calibrator specifications

Symbol	Parameters	Min	Typ	Max	Unit
R_{EXT}	External reference resistor, 1% accuracy (or better), for auto calibration	-	15	-	kΩ
T_{cal}	Time from when PD signal goes low to when CALCOMPL goes high	-	2	2.5	µs

14.1.1 Electrical and timing information

Table 52. Electrical and timing information

Symbol	Parameters	Min	Typ	Max	Unit
HS Line Receiver DC Specifications					
V_{IDTH}	Differential input high voltage threshold	-	-	70	mV
V_{IDTL}	Differential input low voltage threshold	-70	-	-	mV
V_{IHHS}	Single ended input high voltage	-	-	460	mV
V_{ILHS}	Single ended input low voltage	-40	-	-	mV
V_{CMRXDC}	Input common mode voltage	70	-	330	mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	-	-	450	mV
Z_{ID}	Differential input impedance	80	-	125	ohm
LP Line Receiver DC Specifications					
V_{ILLP}	Input low voltage	-	-	550	mV

Table continues on the next page...

1. All rights reserved. This material is reprinted with the permission of the MIPI Alliance, Inc. No part(s) of this document may be disclosed, reproduced or used for any purpose other than as needed to support the use of the products of NXP Semiconductors.

Table 52. Electrical and timing information (continued)

Symbol	Parameters	Min	Typ	Max	Unit
V_{IHLP}	Input high voltage	880	-	-	mV
V_{HYST}	Input hysteresis	25	-	-	mV

14.1.2 D-PHY signaling levels

The signal levels are different for differential HS mode and single-ended LP mode. The figure below shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

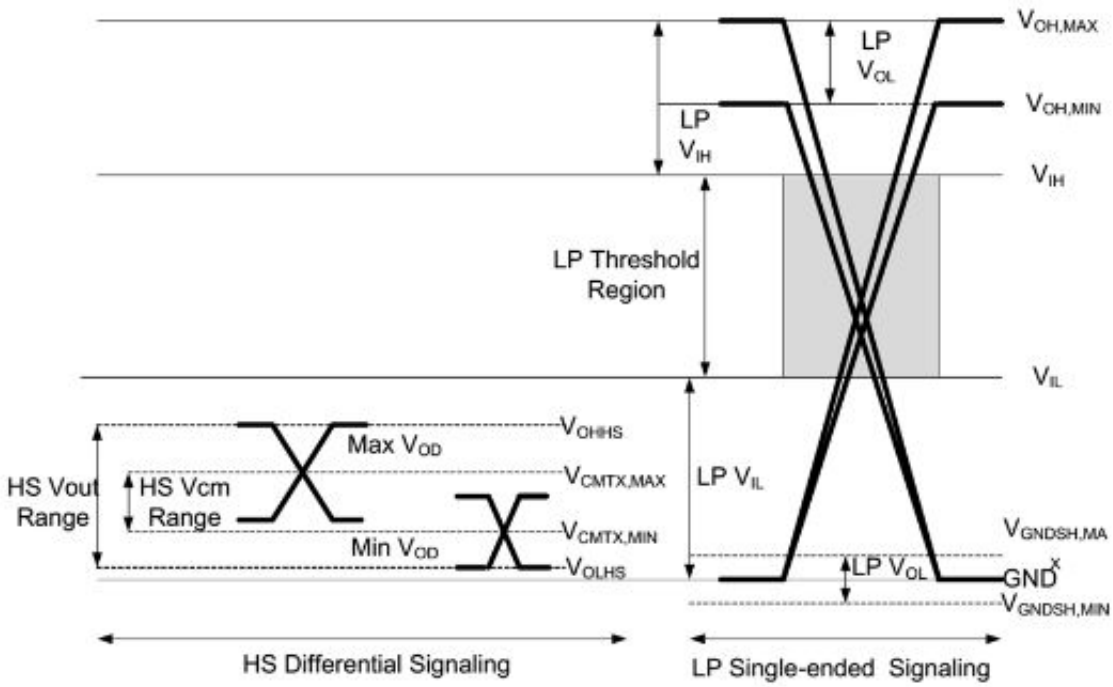

Figure 39. D-PHY signaling levels

14.1.3 D-PHY switching characteristics

Table 53. D-PHY switching characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HS Line Receiver AC Specifications						
-	Maximum serial data rate	On DATAP/N inputs. 80 Ohm<= RL <= 125 Ohm	80	-	1000	Mbps

Table continues on the next page...

14.1.5 Data to clock timing

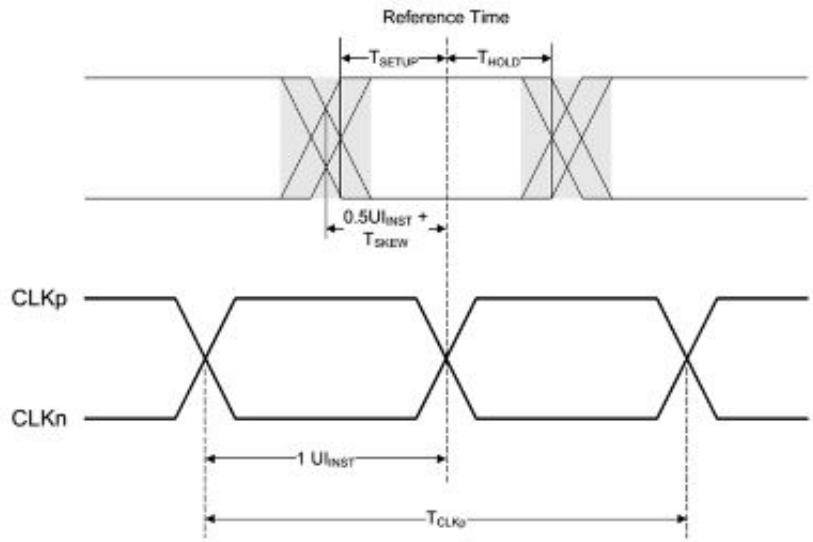

Figure 41. Definition

Table 54. Data to clock timing specifications

Symbol	Parameter	Min	Typ	Max	Unit
T_{CLKP}	Clock Period	40	-	500	MHz
UI_{INST}	UI Instantaneuous	1	-	12.5	ns
T_{SETUP}	Data to Clock Setup Time	0.15	-	-	UIINST
T_{HOLD}	Clock to Data Hold Time	0.15	-	-	UIINST

14.2 MIPICSI2 Disclaimer

The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled by any of the authors or developers of this material or MIPI®. The material contained herein is provided on an “AS IS” basis and to the maximum extent permitted by applicable law, this material is provided AS IS AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of negligence.

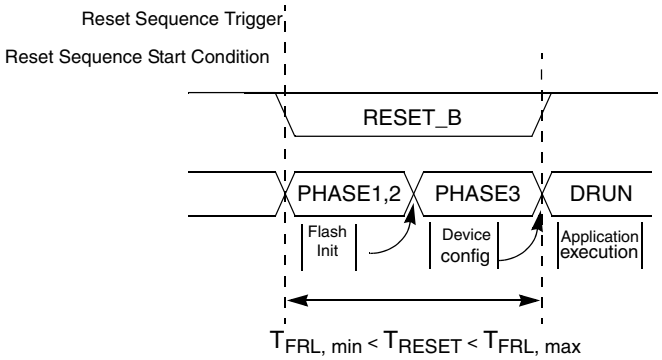

Figure 45. Functional reset sequence long

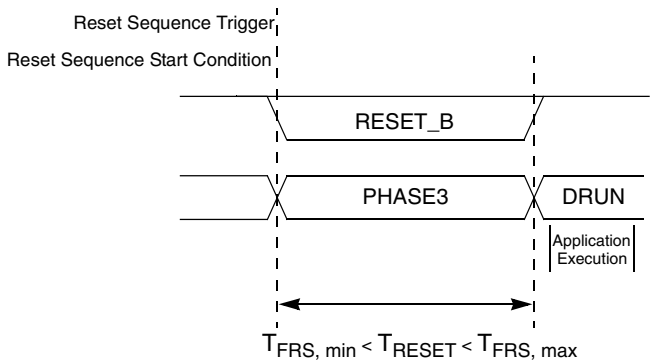

Figure 46. Functional reset sequence short

The reset sequences shown in Figure 45 and Figure 46 are triggered by functional reset events. $\overline{\text{RESET}}$ is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

18 Power sequencing requirements

The device does not require any specific power sequencing as far as user follows recommendations in this section.

Either ramp $V_{DD\_HV\_IO}$ and $V_{DD\_HV\_PMU}$ together or ramp $V_{DD\_HV\_IO}$ before $V_{DD\_HV\_PMU}$ such that the two supplies always maintain 100 mV or less difference, when using internal regulation mode. $V_{DD\_LV\_DPHY}$ and $V_{DD\_LV\_CORE}$ are to be driven from same source. $V_{DD\_HV\_IO}$, $V_{DD\_HV\_IO\_RGMII}$, $V_{DD\_HV\_IO\_PWM}$ and $V_{DD\_HV\_IO\_LFAST}$ supplies should be treated as a single supply from board perspective.

As mentioned in the previous section, it is expected that the external ASIC which powers up the device in external regulation mode deasserts VREG_POR_B pin only when all the power supplies to the design are in operating range.

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Document Number S32R274
Revision 4, 05/2018