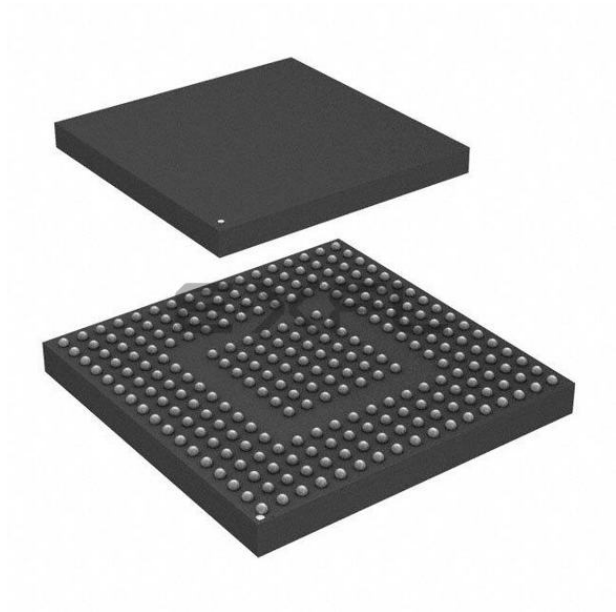

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4, e200z7 (2)
Core Size	32-Bit Tri-Core
Speed	180MHz, 240MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI, ZipWire
Peripherals	POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	1.5M x 8
Voltage - Supply (Vcc/Vdd)	1.19V ~ 5.5V
Data Converters	A/D 16x12b SAR, 4x12 Sigma; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32r274ksk2vmm

1.3 Block diagram

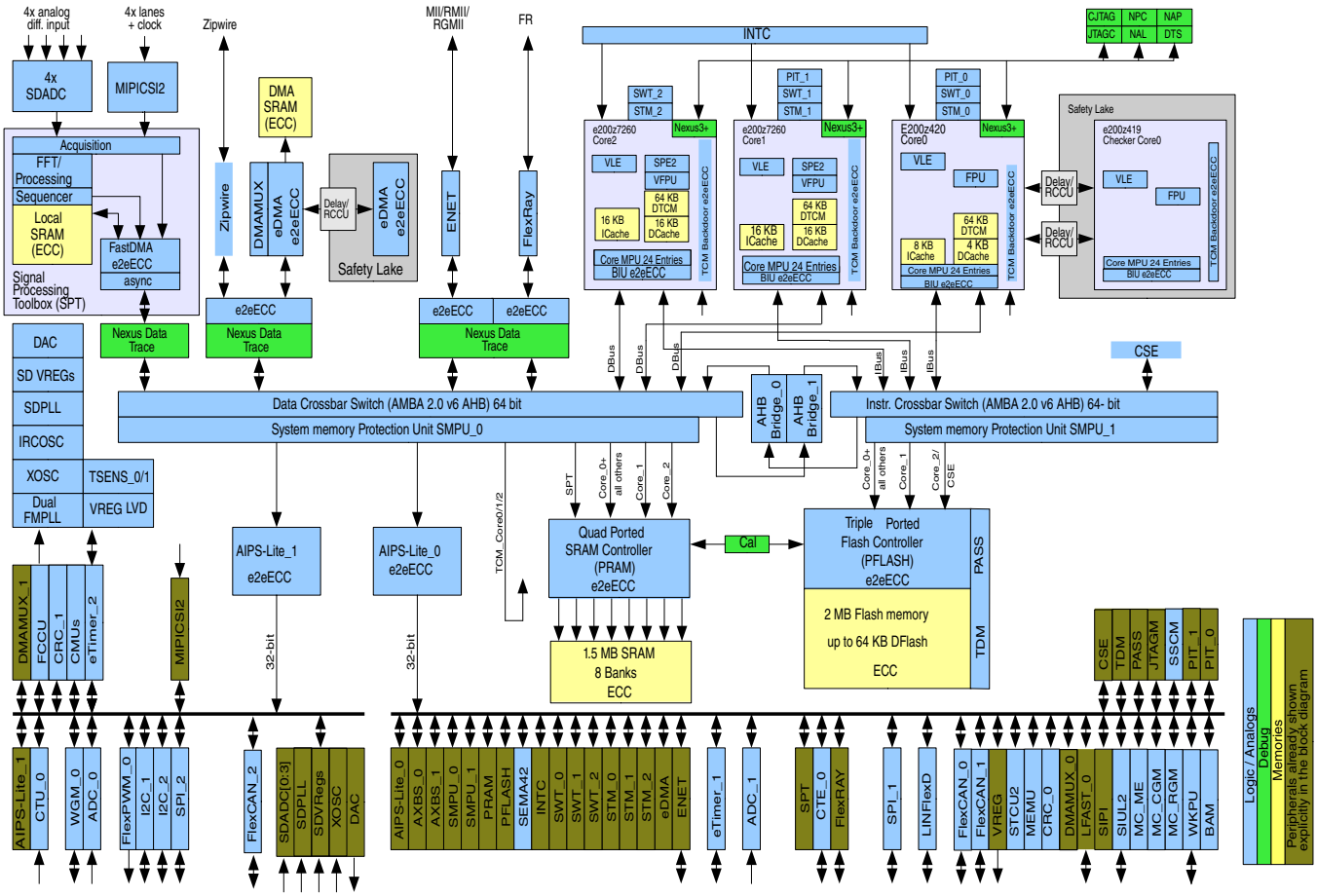

Figure 1. S32R274 block diagram

2 Ordering parts

2.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the device number.

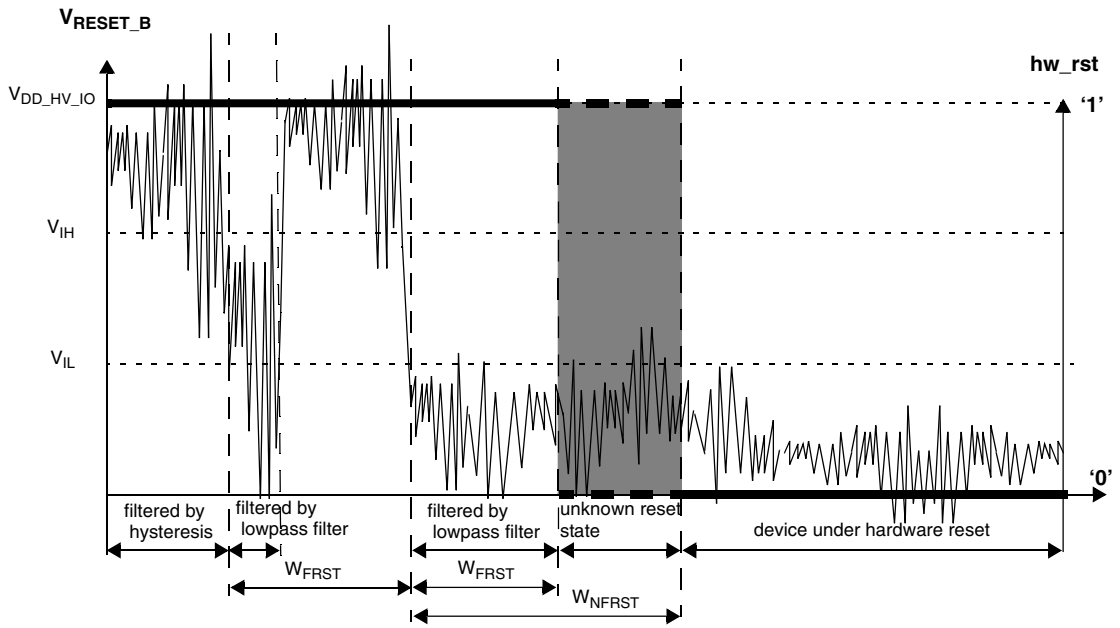

Figure 5. Noise filtering on reset signal

Table 18. RESET_B electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level TTL (Schmitt Trigger)	—	2.0	—	$V_{DD\_HV\_IOx}$ + 0.4	V
V_{IL}	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.56	V
V_{HYS}[2]	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV
I_{OL_R}	Strong pull-down current	Device under power-on reset $V_{DD\_HV\_IO}$ = 1.2 V V_{OL} = 0.35 x $V_{DD\_HV\_IO}$	0.2	—	—	mA
		Device under power-on reset $V_{DD\_HV\_IO}$=3.0 V V_{OL} = 0.35 x $V_{DD\_HV\_IO}$	15	—	—	mA
W_{FRST}	RESET_B input filtered pulse	—	—	—	500	ns
W_{NFRST}	RESET_B input not filtered pulse	—	2400	—	—	ns
$\lvert I_{WPD} \rvert$	Weak pull-down current absolute value	V_{IN} = $V_{DD\_HV\_IOx}$	30	—	100	µA

1. $V_{DD\_HV\_IOx}$ = 3.3 V -5%,+10%, T_J = –40 / 150°C, unless otherwise specified.
2. Data based on characterization results, not tested in production.

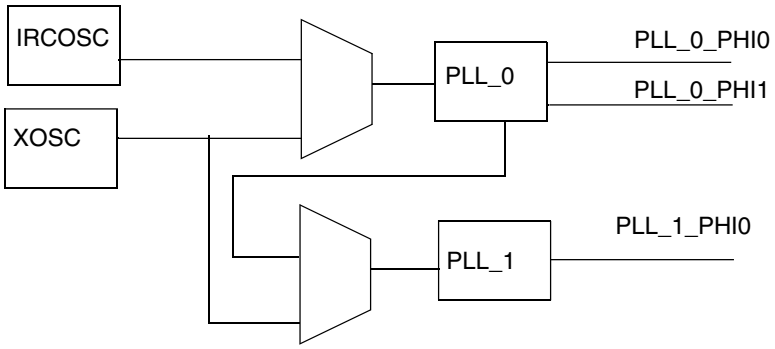

Figure 6. PLL integration

Table 20. PLL0 electrical characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{PLL0IN}	PLL0 input clock[2, 3]	—	14	—	44	MHz
Δ_{PLL0IN}	PLL0 input clock duty cycle[2]	—	40	—	60	%
$f_{PLL0VCO}$	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI0}$	PLL0 output clock PHI0	—	4.76	—	625[4]	MHz
$f_{PLL0PHI1}$	PLL0 output clock PHI1	—	20	—	156	MHz
$t_{PLL0LOCK}$	PLL0 lock time	—	—	—	100	µs
$\Delta_{PLL0LTJ}$	PLL0 long term jitter f_{PLL0IN} = 8 MHz (resonator)[5]	$f_{PLL0PHI0}$ = 40 MHz, 1 µs			± 1	ns
		$f_{PLL0PHI0}$ = 40 MHz, 13 µs			± 1	ns
I_{PLL0}	PLL0 consumption		—	—	5	mA

1. $V_{DD\_LV\_PLL0}$ =1.25 V ± 5%, T_J = -40 / 150 °C unless otherwise specified.
2. PLL0IN clock retrieved directly from either IRCOSC or external XOSC clock.
3. f_{PLL0IN} frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure the reference clock to the PLL analog loop is in the range 8 MHz-20 MHz
4. The maximum clock outputs are limited by the design clock frequency requirements as per recommended operating conditions.
5. $V_{DD\_LV\_PLL0}$ noise due to application in the range $V_{DD\_LV\_PLL0}$ = 1.25 V±5%, with frequency below PLL bandwidth (40 KHz) will be filtered.

Table 21. FMPLL1 electrical characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{PLL1IN}	PLL1 input clock[2]	—	38	—	78	MHz
Δ_{PLL1IN}	PLL1 input clock duty cycle[2]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI0}$	PLL1 output clock PHI0	—	4.76	—	625	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	µs
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
I_{PLL1}	PLL1 consumption		—	—	6	mA

1. $V_{DD\_LV\_PLL0}$ = 1.25 V ± 5%, T_J = -40 / 150°C unless otherwise specified.
2. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock.

Table 26. Sigma Delta ADC Parameters (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Characterized under the following conditions: • 0.6 Vpp (i.e. -6 dBFS) input signals applied at the following frequencies one at a time: 20.77 KHz, 317.7 KHz, 857.7 KHz, 1.411 MHz, 2.95 MHz, 3.897 MHz, and 4.997 MHz and the SNR in dBFS is then calculated. • SNR at 5 MHz will be reduced by 5 dB due to decimation filter roll off. • The SNR is specified to be 67 dBFS typical for input frequencies between 20 KHz and 4 MHz. Mismatch shaper on.				
$SNR_{SDA\_MM\_OFF}$[1]	Signal-to-Noise Ratio Mismatch Shaper off	Input Frequency Range and integration bandwidth are from 20 KHz to 5 MHz. (using full-bandwidth decimation filter coefficients). Production test frequencies 449 KHz and 4 MHz. Production test amplitude is -6 dBFS = 0.6 Vpp. Characterized under the following conditions: • 0.6 Vpp (i.e. -6dBFS) input signals applied at the following frequencies one at a time: 20.77 KHz, 317.7 KHz, 857.7 KHz, 1.411 MHz, 2.95 MHz, 3.897 MHz, and 4.997 MHz and the SNR in dBFS is then calculated. • SNR at 5 MHz will be reduced by 5 dB due to decimation filter roll off. • The SNR is specified to be 67 dBFS typical for input frequencies between 20 KHz and 4 MHz. Mismatch shaper off.	65	67	—	dBFS
$SNDR_{SDA\_MM\_ON}$[1]	Signal-to-Noise-and-Distortion Ratio Mismatch Shaper on	Input Frequency Range and integration bandwidth are from 20 KHz to 5 MHz. (using full-bandwidth decimation filter coefficients). Production test frequencies 449 KHz and 4 MHz. Production test amplitude is -6 dBFS = 0.6 Vpp. Characterized under the following conditions: • 0.6 Vpp (i.e. -6 dBFS) input signals applied at the following frequencies one at a time: 20.77 KHz, 317.7 KHz, 857.7 KHz, 1.411 MHz, 2.95 MHz, 3.897 MHz, and 4.997 MHz and the SNDR in dBFS is then calculated. • SNR at 5 MHz will be reduced by 5 dB due to decimation filter roll off. • The SNR is specified to be 64 dBFS typical for input frequencies between 20 KHz and 4 MHz. Mismatch shaper on.	62	64	—	dBFS
$SNDR_{SDA\_MM\_OFF}$[1]	Signal-to-Noise-and-Distortion Ratio Mismatch Shaper off	Input Frequency Range and integration bandwidth are from 20 KHz to 5 MHz. (using full-bandwidth decimation filter coefficients)	60	62	—	dBFS

Table continues on the next page...

Table 34. RMII signal switching specifications (continued)

Num	Description	Min.	Max.	Unit
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

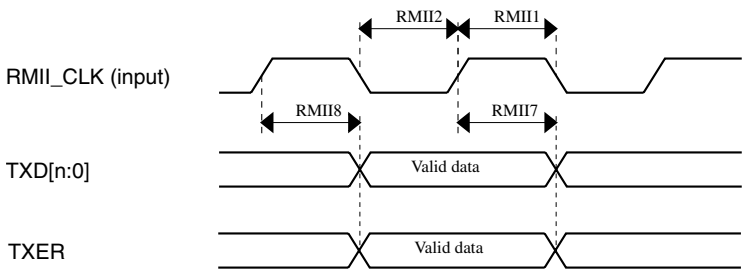

Figure 12. RMII transmit signal timing diagram

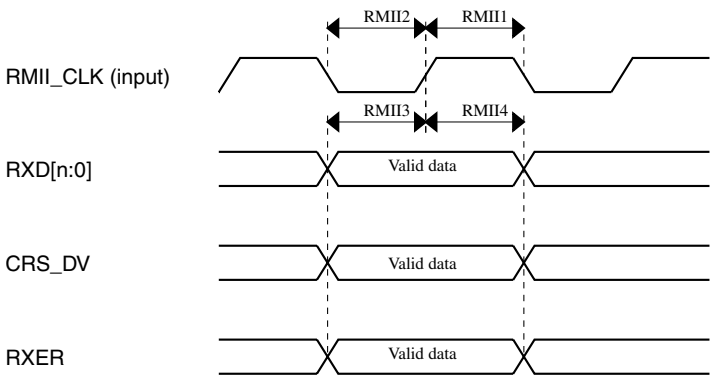

Figure 13. RMII receive signal timing diagram

9.1.3 RGMII signal switching specifications

The RGMII interface works at 3.3 V compatible levels as mentioned in RGMII pad DC electrical characteristics.

The following timing specs meet the requirements for RGMII style interfaces for a range of transceiver devices.

- Measurements are with input transition of 0.750 ns and output load of 10 pF.

Table 35. RGMII signal switching specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
—	Input Duty cycle (Clock from external PHY)	48	—	52	%	
Tcyc	Clock cycle duration	7.2	8.0	8.8	ns	1
TskewT	Data to clock output skew at transmitter	-500	0	500	ps	2
TskewR	Data to clock input skew at receiver	1	1.8	2.6	ns	2

Table continues on the next page...

Table 42. LFAST electrical characteristics (continued)

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
T_{PD2NM_TX}	Transmitter startup time (power down to normal mode)[3]	—	—	0.2	2	µs
T_{SM2NM_TX}	Transmitter startup time (sleep mode to normal mode)[4]	—	—	0.2	0.5	µs
T_{PD2NM_RX}	Receiver startup time[5] (Power down to Normal mode)	—	—	20	40	ns
T_{PD2SM_RX}	Receiver startup time[4] (Power down to Sleep mode)	—	—	20	50	ns
TRANSMITTER						
V_{OS_DRF}	Common mode voltage	—	1.08	—	1.32	V
$\lvert\Delta V_{OD\_DRF}\rvert$	Differential output voltage swing (terminated)	—	±100	±200	± 285	mV
T_{TR_DRF}	Rise/Fall time (10% - 90% of swing)	—	0.26	—	1.5	ns
R_{OUT_DRF}	Terminating resistance		67	—	198	Ω
C_{OUT_DRF}	Capacitance[6]	—	—	—	5	pF
RECEIVER						
V_{ICOM_DRF}	Common mode voltage	—	0.15[7]	—	1.6[8]	V
$\lvert D_{VI\_DRF}\rvert$	Differential input voltage	—	100	—	—	mV
V_{HYS_DRF}	Input hysteresis	—	25	—	—	mV
R_{IN_DRF}	Terminating resistance		80	115	150	Ω
C_{IN_DRF}	Capacitance[9]	—	—	3.5	6	pF
L_{IN_DRF}	Parasitic Inductance[10]	—	—	5	10	nH
TRANSMISSION LINE CHARACTERISTICS (PCB Track)						
Z_0	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	Transmission line differential impedance	—	95	100	105	Ω

1. $V_{DD\_VH\_IOx}$ = 3.3 V -5%,+10%, T_J = –40 / 150 °C, unless otherwise specified
2. Startup time is defined as the time taken by LFAST current reference block for settling bias current after its pwr_down (power down) has been deasserted. LFAST functionality is guaranteed only after the startup time.
3. Startup time is defined as the time taken by LFAST transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
4. Startup time is defined as the time taken by LFAST transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
5. Startup time is defined as the time taken by LFAST receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.

6. Total lumped capacitance including silicon, package pin and bond wire. Application board simulation is needed to verify LFAST template compliancy.
7. Absolute min = 0.15 V – (285 mV / 2) = 0 V
8. Absolute max = 1.6 V + (285 mV / 2) = 1.743 V
9. Total capacitance including silicon, package pin and bond wire
10. Total inductance including silicon, package pin and bond wire

9.4 Serial Peripheral Interface (SPI) timing specifications

The following table describes the SPI electrical characteristics.

MTEF=1 Mode timing values given below are only applicable when external SPI is in classic mode. Slave mode timing values given below are applicable when device is in MTFE=0.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured as SRE = 11.

Table 43. SPI timing

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	SPI cycle time	Master (MTFE = 0)	50	—	ns
			Master (MTFE = 1)	50	—	
			Slave (MTFE = 0)	50	—	
			Slave Receive Only mode[1]	16	—	
2	t_{CSC}	PCS to SCK delay	Master	63.8[2]	—	ns
3	t_{ASC}	After SCK delay	Master	68.8[3]	—	ns
4	t_{SDC}	SCK duty cycle	Master[4]	$t_{SCK}/2 - 1$	$t_{SCK}/2 + 1$	ns
			Slave[5]	—	—	ns
			Slave Receive only mode[6]	tSCK/2 – 0.750	tSCK/2 + 0.750	ns
5	t_A	Slave access time	$\overline{SS}$ active to SOUT valid	—	25	ns
6	t_{DIS}	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	25	ns
7	t_{PCSC}	PCSx to $\overline{PCSS}$ time	—	13 [7]	—	ns
8	t_{PASC}	$\overline{PCSS}$ to PCSx time	—	13 [8]	—	ns
9	t_{SUI}	Data setup time for inputs	Master (MTFE = 0)	15	—	ns
			Slave	2	—	
			Slave Receive Mode	2	—	
			Master (MTFE = 1, CPHA = 0)[9]	15-N x SPI IPG clock period[10]	—	
			Master (MTFE = 1, CPHA = 1)	15	—	
10	t_{HI}	Data hold time for inputs	Master (MTFE = 0)	–2	—	ns
			Slave	4	—	
			Slave Receive Mode	4	—	

Table continues on the next page...

Table 43. SPI timing (continued)

No.	Symbol	Parameter	Conditions	Min	Max	Unit
			Master (MTFE = 1, CPHA = 0)[9]	-2 + N x SPI IPG clock period [10]	—	
			Master (MTFE = 1, CPHA = 1)	–2	—	
11	t_{SUO}	Data valid (after SCK edge)	Master (MTFE = 0)	—	7 [11]	ns
			Slave	—	23	
			Master (MTFE = 1, CPHA = 0)[12]	—	7 + SPI IPG Clock Period	
			Master (MTFE = 1, CPHA = 1)	—	7	
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	–4 [11]	—	ns
			Slave	3.8	—	
			Master (MTFE = 1, CPHA = 0) [12]	-4 + SPI IPG Clock Period	—	
			Master (MTFE = 1, CPHA = 1)	–4	—	

1. Slave Receive Only mode can operate at a maximum frequency of 60 MHz. In this mode, the SPI can receive data on SIN, but no valid data is transmitted on SOUT.
2. For SPI_CTARn[PCSSCK] - 'PCS to SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[CSSCK] - 'PCS to SCK Delay Scaler' configuration is '2' (0000h).
3. For SPI_CTARn[PASC] - 'After SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[ASC] - 'After SCK Delay Scaler' configuration is '2' (0000h).
4. The numbers are valid when SPI is configured for 50/50. Refer the Reference manual for the mapping of the duty cycle to each configuration. A change in duty cycle changes the parameter here. For example, a configuration providing duty cycle of 33/66 at SPI translates to min tSCK/3 - 1.5 ns and max tSCK/3 + 1.5 ns.
5. The slave mode parameters (t_{SUI}, t_HI, t_{SUO} and t_{HO}) assume 50% duty cycle on SCK input. Any change in SCK duty cycle input must be taken care during the board design or by the master timing.
6. The slave receive only mode parameters (t_{SUI} and t_{HI}) assume 50% duty cycle on SCK input. Any change in SCK duty cycle input must be taken care during the board design or by the master timing. However, there is additional restriction in the slave receive only mode that the duty cycle at the slave input should not go below t_{sdc}(min) corresponding to the t_{sdc}(min) for the slave receive mode.
7. In the master mode, this is governed by t_{PCSSCK}. Refer the SPI chapter in the Reference Manual for details. The minimum spec is valid only for SPI_CTARn[PCSSCK]= '0b01' (PCS to SCK delay prescalar of 3) or higher.
8. In the master mode, this is governed by t_{PASC}. Refer the SPI chapter in the Reference Manual for details. The minimum spec is valid only for SPI_CTARn[PASC]= '0b01' (after SCK delay prescalar of 3) or higher.
9. For SPI_CTARn[BR] - 'Baud Rate Scaler' configuration is >= 4.
10. N = Configured sampling point value in MTFE=1 Mode.
11. Same value is applicable for PCS timing in continuous SCK mode.
12. SPI_MCR[SMPL_PT] should be set to 1.

NOTE

For numbers shown in the following figures, see Table 43.

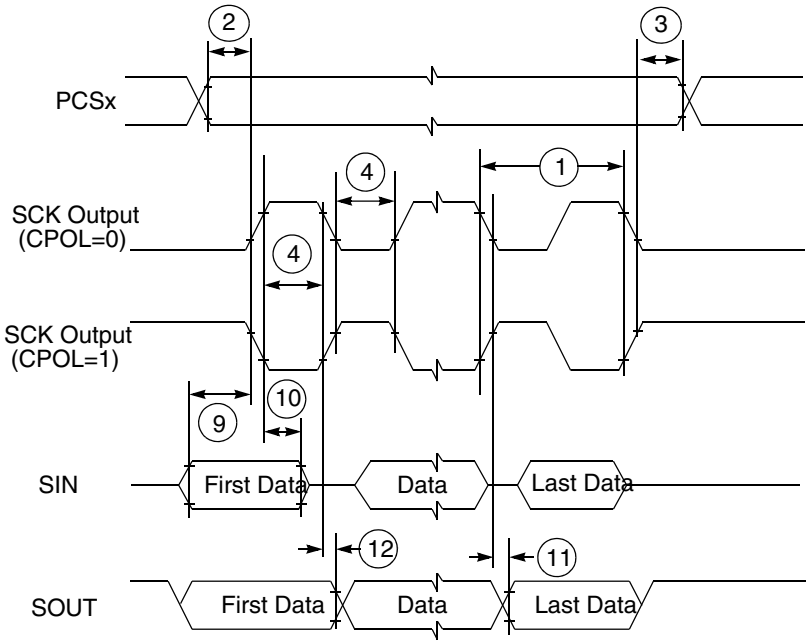

Figure 24. SPI classic SPI timing — master, CPHA = 0

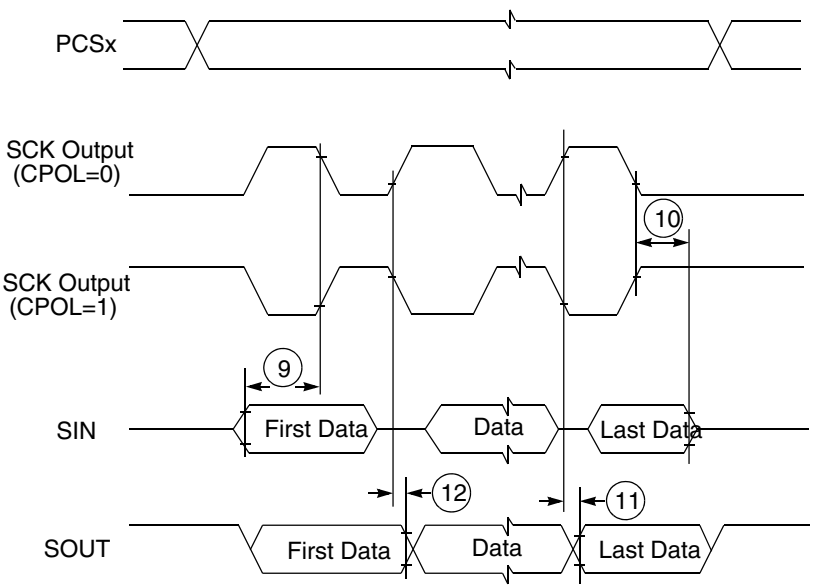

Figure 25. SPI classic SPI timing — master, CPHA = 1

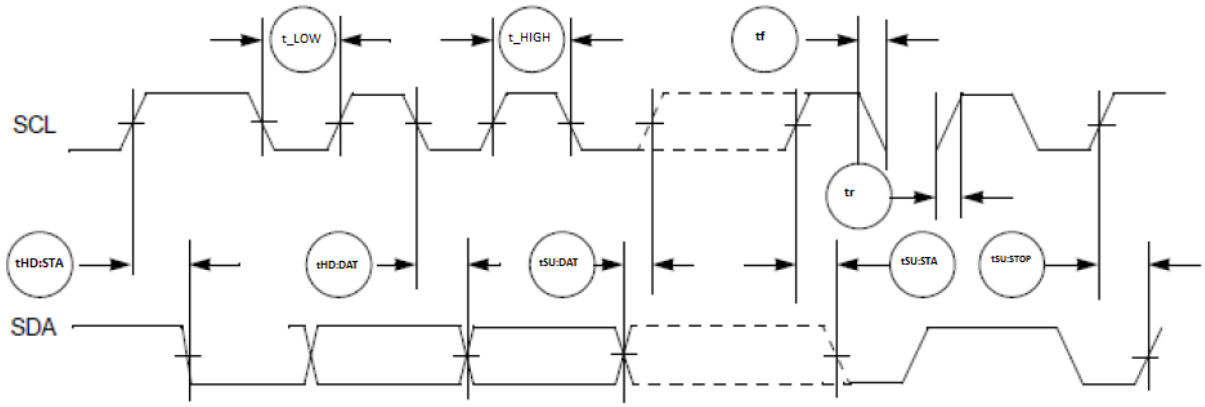

Figure 31. I²C input/output timing

10 Debug modules

10.1 JTAG/CJTAG interface timing

The following table lists JTAGC/CJTAG electrical characteristics.

- Measurements are with input transition of 1 ns, output load of 50 pF and pads configured with SRE=11.

Table 46. JTAG/CJTAG pin AC electrical characteristics [1]

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}[2]	TCK Cycle Time (JTAG)	36	—	ns
		TCK Cycle Time (CJTAG)	50		
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO/TMS Data Valid [3]	—	15[4]	ns
7	t_{TDOI}	TCK Low to TDO/TMS Data Invalid[3]	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO/TMS High Impedance[3]	—	22	ns
9	t_{JCMPPW}	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600[5]	ns
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns

Table continues on the next page...

Table 47. Nexus Aurora debug port timing (continued)

#	Symbol	Characteristic	Min	Max	Unit
9	S_O	Differential output skew	—	20	ps
10	S_{MO}	Lane to lane output skew	—	1000	ps
11	OUI	Aurora lane Unit Interval	800	800	ps

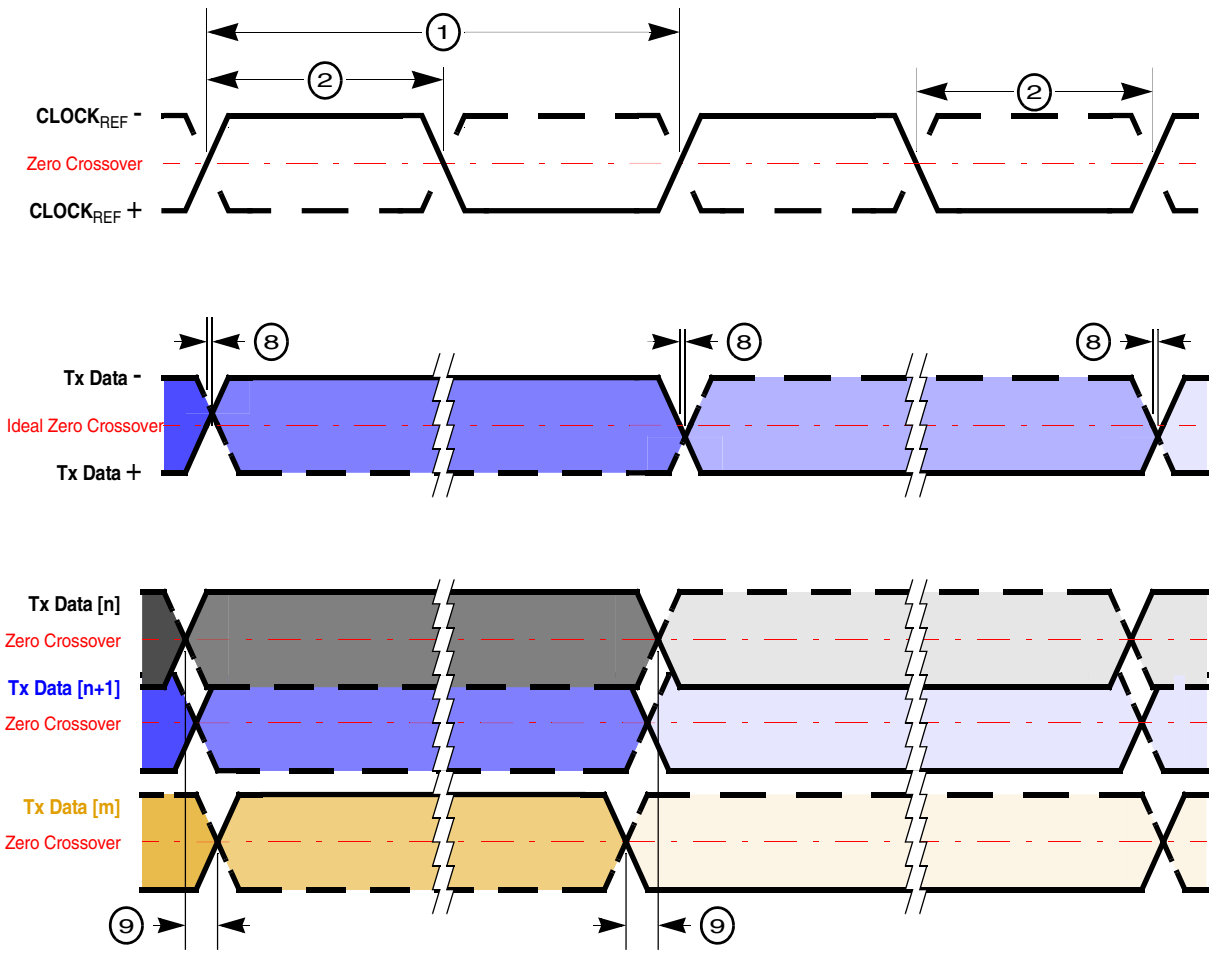

Figure 36. Nexus Aurora timings

11 WKUP/NMI timing specifications

Table 48. WKUP/NMI glitch filter

Symbol	Parameter	Min	Typ	Max	Unit
W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
W_{NFNMI}	NMI pulse width that is passed	400	—	—	ns

12 External interrupt timing (IRQ pin)

Table 49. External interrupt timing

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time[1]	—	6	—	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both

NOTE

tCYC is equivalent to TCK (prescaled filter clock period) which is the IRC clock prescaled to the Interrupt Filter Clock Prescaler (IFCP) value. TCK = T(IRC) x (IFCP + 1) where T(IRC) is the internal oscillator period. Refer SIUL2 chapter of the device reference manual for details.

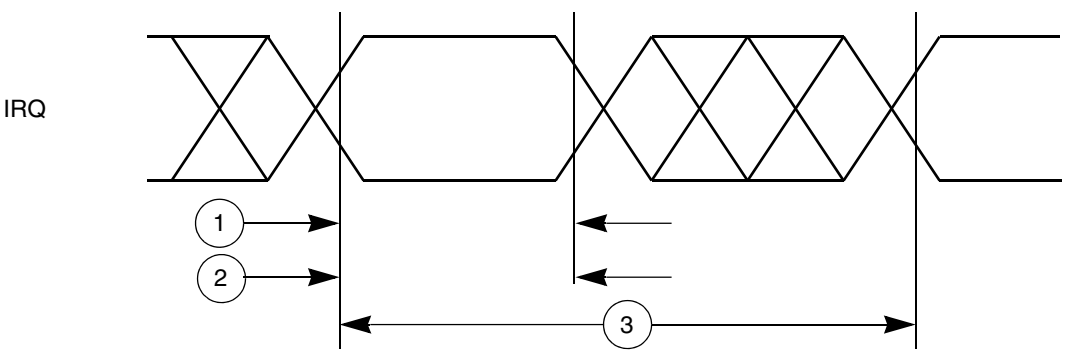

Figure 37. External interrupt timing

13 Temperature sensor electrical characteristics

The following table describes the temperature sensor electrical characteristics.

Table 50. Temperature sensor electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
—	Temperature monitoring range		-40	—	150	°C
T_{SENS}	Sensitivity		—	5.18	—	mV/°C
T_{ACC}	Accuracy	T_J = -40 to 150°C	5	—	5	°C

14 Radar module

14.1 MIPICSI2 D-PHY electrical and timing specifications

This section describes MIPICSI2[1] D-PHY electrical specifications, compliant with MIPICSI2 version 1.1, D-PHY specification Rev. 1.0 (for MIPI sensor port x4 lanes).

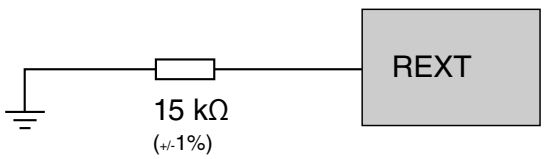

Figure 38. MIPICSI2 circuit

Table 51. Calibrator specifications

Symbol	Parameters	Min	Typ	Max	Unit
R_{EXT}	External reference resistor, 1% accuracy (or better), for auto calibration	-	15	-	kΩ
T_{cal}	Time from when PD signal goes low to when CALCOMPL goes high	-	2	2.5	µs

14.1.1 Electrical and timing information

Table 52. Electrical and timing information

Symbol	Parameters	Min	Typ	Max	Unit
HS Line Receiver DC Specifications					
V_{IDTH}	Differential input high voltage threshold	-	-	70	mV
V_{IDTL}	Differential input low voltage threshold	-70	-	-	mV
V_{IHHS}	Single ended input high voltage	-	-	460	mV
V_{ILHS}	Single ended input low voltage	-40	-	-	mV
V_{CMRXDC}	Input common mode voltage	70	-	330	mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	-	-	450	mV
Z_{ID}	Differential input impedance	80	-	125	ohm
LP Line Receiver DC Specifications					
V_{ILLP}	Input low voltage	-	-	550	mV

Table continues on the next page...

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Table 53. D-PHY switching characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔVCMRX(HF)	Common mode interference beyond 450 MHz		-	-	100	mVpp
ΔVCMRX(LF)	Common mode interference between 50 MHz and 450 MHz		-50	-	50	mVpp
CCM	Common mode termination		-	-	60	pF
LP Line Receiver AC Specification						
e_{SPIKE}	Input pulse rejection		-	-	300	Vps
T_{MIN}	Minimum pulse response		20	-	-	ns
V_{INT}	Pk-to-Pk interference voltage		-	-	200	mV
f_{INT}	Interference frequency		450	-	-	MHz

14.1.4 Low-power receiver timing

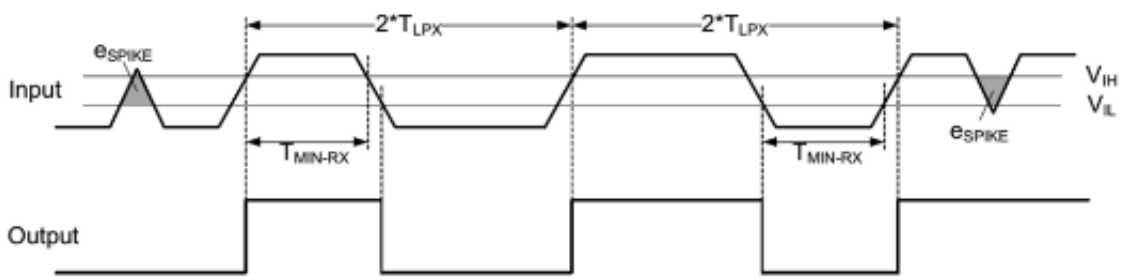

Figure 40. Input Glitch Rejection of Low-Power Receivers

package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

15.1.2 References

Semiconductor Equipment and Materials International; 3081 Zanker Road; San Jose, CA 95134 USA; (408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the Web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

16 Packaging

The S32R274 is offered in the following package types.

If you want the drawing for this package	Then use this document number
257-ball MAPBGA	98ASA00081D

NOTE

For detailed information regarding package drawings, refer to www.nxp.com.

17 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

17.1 Reset sequence duration

Table 57 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Reset sequence description.

Table 57. RESET sequences

No.	Symbol	Parameter	T_{Reset}			Unit
			Min	Typ	Max[1]	
1	T_{DRB}	Destructive Reset Sequence, BIST enabled	15		50[2]	ms
2	T_{DR}	Destructive Reset Sequence, BIST disabled	400		2000	µs
3	T_{ERLB}	External Reset Sequence Long, BIST enabled	15		50	ms
4	T_{FRL}	Functional Reset Sequence Long, BIST disabled	400		2000	µs
5	T_{FRS}	Functional Reset Sequence Short[3]	1		500	µs

1. The maximum value is applicable only if the reset sequence duration is not prolonged by an extended assertion of $\overline{\text{RESET}}$ by an external reset generator.
2. Max time is based on STCU BIST configuration execution time + max RESET time (TDR). For default STCU BIST configuration execution time, refer to EB834. Contact your NXP sales representative for details.
3. BIST is not executed on short functional reset

17.2 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The doted lines in the figures indicate the starting point and the end point for which the duration is specified in Table 57.

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The SMPS self test is always triggered during Phase3 after a destructive reset so that duration is included into Phase3 below.

In external regulation mode, the VREG_POR_B pin should be de-asserted only when all the design supplies are in operating range. Deassertion of VREG_POR_B pin triggers the start of reset sequence in internal as well as external regulation modes.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only

be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in Table 57 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

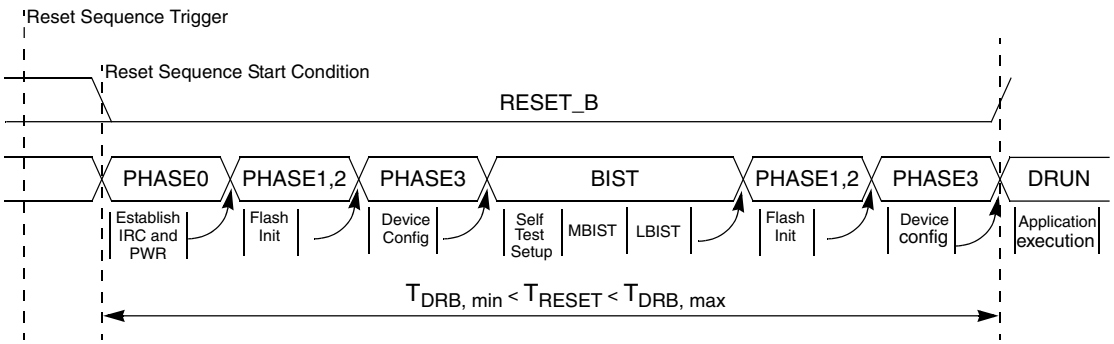

Figure 42. Destructive reset sequence, BIST enabled

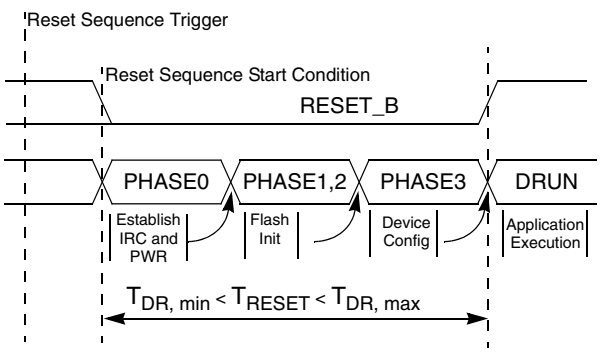

Figure 43. Destructive reset sequence, BIST disabled

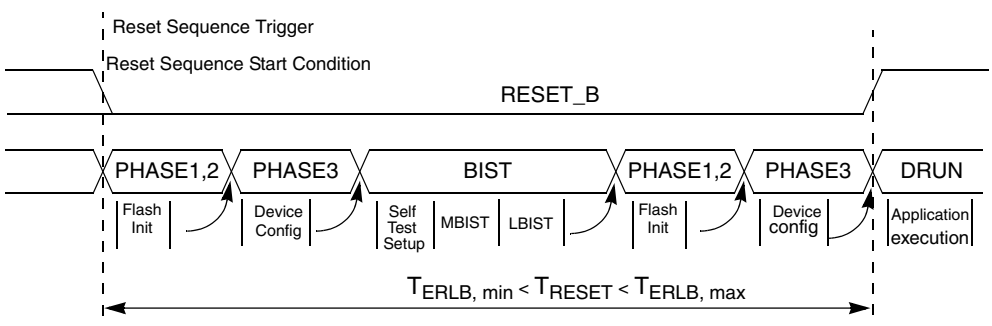

Figure 44. External reset sequence long, BIST enabled

It should be noted that LVD and HVD detectors on VDD supply are disabled by default in external regulation mode for preventing a conflict with external regulator operation but they can be enabled by software once design is powered up.

While designing the system, it is important to ensure that AFE supplies are powered up before data is sent on its input pads.

19 Pinouts

19.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

20 Revision History

Table 58. Revision History

Revision	Date	Description

Rev 4	May, 2018	• Removed section "4.1 Introduction".
		• Removed section "3.2 Format".
		• In Fields, removed figure "Commercial product code structure".
		• In Nexus Aurora debug port timing, added t_{EVTIPW} row.
		• In Ethernet switching specifications changed the following:
		  • Updated the figure RMII/MII serial management channel timing diagram.
		  • In Ethernet MDIO timing table changed MDC10 Min value and MDC11 Max value.
		• Extensively updated Table 32.
		• In Table 7, changed $V_{inxoscclkvih}$ Max value from 1.2 to 1.23.
		• In Table 25, added rows for the symbols $t_{sampleC}$, $t_{sampleS}$,$t_{sampleBG}$, and $t_{sampleTS}$.
		• In Table 6, changed V_{INA} maximum value to 6.0.
		• Added the following footnotes in Absolute maximum ratings :
		  • The maximum value limits of injection current and input voltage both must be followed together for proper device operation.
		  • The maximum value of 10 mA applies to pulse injection only. DC current injection is limited to a maximum of 5 mA.
		• In Table 7, changed V_{INA} maximum value to $V_{DD\_HV\_ADCREFx}$.
		• In Table 2 :
		  • Changed part from FS32R274KBK2MMM to FS32R274KSK2MMM and changed configuration from "B" to "S"
		  • Changed part from FS32R274KBK2VMM to FS32R274KSK2VMM and changed configuration from "B" to "S"
		  • Added "B or S" to Table 3