Zilog - Z8401506FEC00TR Datasheet

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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	6MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8401506fec00tr

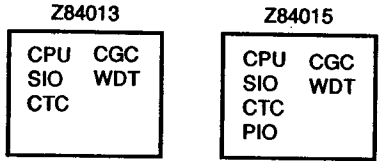


Figure 1. Z84013/015 Version

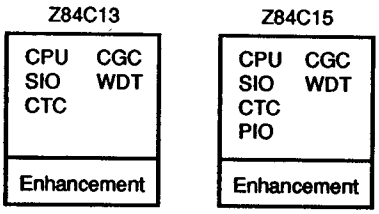


Figure 2. Z84C13/C15 Version

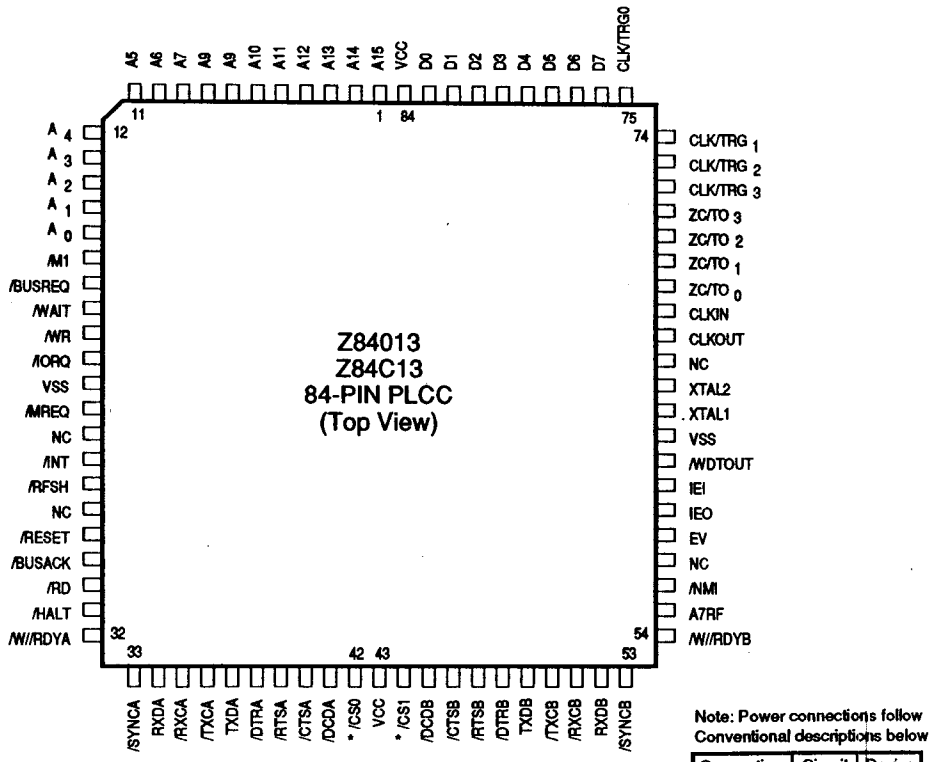


Figure 3. Z84013/Z84C13 Pin-out Assignments

SIO SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, 3-State	Function
/RxCA, /RxCB	35,51(x13), 33,49(x15)	In	Receive clock signal. In the asynchronous mode, the receive clocks can be 1, 16, 32, or 64 times the data transfer rate.
/TxCA, /TxCB	36,50(x13), 34,48(x15)	In	Transmitter clock signal. In the asynchronous mode, the transmitter clocks can be 1, 16, 32, or 64 times the data transfer rate.
TxDA, TxDB	37,49(x13), 35,47(x15)	Out	Serial transmit data signal.
/DTRA, /DTRB	38,48(x13), 36,46(x15)	Out	Data terminal ready signal. When ready, these signals go active to enable the terminal transmitter. When not ready they go inactive to disable the transfer from the terminal.
/RTSA, /RTSB	39,47(x13), 37,45(x15)	Out	Request to send signal. "0" when transmitting serial data. They are active when enabling their receivers to transmit data.
/CTSA, /CTSB	40,46(x13), 38,44(x15)	In	Clear to send signal. When "0", after transmitting these signals the modem is ready to receive serial data. When ready, these signals go active to enable terminal transmitter. When not ready, these signals go inactive to disable transfer from the terminal.
/DCDA, /DCDB	41,45(x13), 39,43(x15)	In	Data carrier detect signal. When "0", serial data can be received. These signals are active to enable receivers to transmit.

SYSTEM CONTROL SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
IEI	60(x13), 72(x15)	In	Interrupt enable input signal. IEI is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.
IEO	59(x13), 71(x15)	Out	The interrupt enable output signal. In the daisy chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is "1" and the CPU is not servicing an interrupt from the on-chip peripherals.
/CS0 (C13/C15 only)	42(C13), 40(C15)	Out	Chip Select 0. Used to access external memory or I/O devices. This pin has been assigned to "ICT" pin on Z84013/015. This signal is decoded only from A15-A12 without control signals. Refer to "Functional Description" on-chip select signals for further explanation.

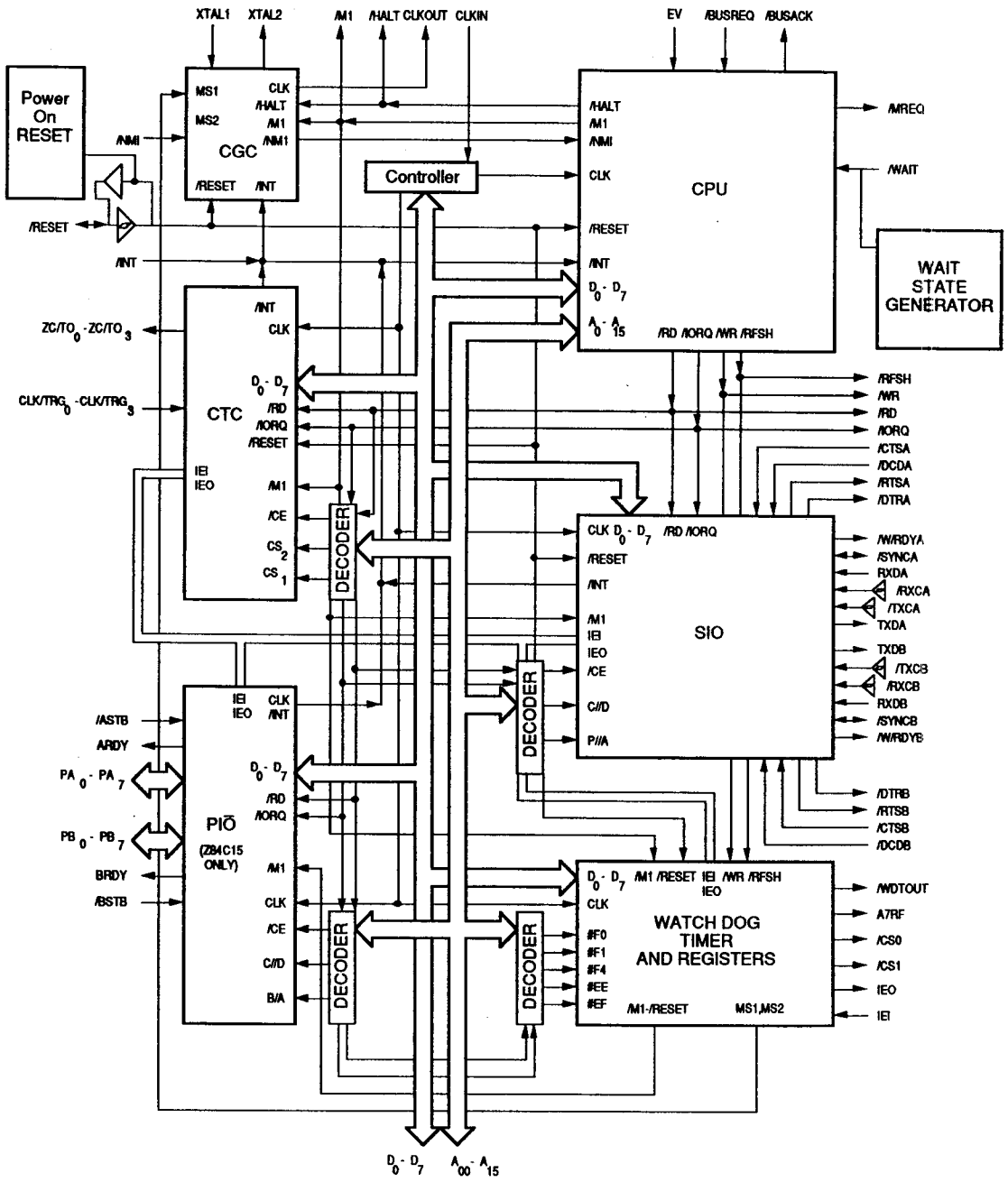


Figure 5(b). Block Diagram for 84C13/C15 IPC

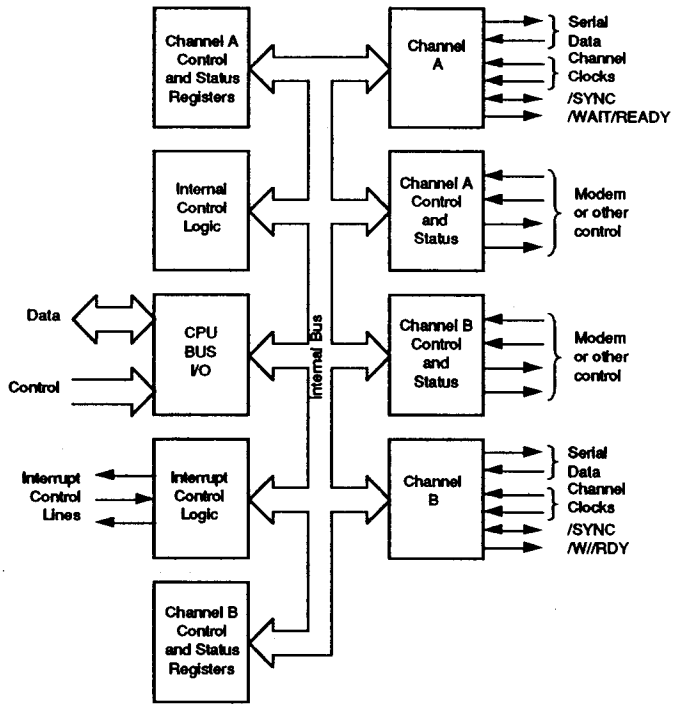


Figure 8. SIO Block Diagram

Watch Dog Timer (WDT) Logic Unit
This logic unit has been superintegrated into the IPC. It detects an operation error, caused by the program runaway, and returns to normal operation. Figure 9, shows the block diagram of the WDT. Upon Power-On Reset, this unit is enabled. If WDT is not required, but /WDTOUT is connected to /RESET or any other circuit, it has to be disabled. During the power-down mode of operation (either IDLE1/2 or Stop), the Watch Dog Timer is halted.

WDT Output (/WDTOUT pin). When the WDT is used, the "0" level signal is output from the /WDTOUT pin after a duration of time specified in the WDTP or in the WDTMR. The output pulse width is one of the following, depending on the /WDTOUT pin connection.

- The /WDTOUT is connected to the /RESET pin: The "0" level is pulsed for 5TcC (System clock cycles).
- The /WDTOUT is connected to a pin other than the /RESET pin: The "0" level is kept until the Watch Dog timer is cleared by software, or reset by /RESET pin.

CGC Logic Unit. The IPC has CGC (Clock Generator/Controller) unit. This unit is identical to the one with the Z84C01 and the Z84C50, and supports power-down modes of operation. The output from this unit is on the pin called CLKOUT, and is not connected to the system clock internally. The CLKIN pin is the system clock input. The user can connect CLKOUT to CLKIN to utilize this CGC unit, or supply external clock from CLKIN pin.

The CGC unit allows crystal input (XTAL1, XTAL2) or External Clock input on the XTAL1 pin. It has clock divide-by-two circuits and generates a half-speed clock to the input.

Z84C13/C15. The power-down modes of the IPC vary depending upon whether the system clock is fed from the CGC unit (tie CLKOUT to CLKIN) or the external clock source on the CLKIN pin. They also have divide-by-one Mode. If the clock is supplied by this CGC unit, all of the modes in "halt" state are available. When external clock is provided on the CLKIN pin, XTAL1 is not left open (tied to "0" or "1") to avoid meta-stable conditions to minimize power consumption.

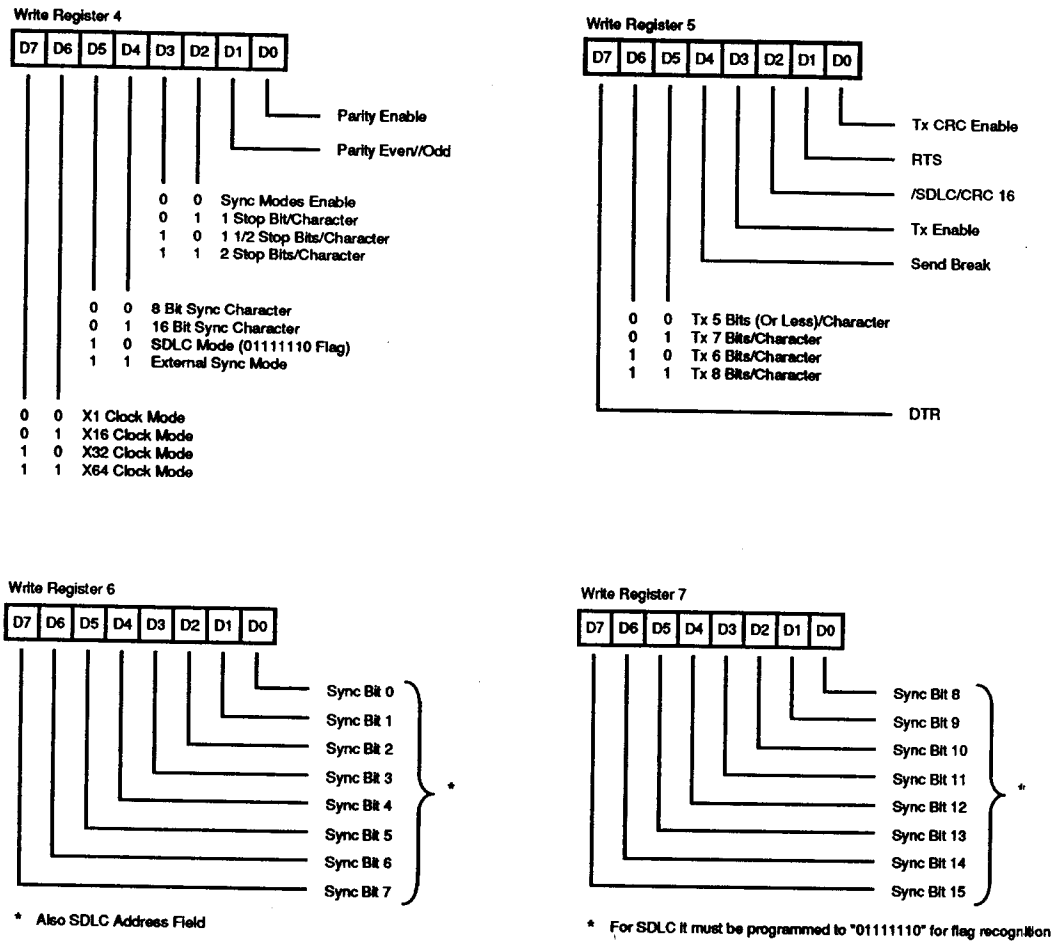


Figure 21. SIO Write Registers (Continued)

WATCH DOG CONTROL REGISTERS

There are two registers to control Watch Dog Timer operations. These are Watch Dog Timer Master Register (WDTMR; I/O Address F0h) and the WDT Command Register (WDTCR; I/O Address F1h). Watch Dog Timer Logic has a "double key" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop due to program runaway. Programming the WDT follows this procedure. Also, these registers program the power-down mode of operation. The "Second key" is needed when turning off the Watch Dog Timer.

Enabling the WDT. The WDT is enabled by setting the WDT Enable Bit (D7:WDTE) to "1" and the WDT Periodic field (D5,D6:WDTP) to the desired time period. These command bits are in the Watch Dog Timer Master Register (WDTMR; I/O Address F0h).

Disabling the WDT. The WDT is disabled by clearing WDT Enable bit (WDTE) in the WDTMR to "0" followed by writing "B1h" to the WDT Command Register (WDTCR; I/O Address F1h).

Bit D3. *Reset Output Disable.* "0"-Reset output is enabled, "1"-Reset output is disabled. This bit controls the /RESET signal and is driven out when reset input is used to take the Z84C13/C15 out of the "Halt" state. The reset pulse is driven out for 16-clock cycles from the falling edge of /RESET input, unless this bit is set. Upon Power-on reset, this bit is cleared to 0.

Bit D2. *32-Bit CRC enable.* "0"-Normal mode (16-bit CRC) "1"-32-bit CRC generation/Checking is enabled on SIO Channel A. This bit determines if the 32-bit CRC feature is enabled on Channel A of the SIO. If this bit is 0, the SIO is in a normal mode of operation. If this bit is set to 1, a normal CRC generator/checker is replaced with a 32-bit CRC generator/checker. Upon Power-on Reset, this bit is clear to "0".

Bit D1. */CS1 Enable. "0"-Disable, "1"-Enable.* This bit enables /CS1 output. While this bit is "0", /CS1 is forced to "1". While this bit is "1", /CS1 carries the address range specified in the CSBR. Upon Power-on Reset, this bit is cleared to "0".

Bit D0. */CS0 Enable. "0"-Disable, "1"-Enable.* This bit enables /CS0 output. While this bit is "0", /CS1 pin is forced to "1". While this bit is "1", the /CS0 carries address range specified in the CSBR. Upon Power-on Reset, this bit is set to "1".

Operation modes

There are four kinds of operation modes available for the IPC in connection with clock generation; RUN Mode, IDLE1/2 Modes and STOP Mode.

The Operation mode is effective when the HALT instruction is executed. Restart of the MPU from the stopped state under IDLE1/2 Mode or STOP mode is affected by inputting either /RESET or interrupt (/NMI or /INT). The mode selection of these power-down modes is made by programming the HALTM field (Bit D4-3) of WDTMR.

Setting Halt Mode

Duplicate control is provided to prevent the stopping of the WDT operation caused by the halt mode setting an error due to program runaway. As described in the programming section, changing the Halt Mode field of WDTMR is in two steps. First, write "DBh" to WDTCR followed by a write to the WDTMR with the value in HALTM. Table 2 has descriptions of each mode, and Table 3 has device status in the Halt state.

Table 2. Power-down Modes

(When using on-chip CGC unit; CLKOUT and CLKIN are tied together)

Operation Mode	WDTMR Bit D4	Bit D3	Description at HALT State
RUN Mode	1	1	The IPC continues the operation and continuously supplies a clock to the outside.
IDLE1 Mode	0	0	The internal oscillator's operation is continued. Clock output (CLKOUT) as well as internal clock to the CPU, PIO, SIO, CTC and the Watch Dog Timer is stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
IDLE2 Mode	0	1	The internal oscillator and the CTC's operation continues and supplies clock to the outside on the CLKOUT pin continuously. But the internal clock to the CPU, PIO, SIO and the Watch Dog Timer is stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
STOP Mode	1	0	All operations of the internal oscillator, clock (CLK) output, internal clock to the CPU, PIO, CTC, SIO and the Watch Dog Timer are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.

In IDLE2 Mode, the internal oscillator and clock output (CLKOUT) continue to operate. The internal system clock, fed from CLKIN to the components other than CTC is stopped at the T4 Low state of HALT instruction execution.

STOP Mode (HALTM=10). Shown in Figure 34 is the basic timing when the halt instruction is executed in STOP Mode.

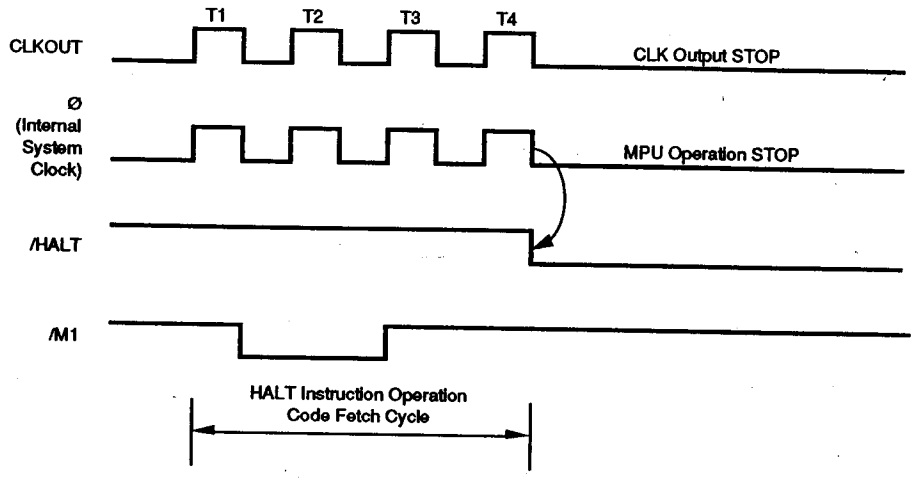


Figure 34. STOP Mode Timing
(At Halt Instruction Execution)

In STOP Mode, the on-chip CGC unit is stopped at T4 Low state of HALT instruction execution. Therefore, clock output (CLKOUT), operation of Watch Dog Timer, CPU, PIO, CTC, SIO are stopped.

Release from Halt State. The halt state of the CPU is released when "0" is input to the /RESET signal and the MPU is reset or an interrupt request is accepted. An interrupt request signal is sampled at the leading edge of the last clock cycle (T4 state) of NOP instruction. In case of the maskable interrupt, interrupt will be accepted by an active /INT signal ("0" level). Also, the interrupt enable flip-flop is set to "1". The accepted interrupt process is started from the next cycle.

Further, when the internal system clock is stopped (IDLE1/2 Mode, STOP Mode), it is necessary first to restart the internal system clock. The internal system clock is restarted when /RESET or interrupt signal (/NMI or /INT) is asserted.

RUN Mode (HALTM=11). The halt release operation is enabled by interrupt request in RUN Mode (Figure 35).

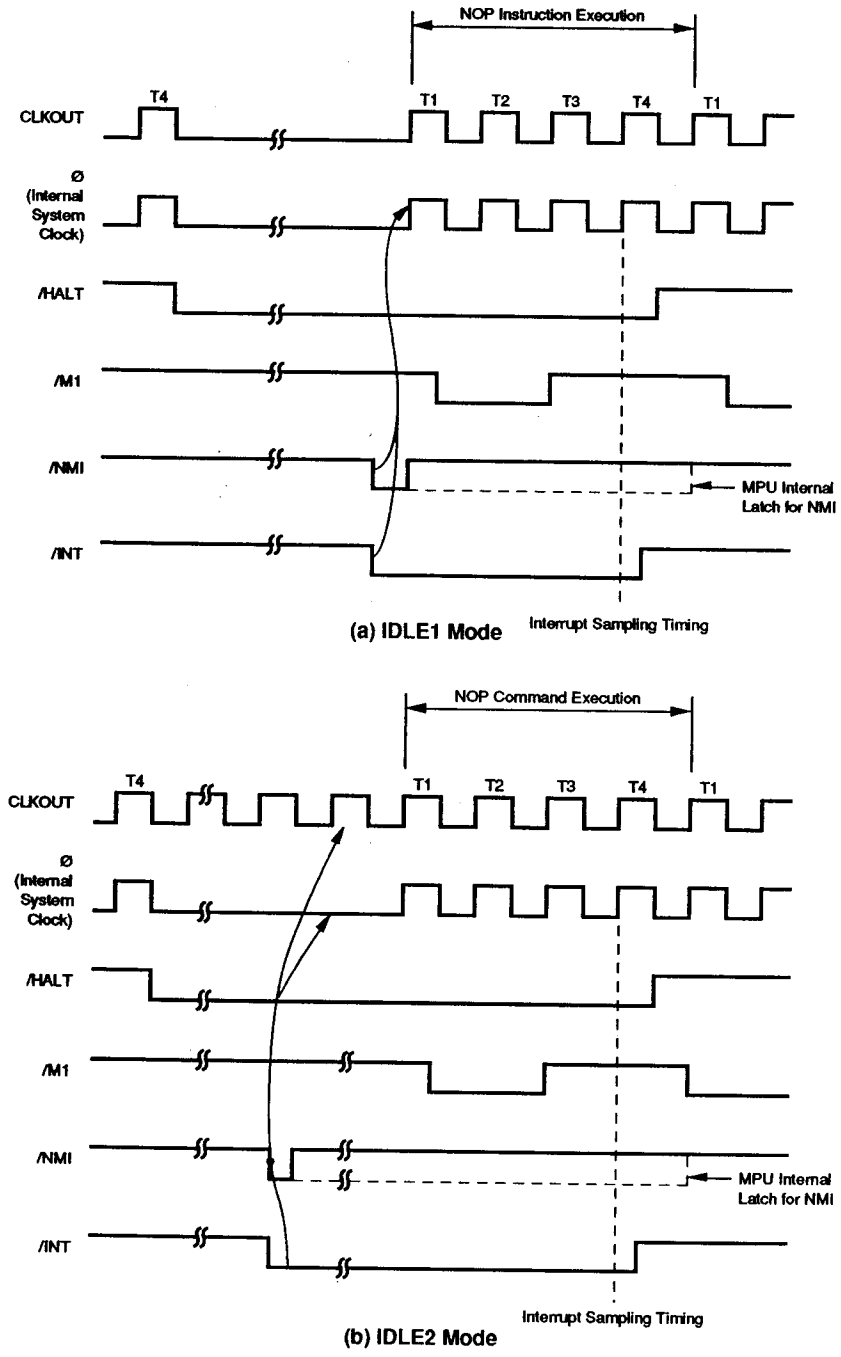


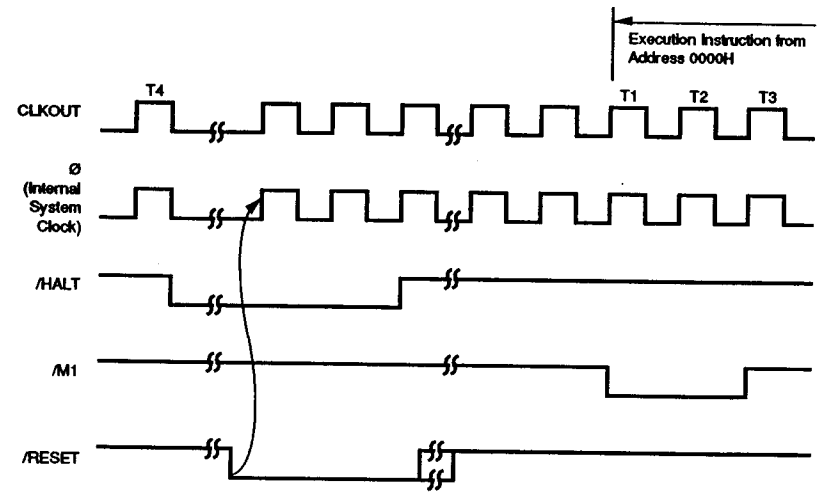
Figure 37. Halt Release Operation Timing By Interrupt Request Signal in IDLE1/2 Mode

When receiving /NMI or /INT signals, the stopped internal system clock starts to feed. In IDLE1 Mode, the IPC starts clock output on CLKOUT at the same time.

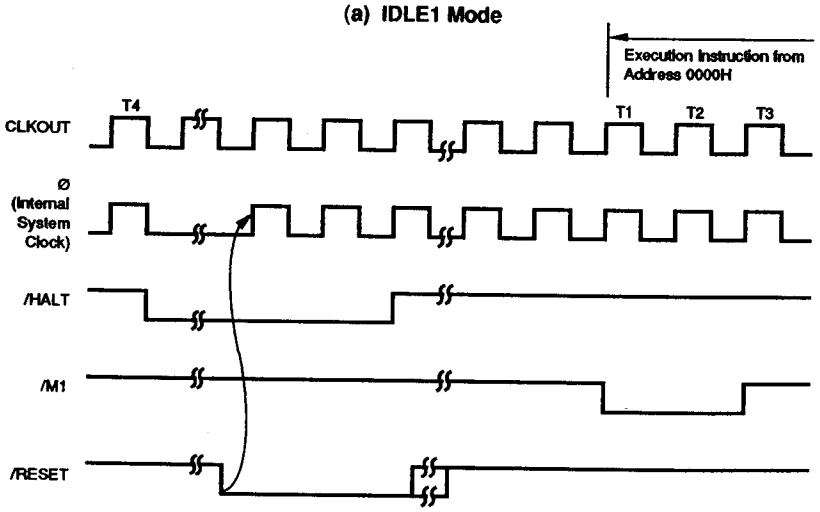
The operation stop of CPU in IDLE2 mode is taking place at "0" level during T4 state in the halt instruction op-code fetch cycle. Therefore, after being restarted by the interrupt signal, CPU executes one NOP instruction and samples an interrupt signal at the rise of T4 state during the execution of this NOP instruction, and executes the interrupt process from next cycle.

If no interrupt signal is accepted during the execution of the first NOP instruction after the internal system clock is restarted, CPU is not released from the halt state. It is placed in IDLE1/2 Mode again at "0" level during T4 state of the NOP instruction, stopping the internal system clock. If /INT signal is not at "0" level at the rise of T4 state, no interrupt request is accepted.

The halt release operation resets the IPC in IDLE1 Mode (Figure 38a) and in IDLE2 Mode (Figure 38b).



(a) IDLE1 Mode



(b) IDLE2 Mode

Figure 38. Halt Release Operation Timing By Reset in IDLE1/2 Mode

Instruction Op-code Fetch. The CPU places the contents of the Program Counter (PC) on the address bus at the start of the cycle (Figure 41). Approximately one-half clock cycle later, /MREQ goes active. When active, /RD indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the /WAIT input with the falling edge of clock state T2. During clock states T3 and T4 of an M1 cycle, dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction.

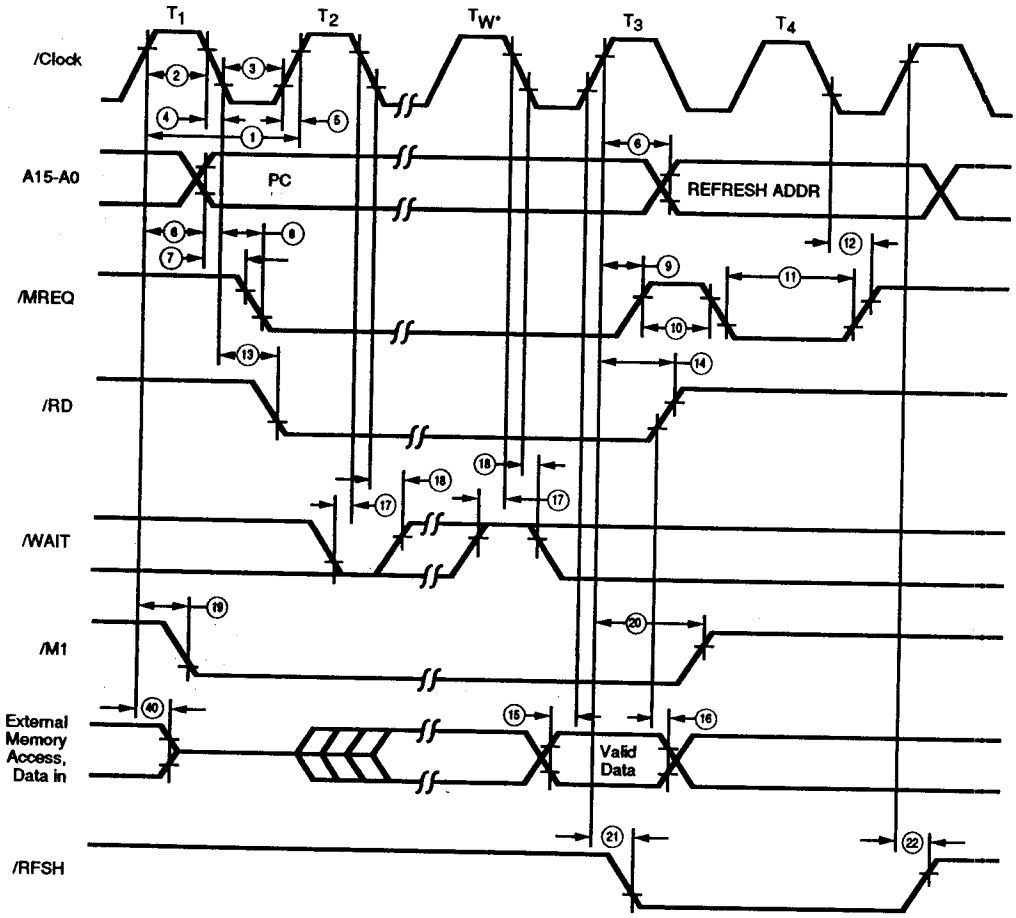


Figure 41. Instruction Op-code Fetch
(See Table A)

Memory Read or Write Cycles. Figure 42 shows the timing of memory read or write cycles other than an Op-code fetch (/M1) cycle. The /MREQ and /RD signals function like the Op-code fetch cycle.

In a memory write cycle, /MREQ also becomes active when the Address Bus is stable. The /WR line is active when the Data Bus is stable, so that it can be used directly as an R/W pulse to most semiconductor memories.

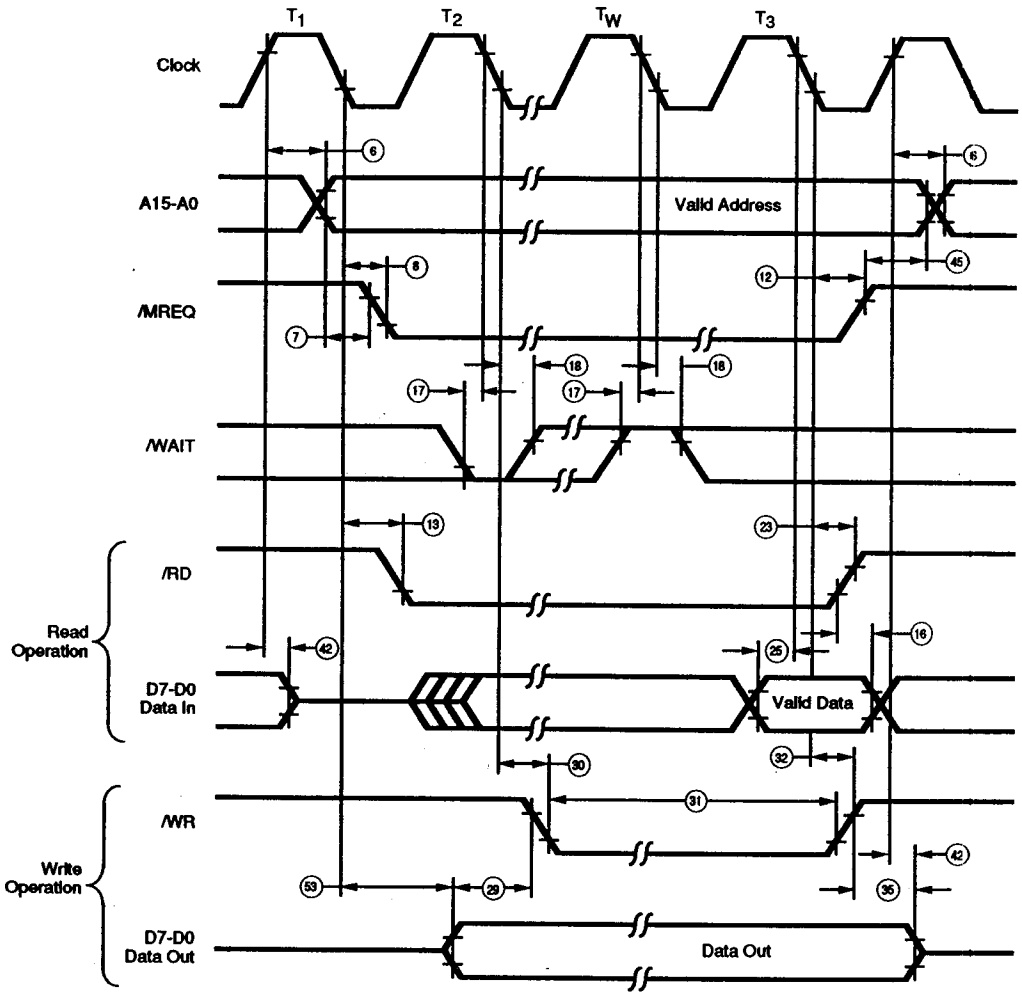
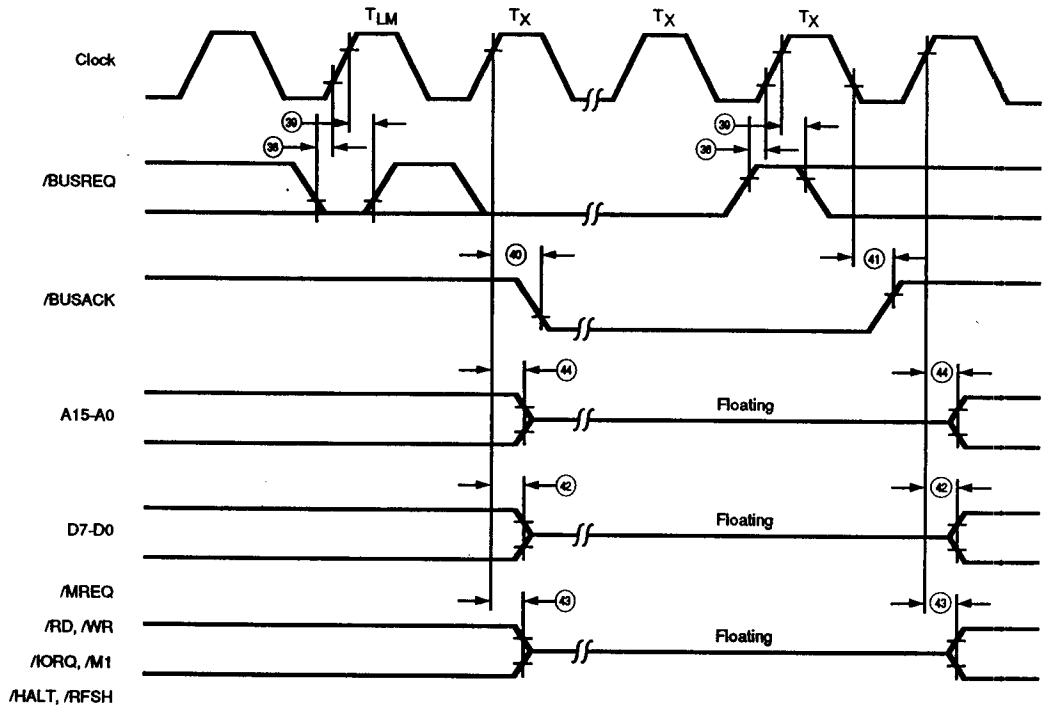


Figure 42. Memory Read or Write Cycle
(See Table A)

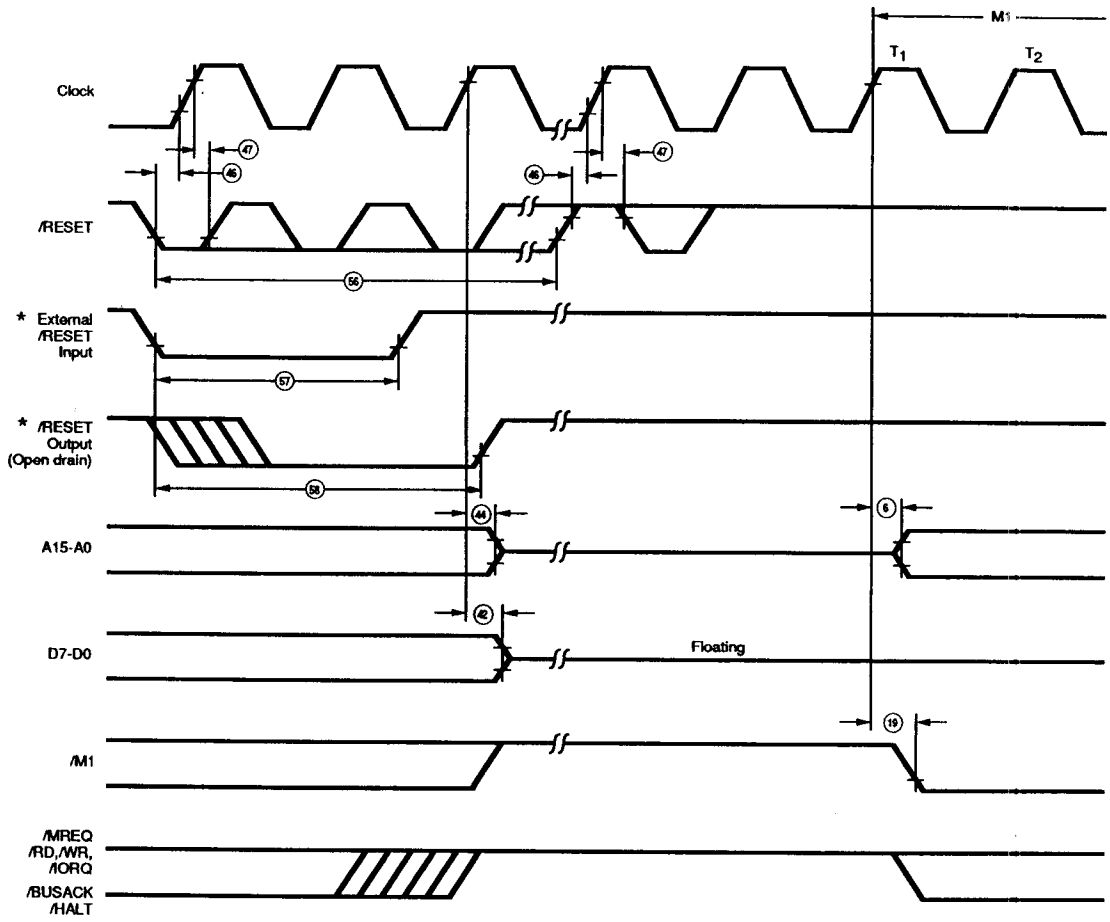
Bus Request/Acknowledge Cycle. The CPU samples /BUSREQ with the rising edge of the last clock period of any machine cycle (Figure 46). If /BUSREQ is active, the CPU sets its address, data, and /MREQ to Inputs, and /IORQ, /RD and /WR lines set to an input for on-chip peripheral access from an external bus master with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.



Notes: 1) T_{LM} = Last state of any M cycle

2) T_X = An arbitrary clock cycle used by requesting device

Figure 46. BUS Request/Acknowledge Cycle
(See Table A)



* 84C13/15 Only Reset Output is Enabled

Figure 48. Reset Cycle
(See Table A)

CGC TIMING

Figure 49 to Figure 52 shows the timing related CGC and Power-On Reset circuit.

Parameters referenced in Figure 49 thru Figure 52 appear in Table B.

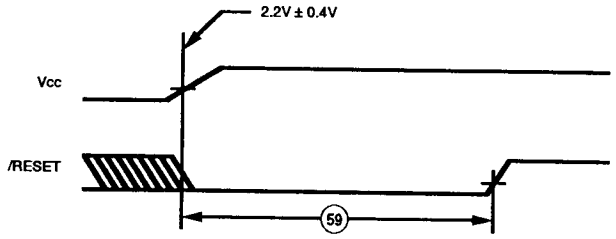


Figure 49. Reset on Power-up (Applies only for Z84C13/C15)
(See Table B)

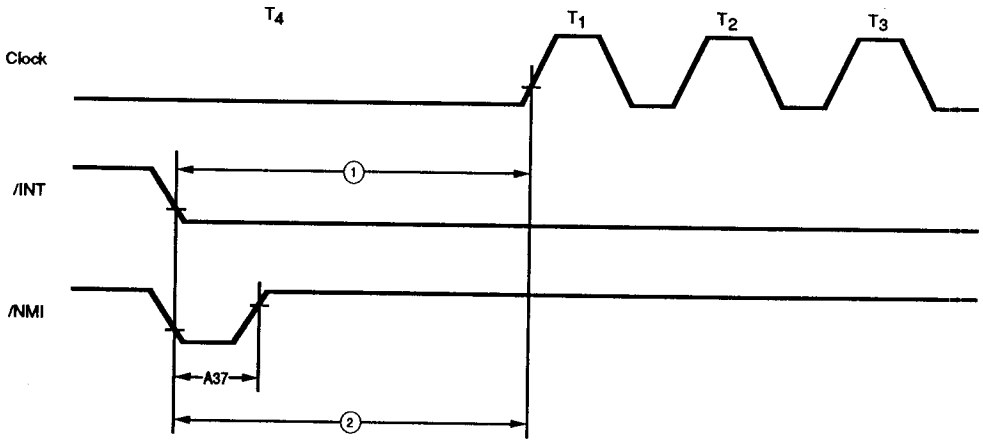
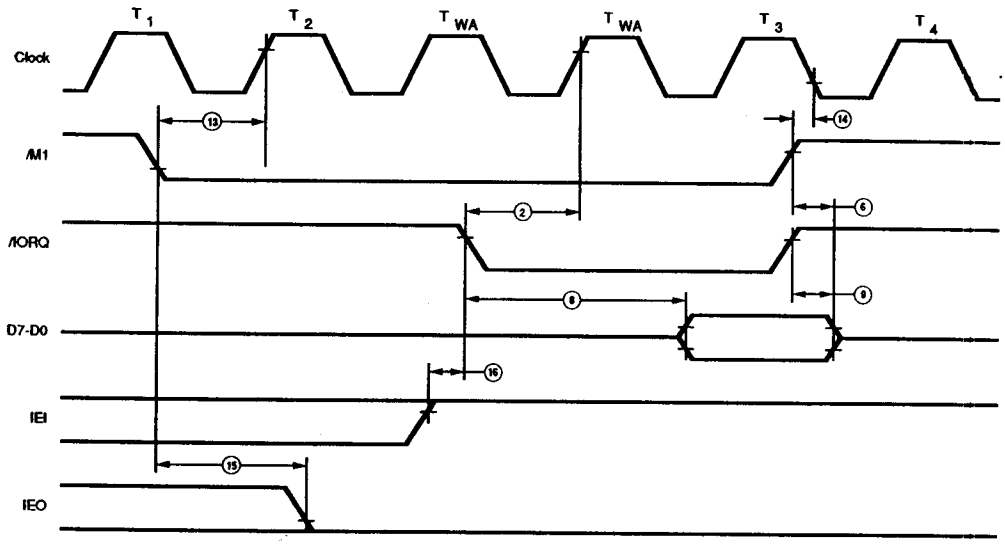
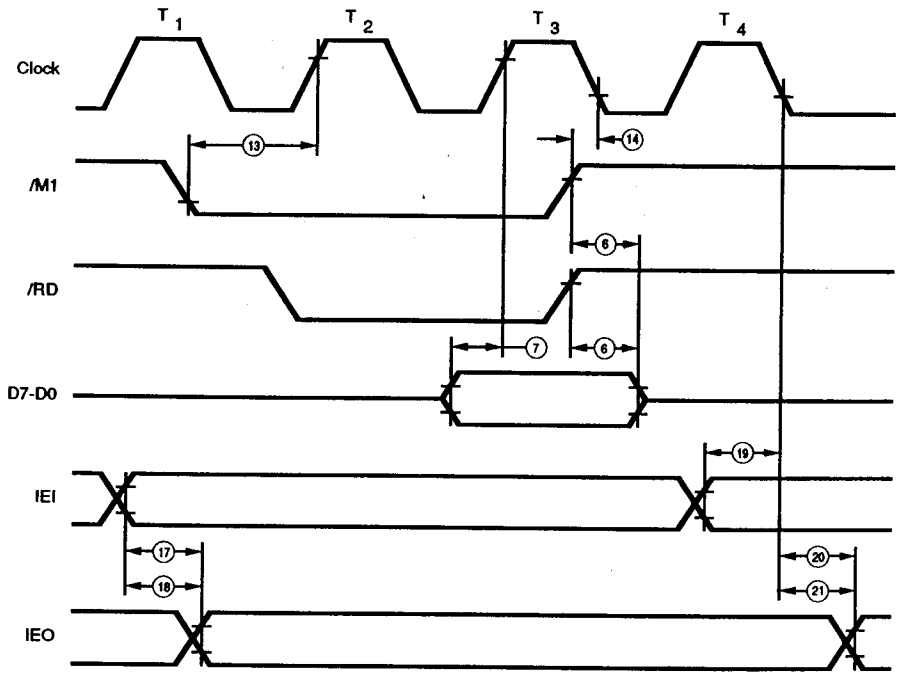


Figure 50. Clock Restart Timing by /INT, /NMI (STOP Mode)
(See Table B)



(b) Interrupt Acknowledge Cycle Timing for On-chip peripheral from External Bus master
(See Table C)



(c) Op-code fetch Cycle Timing for On-chip peripheral from External Bus master
(See Table C)

Figure 53. On-chip Peripheral Timing from External Bus master (Continued)

PIO timing
(Not applicable on Z84x13) Figure 54 shows the timing for on-chip PIO.

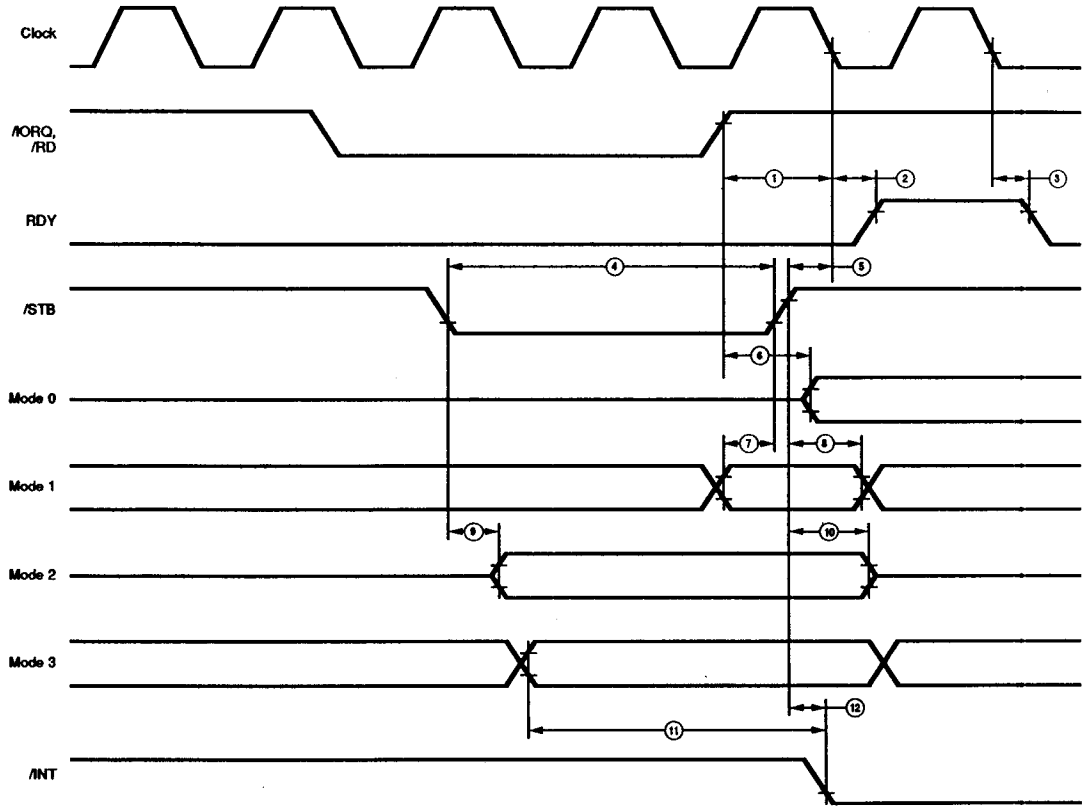


Figure 54. PIO Timing
(See Table D)

SIO Timing

Figure 56 shows the timing for on-chip SIO.

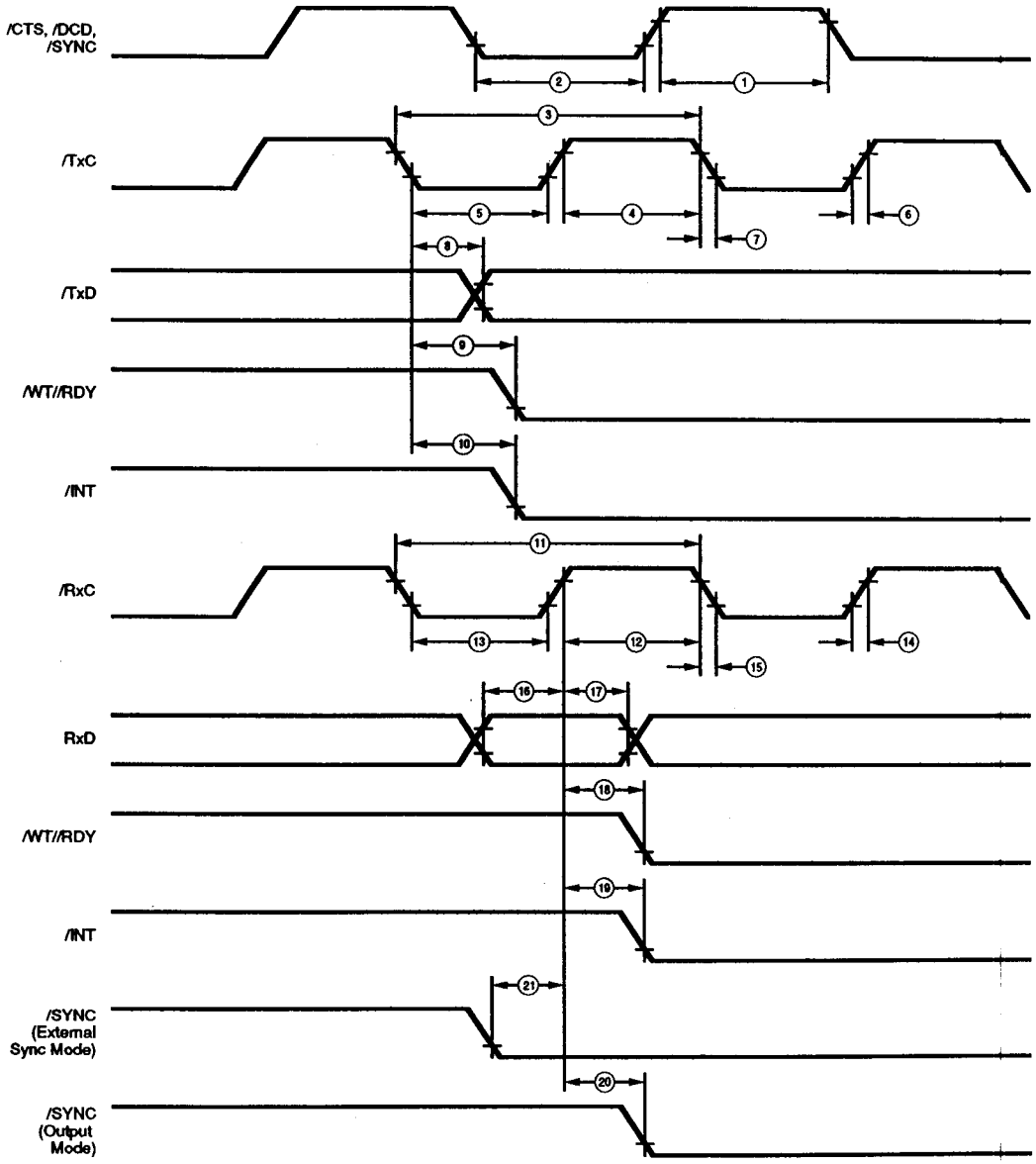


Figure 56. SIO Timing
(See Table F)

AC CHARACTERISTICS (Continued)

Table A. CPU Timing (Continued)

No	Symbol	Parameter	Z84X1306 Z84X1506 Min	Z84X1306 Z84X1506 Max	Z84X1310 Z84X1510 Min	Z84X1310 Z84X1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
41	TdCf(BUSACKr)	Clock Fall to /BASACK Rise Delay		90		75		40	ns	
42	TdCr(Dz)	Clock Rise to Data Float Delay		80		65		40	ns	
43	TdCr(CTz)	Clock Rise to Control Outputs Float Delay (/MREQ, /IORQ, /RD and /WR)		70		65		40	ns	
44	TdCr(Az)	Clock Rise to Address Float Delay		80		75		40	ns	
45	TdCTr(A)	Address Hold Time from /MREQ, /IORQ, /RD or /WR	35**		20**			0	ns	
46	TsRESET(Cr)	/RESET to Clock Rise Setup Time	60		40		15		ns	
47	ThRESET(Cr)	/RESET to Clock Rise Hold Time	10		10		10		ns	
48	TsINTf(Cr)	/INT Fall to Clock Rise Setup Time	70		50		15		ns	
49	ThINTr(Cr)	/INT Rise to Clock Rise Hold Time	10		10		10		ns	
50	TdM1f(IORQf)	/M1 Fall to /IORQ Fall Delay	359**		220**		100		ns	
51	TdCf(IORQf)	Clock Fall to /IORQ Fall Delay		70		55		45	ns	
52	TdCf(IORQr)	Clock Rise to /IORQ Rise Delay		70		55		45	ns	
53	TdCf(D)	Clock Fall to Data Valid Delay		130		110		75	ns	
54	TRDf(D)	/RD Fall to Output Data Valid		TBD		60		40	ns	
55	TdIORQ(D)	/IORQ Fall to Output Data Valid		TBD		70		45	ns	
56	TwRESET	/RESET Pulse Width 013/015, or C13/C15 with RESET Output Disabled	3TcC		3TcC		3TcC		ns	
57	TwRESEToe	/RESET Pulse Width RESET Output Enabled	2TcC		2TcC		2TcC		ns	
58	TwRESETdo	/RESET Drive Duration RESET Output Enabled	16TcC		16TcC		16TcC		ns	
59	TwRESETpor	/RESET drive duration on Power-On Sequence	10	75	10	75	10	75	ms	

Notes:

* 16 MHz Timings are preliminary and subject to change. Only C version

** For clock period other than the minimum shown, calculate parameters using the formula on Table H.

[A1] These parameters apply to the external Clock input on CLKIN pin. For the cases where external Clock is fed from XTAL1, please refer to Table B.

[A2] For loading >= 50 pF, decrease width by 10 ns for each additional 50 pF.

AC CHARACTERISTICS (Continued)

Table D. PIO Timing (Z84x15 only) (See Figure 54)

No	Symbol	Parameter	Z84C1506 Min	Z84C1506 Max	Z84C1510 Min	Z84C1510 Max	Z84C1516* Min	Z84C1516* Max	Unit	Note
1	TslOr(Cr)	/IORQ Rise to Clock Fall Setup Time (To Activate RDY on Next Clock Cycle)	100		100		100		ns	
2	TdCf(RDYr)	Clock Fall to RDY Rise Delay		100		115		30	ns	[D2]
3	TdCf(RDYf)	Clock Fall to RDY Fall Delay		100		115		30	ns	[D2]
4	TwSTB	/STB Pulse Width	100		80		50		ns	[D1]
5	TsSTBr(Cr)	/STB Rise to Clock Fall Setup Time (To Activate RDY on Next Clock Cycle)	100		100		70		ns	[D2]
6	TdIOr(PD)	/IORQ Rise to Port Data Stable Delay (Mode 0)		140		120		100	ns	[D2]
7	TsPD(STBr)	Port Data to /STB Rise Setup Time (Mode 1)	140		75		30		ns	
8	ThPD(STBr)	Port Data to /STB Rise Hold Time (Mode 1)	15		15		15		ns	
9	TdSTBf(PD)	/STB Fall to Port Data Stable (Mode 2)		150		120		30	ns	[D2]
10	TdSTBr(PDz)	/STB Rise to Port Data Float Delay (Mode 2)		140		120		50	ns	
11	TdPD(INTf)	Port Data Match to /INT Fall Delay (Mode 3)		250		200		40	ns	
12	TdSTBr(INTf)	/STB Rise to /INT Fall Delay		290		220		75	ns	

Notes:
[D1] For Mode 2: TwSTB >TsPD(STB).
[D2] Increase these values by 2 ns for 10 pF increase in loading up to 100 pF Max.

Table E. CTC Timing (Figure 55)

No	Symbol	Parameter	Z84C1306 Z84C1506 Min	Z84C1306 Z84C1506 Max	Z84C1310 Z84C1510 Min	Z84C1310 Z84C1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
1	TdCr(INTf)	Clock Rise to /INT Fall Delay		(TcC+100)		(TcC+80)		(TcC+30)		[E1]
2	TsCTR(Cc)	CLK/TRG to Clock Rise Setup Time for Immediate Count	90		90		40		ns	[E2]
3	TsCTR(Ct)	CLK/TRG to Clock Rise Setup Time for Enabling of Prescalor on Following Clock Rise	90		90		40		ns	[E1]
4	TdCTR(INTf)	CLK/TRG to /INT Fall Delay TsCTR(C) Satisfied		(1)+(3)		(1)+(3)		(1)+(3)	ns	[E2]
		TsCTR(C) not Satisfied		TcC+(1)+(3)		TcC+(1)+(3)		TcC+(1)+(3)	ns	[E2]
5	TcCTR	CLK/TRG Cycle time	(2TcC)	DC	(2TcC)	DC	(2TcC)	DC	ns	[E3]
6	TwCTRh	CLK/TRG Width (Low)	90	DC	90	DC	25	DC	ns	
7	TwCTRl	CLK/TRG Width (High)	90	DC	90	DC	25	DC	ns	
8	TrCTR	CLK/TRG Rise Time		30		30		15	ns	
9	TfCTR	CLK/TRG Fall Time		30		30		15	ns	
10	TdCr(ZCr)	Clock Rise to ZC/TO Rise Delay		80		80		25	ns	
11	TdCf(ZCf)	Clock Fall to ZC/TO Fall Delay		80		80		25	ns	

Notes:
[E1] Timer Mode.
[E2] Counter Mode.
[E3] Counter Mode only; when using a cycle time less than 3TcC, parameter #2 must be met.

Table F. SIO Timing (See Figures 53(a) and 56)

No	Symbol	Parameter	Z84C1306 Z84C1506 Min	Z84C1306 Z84C1506 Max	Z84C1310 Z84C1510 Min	Z84C1310 Z84C1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
1	TwPh	Pulse Width (High)	150		120		80		ns	
2	TwPl	Pulse Width (Low)	150		120		80		ns	
3	TcTxC	/TxC Cycle Time	250		200		120		ns	[F1]
4	TwTxCH	/TxC Width (High)	85		80		55		ns	
5	TwTxCL	/TxC Width (Low)	85		80		55		ns	
6	TrTxC	/TxC Rise Time		60		60		60	ns	
7	TfTxC	/TxC Fall Time		60		60		60	ns	
8	TdTxCf(TxD)	/TxC Fall to TxD Delay		160		120		40	ns	
9	TdTxCf(W/RRf) (Ready Mode)	/TxC Fall to /W//RDY Fall Delay	5	9	5	9	5	8	TcC	
10	TdTxCf(INTf)	/TxC Fall to /INT Fall Delay	5	9	5	9	5	9	TcC	
11	TcRxC	/RxC Cycle Time	250		200		120		ns	[F1]
12	TwRxCh	/RxC Width (High)	85		80		55		ns	
13	TwRxCl	/RxC Width (Low)	85		80		55		ns	
14	TrRxC	/RxC Rise Time		60		60		60	ns	
15	TfRxC	/RxC Fall Time		60		60		60	ns	
16	TsRxD(RxCr)	RxD to /RxC Rise Setup Time (X1 Mode)	0		0		0		ns	
17	ThRxCr(RxD)	/RxC Rise to RxD Hold Time (X1 Mode)	80		60			40	ns	
18	TdRxCr(W/RRf)	/RxC Rise to /W//RDY Fall Delay (Ready Mode)	10	13	10	13	10	13	TcC	
19	TdRxCr(INTf)	/RxC Rise to /INT Fall Delay	10	13	10	13	10	13	TcC	
20	TdRxCr(SYNCf)	/RxC Rise to /SYNC Fall Delay (Output Modes)	4	7	4	7	4	7	TcC	
21	TsSYNCf(RxCr)	/SYNC Fall to /RxC Rise Setup (External Sync Modes)	-100		-100		-100		ns	[F2]
22	TdIOf(W/RRf)	/IORQ Fall or Valid Address to /W//RDY Delay (Wait Mode)		130		110		40	ns	[F2]
23	TdCr(W/RRf)	Clock Rise to /W//RDY Delay (Ready Mode)		85		85		40	ns	[F2]
24	TdCf(W/Rz)	Clock Fall to /W//RDY Float Delay (Wait Mode)		90		80		40	ns	[F2]

Notes:
[F1] In all modes, the System Clock rate must be at least five times the maximum data rate.
[F2] Parameters 22 to 24 are on Figure 53a.