Zilog - Z8401506FEG Datasheet

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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Z80
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	6MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8401506feg

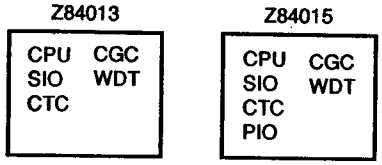


Figure 1. Z84013/015 Version

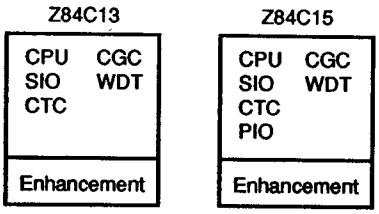


Figure 2. Z84C13/C15 Version

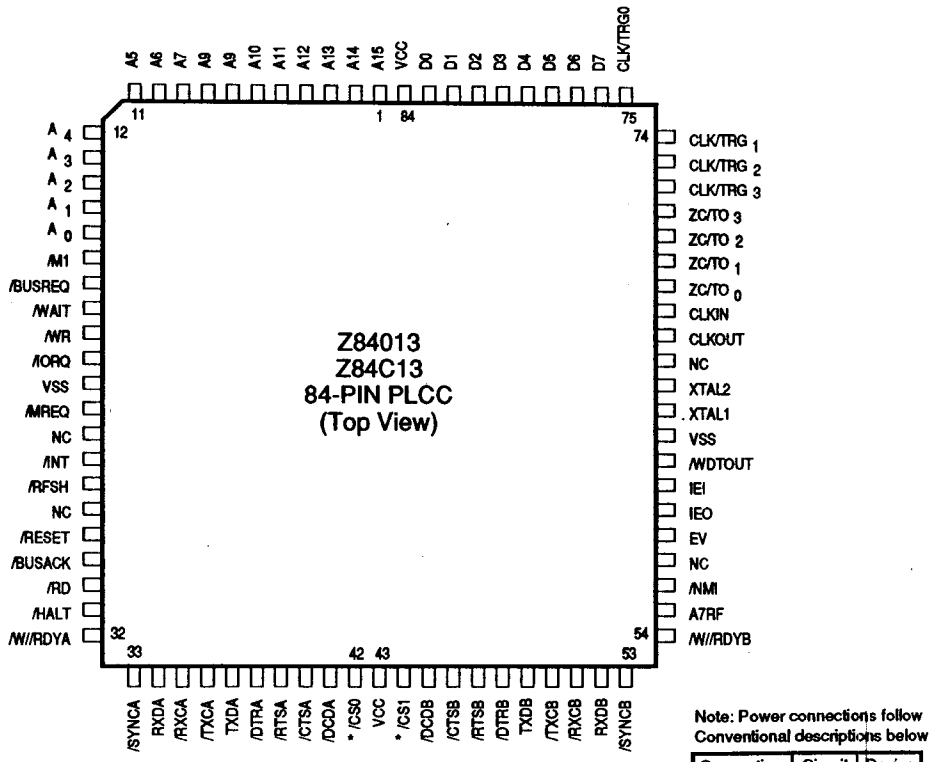
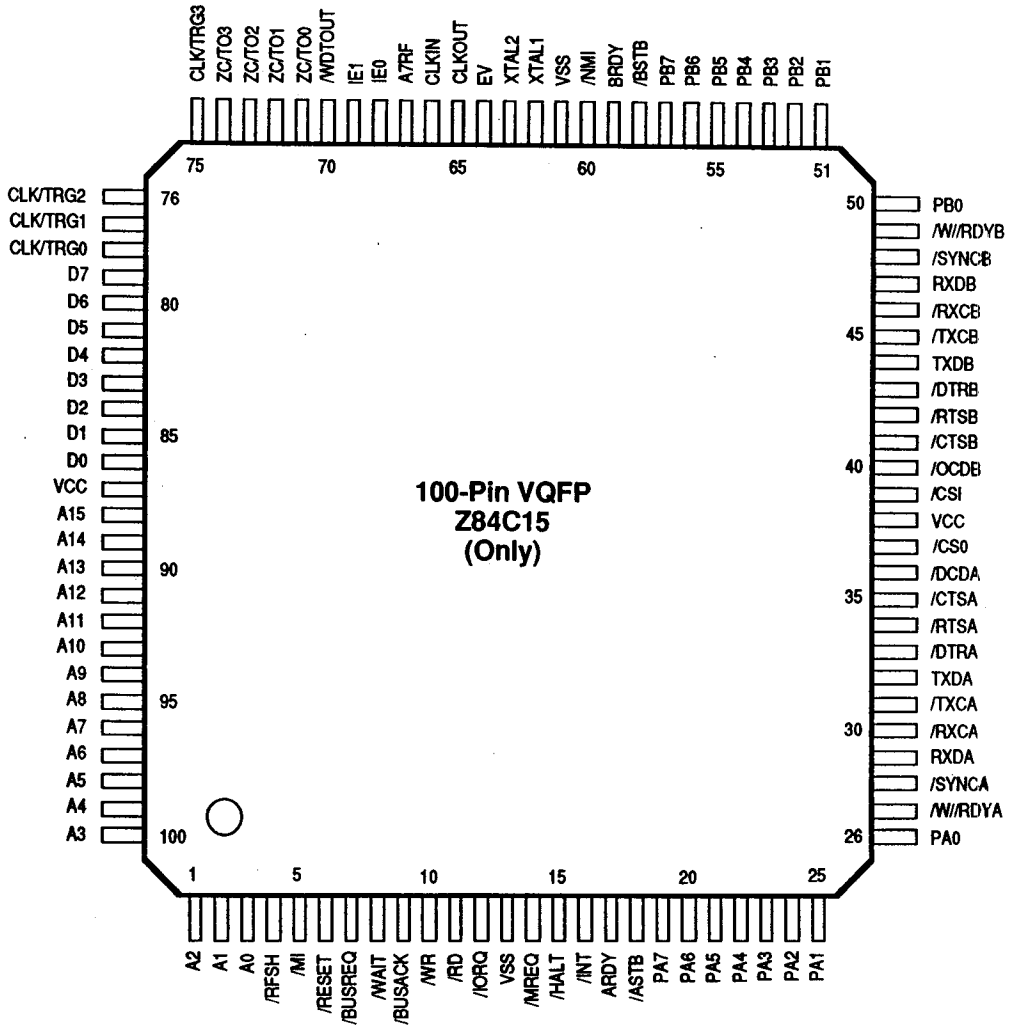


Figure 3. Z84013/Z84C13 Pin-out Assignments



Z84C15 Pin-out Assignments

SIO SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, 3-State	Function
/RxCA, /RxCB	35,51(x13), 33,49(x15)	In	Receive clock signal. In the asynchronous mode, the receive clocks can be 1, 16, 32, or 64 times the data transfer rate.
/TxCA, /TxCB	36,50(x13), 34,48(x15)	In	Transmitter clock signal. In the asynchronous mode, the transmitter clocks can be 1, 16, 32, or 64 times the data transfer rate.
TxDA, TxDB	37,49(x13), 35,47(x15)	Out	Serial transmit data signal.
/DTRA, /DTRB	38,48(x13), 36,46(x15)	Out	Data terminal ready signal. When ready, these signals go active to enable the terminal transmitter. When not ready they go inactive to disable the transfer from the terminal.
/RTSA, /RTSB	39,47(x13), 37,45(x15)	Out	Request to send signal. "0" when transmitting serial data. They are active when enabling their receivers to transmit data.
/CTSA, /CTSB	40,46(x13), 38,44(x15)	In	Clear to send signal. When "0", after transmitting these signals the modem is ready to receive serial data. When ready, these signals go active to enable terminal transmitter. When not ready, these signals go inactive to disable transfer from the terminal.
/DCDA, /DCDB	41,45(x13), 39,43(x15)	In	Data carrier detect signal. When "0", serial data can be received. These signals are active to enable receivers to transmit.

SYSTEM CONTROL SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
IEI	60(x13), 72(x15)	In	Interrupt enable input signal. IEI is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.
IEO	59(x13), 71(x15)	Out	The interrupt enable output signal. In the daisy chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is "1" and the CPU is not servicing an interrupt from the on-chip peripherals.
/CS0 (C13/C15 only)	42(C13), 40(C15)	Out	Chip Select 0. Used to access external memory or I/O devices. This pin has been assigned to "ICT" pin on Z84013/015. This signal is decoded only from A15-A12 without control signals. Refer to "Functional Description" on-chip select signals for further explanation.

SYSTEM CONTROL SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, 3-State	Function
/CS1 (C13/C15 only)	40(x13), 42(x15)	Out	Chip Select 1. Used to access external memory or I/O devices. This pin has been assigned to "ICT" pin on Z84013/015. This signal is decoded only from A15-A12 without control signals. Refer to "Functional Description" on-chip select signals for further explanation.
/WDTOUT	61(x13), 73(x15)	Out(013/015), Open Drain(C13/C15)	Watch Dog Timer Output signal. Output pulse width depends on the externally connected pin.
/RESET	28(x13), 9(x15)	Input(013/015), I/O (Open Drain) (C13/C15)	Reset signal. /RESET signal is used for initializing MPU and other devices in the system. Also used to return from the steady state in the STOP or IDLE modes.

Note: For the Z84013/Z84015 the /RESET must be kept in active state for a period of at least three system clock cycles.

Note: For the Z84C13/Z84C15, during the power-up sequence, the /RESET becomes an Open drain output and the Z84C13/C15 will drive this pin to "0" for 25 to 75 msec after the power supply passes through approx. 2.2V and then reverts to input. If it receives the /RESET signal after power-on sequence, it will drive /RESET pin for 16-processor clock cycles depending on the status of Reset Output Disable bit in Misc Control Register. If this Reset output is disabled, it must be kept in active state for a period of at least three system clock cycles. Note, that if using Z84C13/C15 in a Z84013/015 socket, modification may be required on the reset circuit since this pin is "pure input pin" on the Z84013/015. Also, the /RESET pin doesn't have internal pull-up resistors and therefore requires external pull-ups. For more details on the device, please refer to "Functional Description."

XTAL1	63(x13), 65(x15)	In	Crystal oscillator connecting terminal. A parallel resonant crystal is recommended. If external clock source is used as an input to the CGC unit, supply clock goes into this terminal. If external clock is supply to CLKIN pin (without CGC unit), this terminal must be connected to "0" or "1".
XTAL2	63(x13), 66(x15)	Out	Crystal oscillator connecting terminal.
CLKIN	67(x13), 69(x15)	In	Single-phase System Clock Input.
CLKOUT	66(x13), 68(x15)	Out	Single-phase clock output from on-chip Clock Generator/Controller.
EV	58(x13), 67(x15)	In	Evaluator signal. When "1" is applied to this pin, IPC is put in Evaluation mode.

Note: For the Z84013/015, together with /BUSREQ, the EV signal puts the IPC into the evaluation mode. When this signal becomes active, the status of /M1, /HALT and /RFSH change to input. When using Z84013/015 as an evaluator chip, the CPU is electrically disconnected after one machine cycle is executed with the EV signal "1" and the /BUSREQ signal "0". It follows the instructions from the other CPU (of ICE). Upon receiving /BUSREQ; A15-A0, /MREQ, /IORQ, /RD and /WR are changed to input and D7-D0 changes its direction. /BUSACK is NOT 3-stated so it should be disconnected by an externally connected circuit. For details, please refer to "Functional Description" on EV mode.

SYSTEM CONTROL SIGNALS (Continued)

Note: For the Z84C13/C15, to access on-chip resources from the CPU (e.g., ICE CPU), the CPU is electrically disconnected; A15-A0, /MREQ, /IORQ, /RD and /WR are changed to input; D7-D0 changes its direction; /M1, /HALT and /RFSH are put into the high impedance state when the EV pin is set to "1". Also, /BUSACK is 3-stated. For details, please refer to "Functional Description" on EV mode.

Pin Name	Pin Number	Input/Output, 3-State	Function
ICT	42,44(013), 40,42(015), Not with C13/C15	Out	Test pins. Used in the open state.
NC	24,27,57,65(x13), Not with x15		Not connected.
VCC	43,84(x13), 41,90(x15)	Power Supply	+5 Volts
VSS	22, 62(x13), 16,64(x15)	Power Supply	0 Volts

PIO SIGNALS (for the Z84x15 only)

Pin Name	Pin Number	Input/Output, 3-State	Function
/ASTB	21(x15)	In	Port A strobe pulse from a peripheral device. The signal is used as the handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see "PIO Basic Timing").
/BSTB	61(x15)	In	Port B strobe pulse from a peripheral device. This signal is used as the handshake between Port B and external circuits. The meaning of this signal is the same as /ASTB, except when Port A is in mode 2 (see "PIO Basic Timing").
ARDY	20(x15)	Out	Register A ready signal. Used as the handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see "PIO Basic Timing").
BRDY	62(x15)	Out	Register B ready signal. Used as the handshake between Port B and external circuits. The meaning of this signal is the same as ARDY except when Port A is in mode 2 (see "PIO Basic Timing").
PA7-PA0	22-29(x15)	I/O, 3-State	Port A data signals. Used for data transfer between Port A and external circuits.
PB7-PB0	53-60(x15)	I/O, 3-State	Port B data signals. Used for transfer between Port B and external circuits.

Mode Control Word

Selects the port operating mode. This word is required and is written at any time (Figure 12).

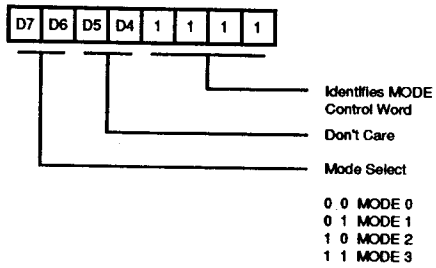


Figure 12. PIO Mode Control Word

I/O Register Control Word

When Mode 3 is selected, the Mode Control Word is followed by the I/O Register Control Word. This word configures the I/O register, which defines which port lines are inputs or outputs. A "1" indicates input while a "0" indicates output. This word is required when in Mode 3 (Figure 13).

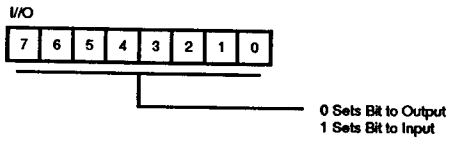
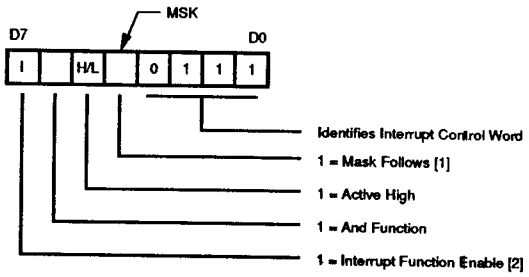


Figure 13. I/O Register Control Word

Interrupt Control Word

In Mode 3 operation, handshake signals are not used. Interrupts are generated as a logic function of the input signal levels. The Interrupt Control Word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active level, an interrupt is triggered), OR (if any one of the input bits change to the active logic level, an interrupt is triggered). The user can program which input bits are to be considered as part of this logic function. Bit D6 sets the logic function, bit D5 sets the logic level, and bit D4 specifies a mask control word to follow (Figure 14).



Note:
[1] Regardless of the operating mode, setting Bit D4 = 1 causes any pending interrupts to be cleared.
[2] The port interrupt is not enabled until the interrupt function enable is followed by an active /M1.

Figure 14. Interrupt Control Word

Mask Control Word

This word sets the mask control register, thus allowing any unused bits to be masked off. If any bits are to be masked, then bit D4 of the interrupt Control Word is set. When bit D4 of the interrupt Control Word is set, then the next word programmed is the Mask Control Word. To mask an input bit, the corresponding Mask Control Word bit is a "1" (Figure 15).

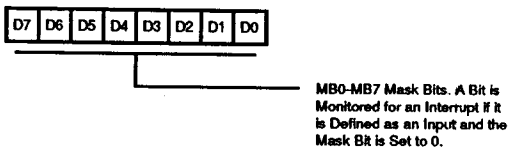


Figure 15. Mask Control Word

Interrupt Disable Word

This word can be used to enable or disable a port's interrupts without changing the rest of the port's interrupt conditions (Figure 16).

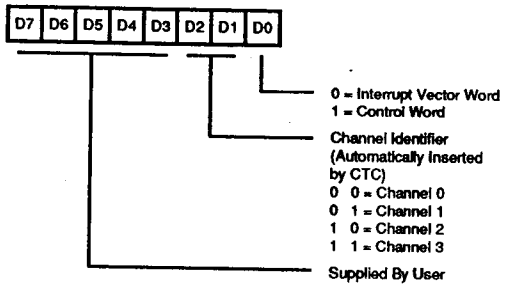


Figure 19. CTC Interrupt Vector Word

SIO REGISTERS

For more detailed information, refer to the SIO Technical Manual.

Read Registers. The SIO channel B contains three read registers while channel A contains only two that are read to obtain status information. To read the contents of a register (rather than RR0), the program must first write a pointer to WR0 in exactly the same manner as a write operation. The next I/O read cycle will place the contents of the selected read registers onto the data bus (Figure 20a, b, c).

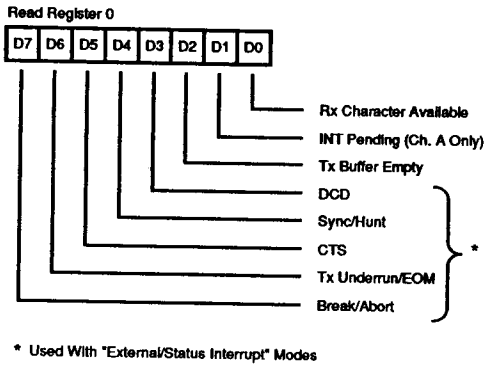


Figure 20a. SIO Read Register 0

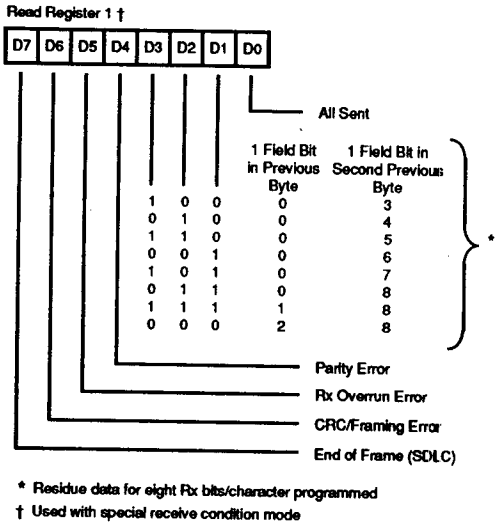


Figure 20b. SIO Read Register 1

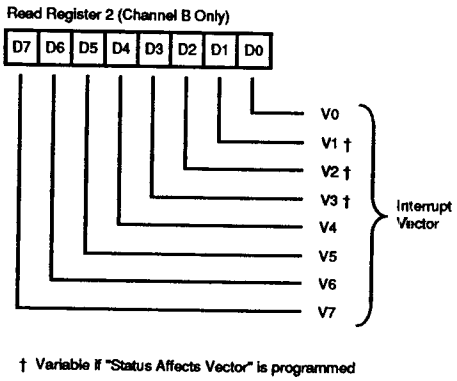


Figure 20c. SIO Read Register 2

Write Registers. The SIO Channel B contains eight write registers while Channel A contains only seven that are programmed to configure the operating mode characteristics of each channel. With the exception of WR0, programming the write registers is a two step operation. The first operation is a pointer written to WR0 which points to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel (Figure 21).

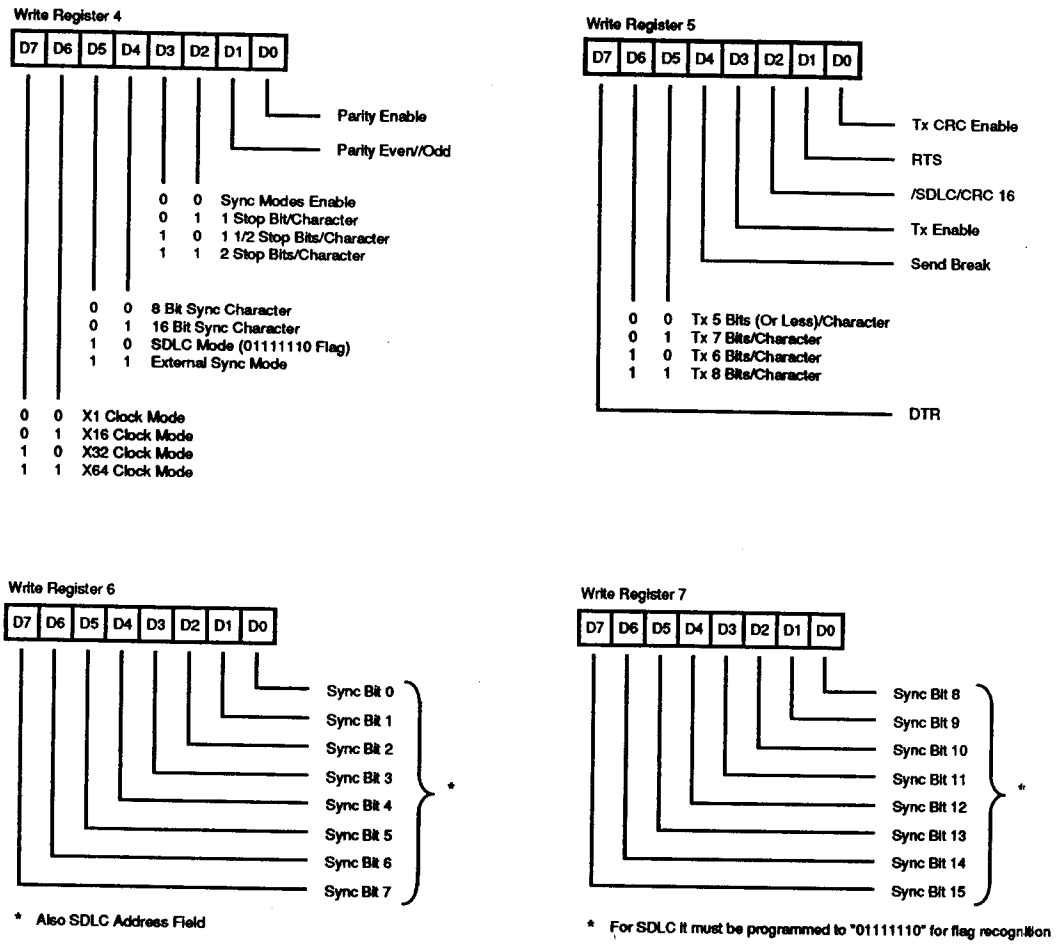


Figure 21. SIO Write Registers (Continued)

WATCH DOG CONTROL REGISTERS

There are two registers to control Watch Dog Timer operations. These are Watch Dog Timer Master Register (WDTMR; I/O Address F0h) and the WDT Command Register (WDTCR; I/O Address F1h). Watch Dog Timer Logic has a "double key" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop due to program runaway. Programming the WDT follows this procedure. Also, these registers program the power-down mode of operation. The "Second key" is needed when turning off the Watch Dog Timer.

Enabling the WDT. The WDT is enabled by setting the WDT Enable Bit (D7:WDTE) to "1" and the WDT Periodic field (D5,D6:WDTP) to the desired time period. These command bits are in the Watch Dog Timer Master Register (WDTMR; I/O Address F0h).

Disabling the WDT. The WDT is disabled by clearing WDT Enable bit (WDTE) in the WDTMR to "0" followed by writing "B1h" to the WDT Command Register (WDTCR; I/O Address F1h).

Table 3. Device status in Halt state
(When using on-chip CGC unit; CLKOUT and CLKIN are tied together)

Mode	CGC	CPU	CTC	PIO	SIO	WDT	CLKOUT
IDLE1	O	X	X	X	X	X	X
IDLE2	O	X	O	X	X	X	O
STOP	X	X	X	X	X	X	X
RUN	O	O	O	O	O	O	O

O: Operating
X: Stop

All of the operating modes listed here are valid with crystal input (Crystal connected between XTAL1/2 or external clock input on XTAL1). For the external clock on the CLKIN pin, only the IDLE2 and RUN modes are applicable.

TIMING

Basic Timing

The basic timing is explained here with emphasis placed on the halt function relative to the clock generator. The following items are identical to those for the Z84C00. Refer to the data sheet for the Z84C00.

- Operation code fetch cycle
- Memory Read/Write operation
- Input/Output operation
- Bus request/acknowledge operation
- Maskable interrupt request operation
- Non-Maskable interrupt request operation
- Reset Operation

Operation When HALT Instruction is Executed. When the CPU fetches a halt instruction in the operation code fetch cycle, /HALT goes active (Low) in synch with the falling edge of T4 state before the peripheral LSI and CPU stops the operation. After this, the system clock generation differs depending upon the operation mode (RUN Mode, IDLE1/2 Mode or STOP Mode). If the internal system clock is running, the CPU continues to execute NOP instruction even in the halt state.

RUN Mode (HALTM = 11). Shown in Figure 31 is the basic timing when the halt instruction is executed in RUN Mode.

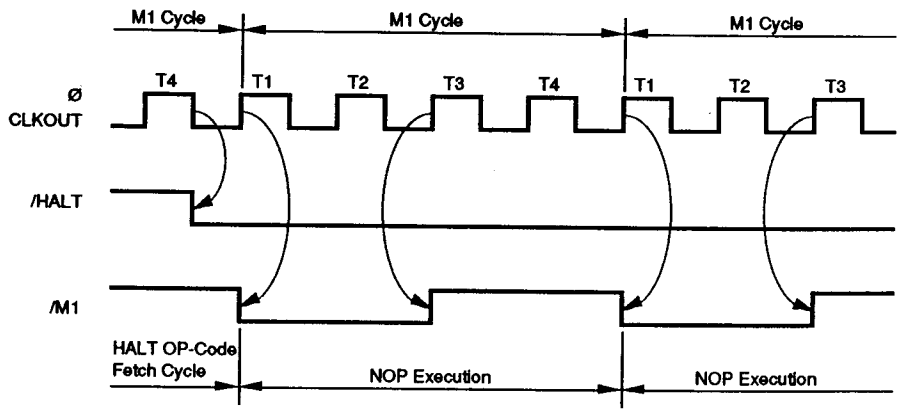


Figure 31. Timing of RUN Mode
(at Halt Instruction Command Execution)

In RUN Mode, output from the CGC unit (CLKOUT) is not stopped and the internal system clock (Ø) continues even after the halt instruction is executed. Therefore, until the halt state is released by the interrupt signal (/NMI or /INT) or /RESET signal, MPU continues to execute HALT instructions (internally executing NOP instructions).

IDLE1 Mode (HALTM=00). Shown in Figure 32 is the basic timing when the halt instruction is executed in IDLE1 Mode.

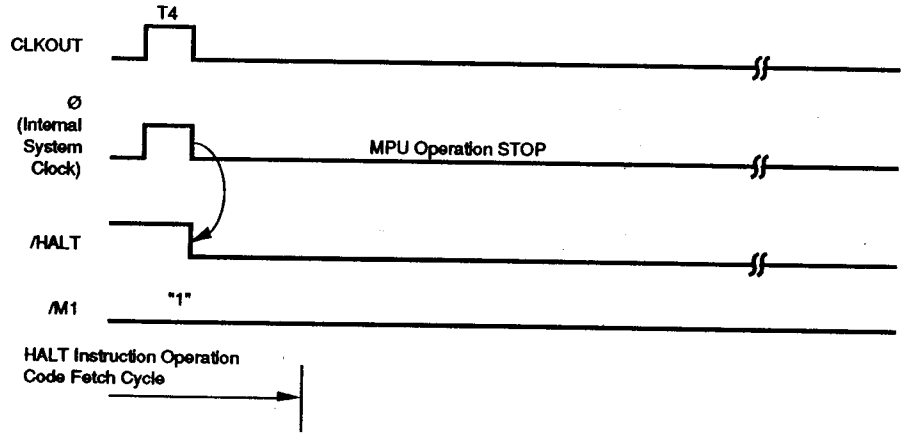


Figure 32. IDLE1 Mode Timing
(At Halt Instruction Execution)

In IDLE1 Mode, the internal oscillator continues to operate, but clock output (CLKOUT) is stopped at T4 Low state of HALT instruction execution. Then all components in the MPU stop their operation. This mode is not supported when the CGC unit is inactive and the external clock is fed from CLKIN pin; CLKOUT should be connected to CLKIN.

IDLE2 Mode (HALTM=01). Shown in Figure 33 is the basic timing when the halt instruction is executed in IDLE2 Mode.

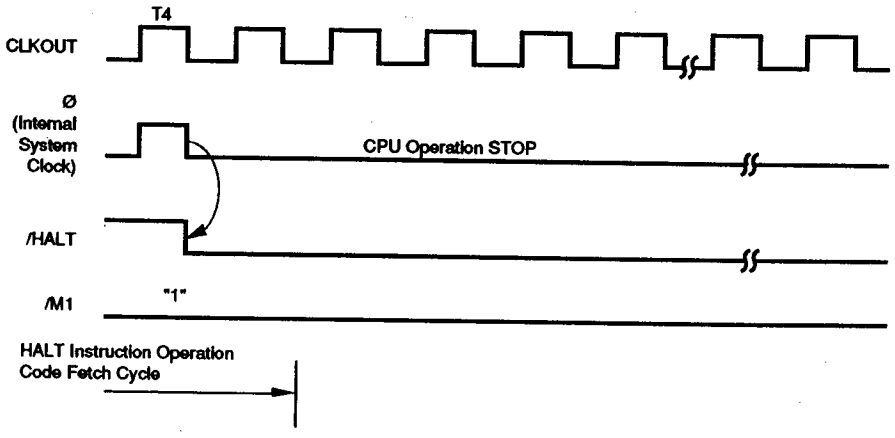


Figure 33. IDLE2 Mode Timing
(At Halt Instruction Execution)

In IDLE2 Mode, the internal oscillator and clock output (CLKOUT) continue to operate. The internal system clock, fed from CLKIN to the components other than CTC is stopped at the T4 Low state of HALT instruction execution.

STOP Mode (HALTM=10). Shown in Figure 34 is the basic timing when the halt instruction is executed in STOP Mode.

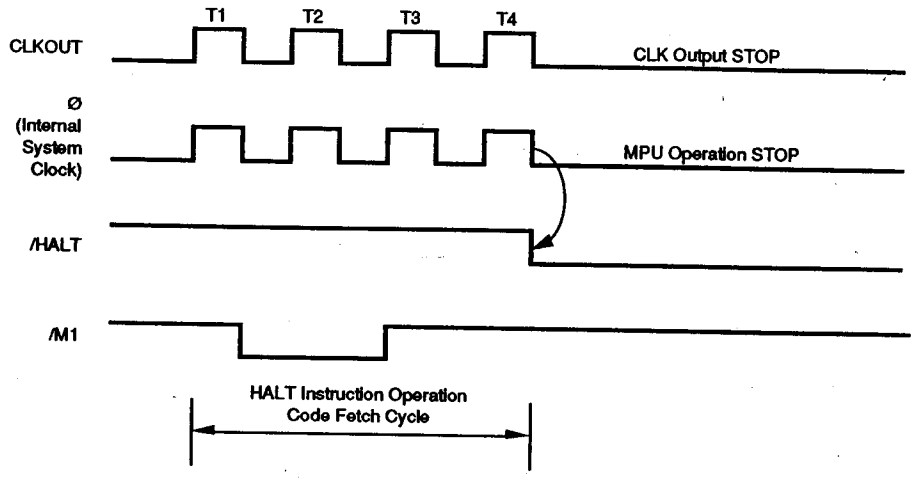


Figure 34. STOP Mode Timing
(At Halt Instruction Execution)

In STOP Mode, the on-chip CGC unit is stopped at T4 Low state of HALT instruction execution. Therefore, clock output (CLKOUT), operation of Watch Dog Timer, CPU, PIO, CTC, SIO are stopped.

Release from Halt State. The halt state of the CPU is released when "0" is input to the /RESET signal and the MPU is reset or an interrupt request is accepted. An interrupt request signal is sampled at the leading edge of the last clock cycle (T4 state) of NOP instruction. In case of the maskable interrupt, interrupt will be accepted by an active /INT signal ("0" level). Also, the interrupt enable flip-flop is set to "1". The accepted interrupt process is started from the next cycle.

Further, when the internal system clock is stopped (IDLE1/2 Mode, STOP Mode), it is necessary first to restart the internal system clock. The internal system clock is restarted when /RESET or interrupt signal (/NMI or /INT) is asserted.

RUN Mode (HALTM=11). The halt release operation is enabled by interrupt request in RUN Mode (Figure 35).

Z84C13/C15 Only. The /RESET pulse is stretched to a minimum of 16 cycles and driven out of the Z84C13/C15 on the /RESET pin if Reset output is enabled (bit D3 of MCR is cleared to "0"). Setting bit D3 disables the driving out of /RESET. The values in the control registers (WDTMR, SCRP, WCR, MWBR, CSBR and MCR) are initialized to the default value on /RESET.

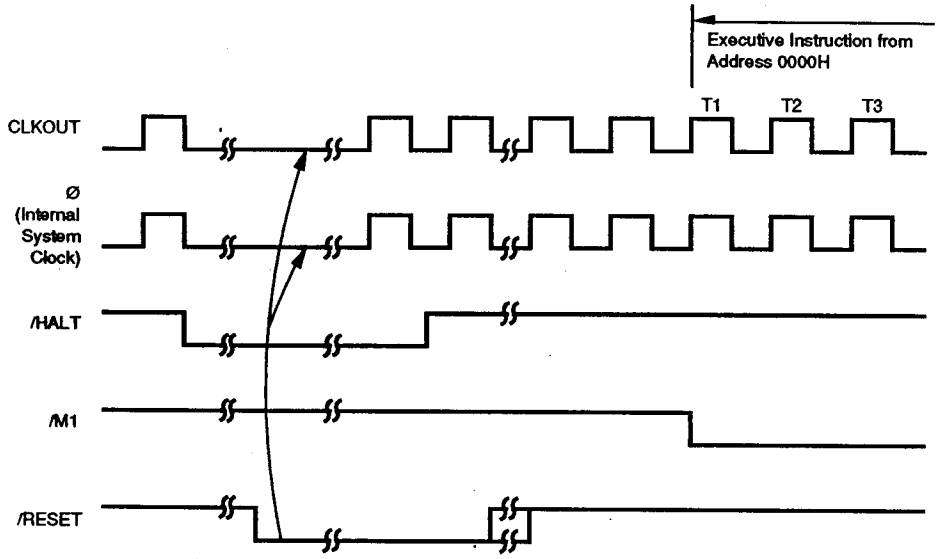


Figure 40. Halt Release Operation Timing By Reset in STOP Mode

Start-up Time at Time of Restart (STOP Mode). When the MPU is released from the halt state by accepting an interrupt request, it executes an interrupt service routine. Therefore, when an interrupt request is accepted, it starts generating clock on the CLKOUT pin, after a start-up time, by the internal counter [(2^{14}+2.5) TcC (TcC:Clock Cycle)]. This obtains a stabilized oscillation for operation.

Further, in case of restart by the /RESET signal, the internal counter does not operate.

Evaluation operation. Each of the CPU signals (A15-0, D7-0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1, /RFSH) can be 3-stated by activating the EV pin. The Z84C13/C15 enhances the counter part by eliminating the requirement of /BUSREQ to go active.

Instruction set. The instruction set of the IPC is the same for the Z84C00. For details, refer to the data sheet of the Z84C00 Technical Manual.

AC TIMING

The following section describes the timing of the IPC. The numbers appearing in the figures refer to the parameters on Table A - F.

CPU Timing
Parameters referenced in Figure 41 through Figure 48 appear in Table A.

The IPC's CPU executes instructions by proceeding through the following specific sequence of operations:

Memory read or write
I/O device read or write
Interrupt acknowledge

The basic clock period is referred to as a Time or Cycle and three or more T cycles make up a machine cycle (e.g., M1, M2 or M3). Machine cycles are extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

Interrupt Request/Acknowledge Cycle. The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 44). When an interrupt is accepted, a special /M1 cycle is generated. During this /M1 cycle, /IORQ becomes active (instead of /MREQ) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.

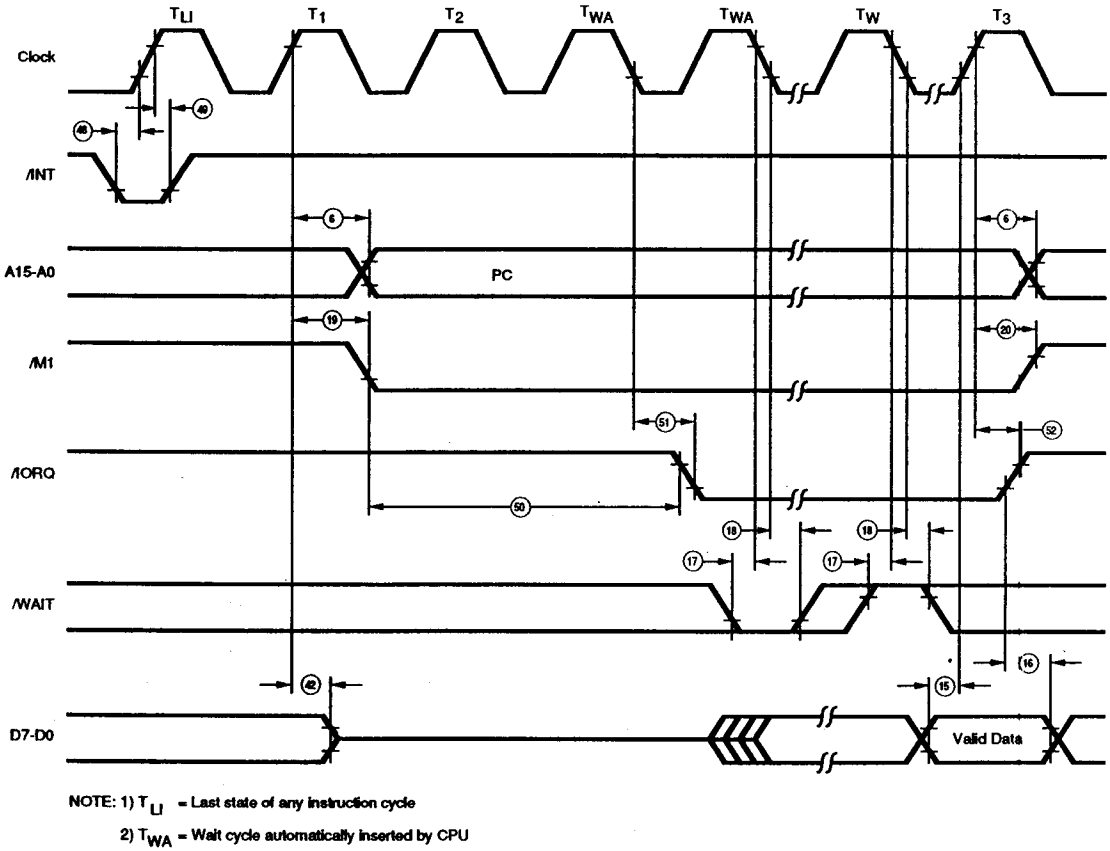
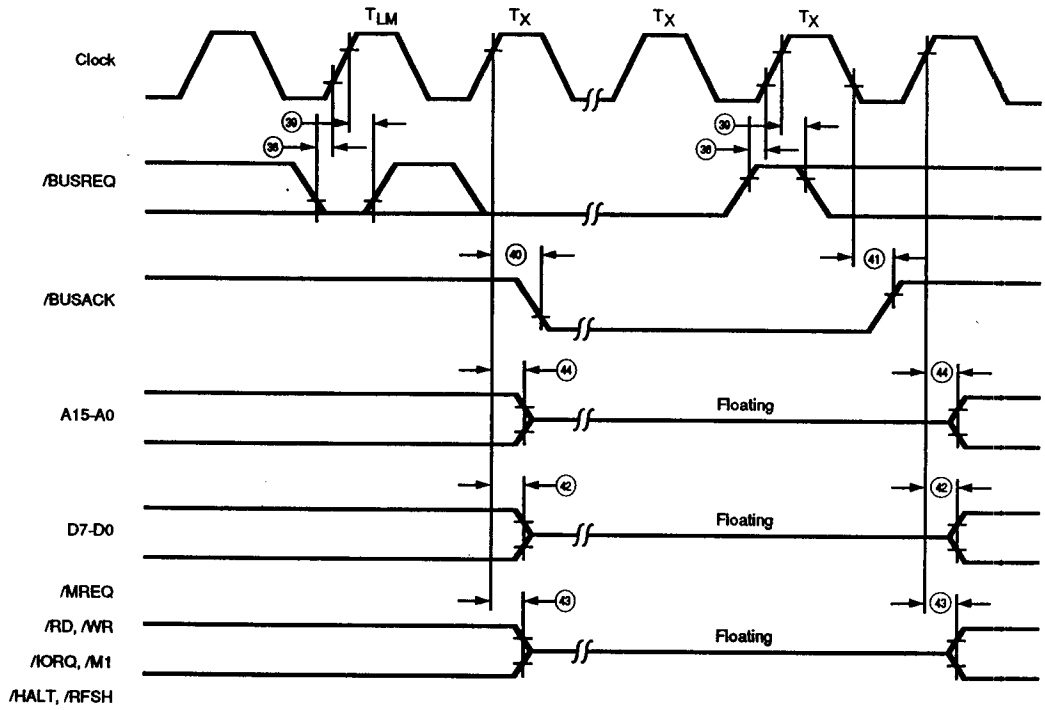


Figure 44. Interrupt Request/Acknowledge Cycle
(See Table A)

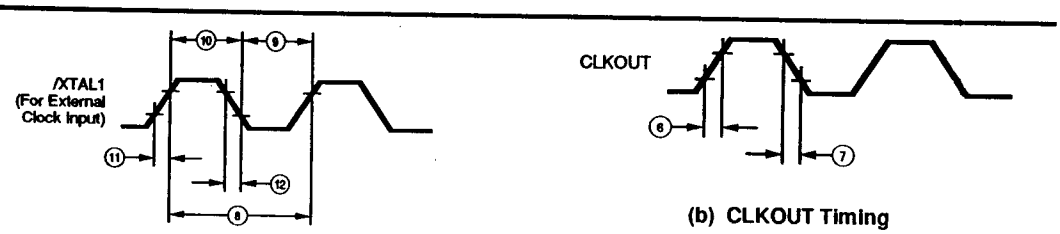
Bus Request/Acknowledge Cycle. The CPU samples /BUSREQ with the rising edge of the last clock period of any machine cycle (Figure 46). If /BUSREQ is active, the CPU sets its address, data, and /MREQ to Inputs, and /IORQ, /RD and /WR lines set to an input for on-chip peripheral access from an external bus master with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.



Notes: 1) T_{LM} = Last state of any M cycle

2) T_X = An arbitrary clock cycle used by requesting device

Figure 46. BUS Request/Acknowledge Cycle
(See Table A)

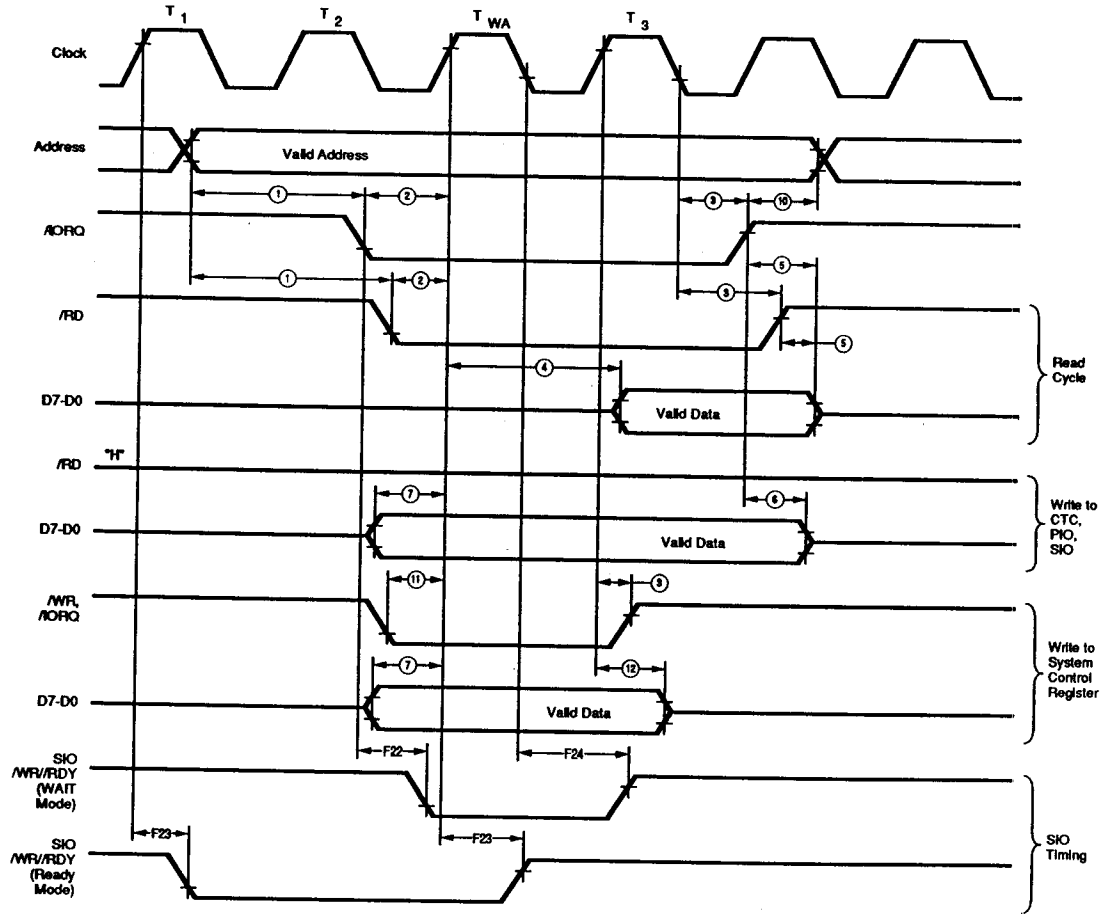


(a) XTAL1 Timing for External Clock Input

(b) CLKOUT Timing

Figure 52. Clock Timing
(See Table B)

On-chip peripheral access from External Bus master. The timing for the on-chip I/O device access from the external bus master is shown in Figure 53. This timing also applies to the timing during EV mode of operation.



(a) On-chip peripheral I/O access from External Bus master
(See Tables C and F)

Figure 53. On-chip Peripheral Timing from External Bus master

Watch-Dog Timer Timing
Figure 57 shows the timing for Watch-dog Timer.

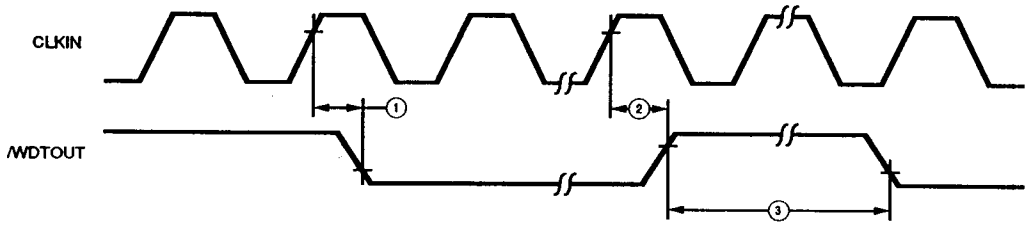


Figure 57. Watch-dog Timer Timing (See Table H)

PRECAUTIONS

(1) To release the HALT state by /RESET signal in STOP Mode, hold the /RESET signal at "0" until the output from the internal oscillator stabilizes.

Z84013/015 Only. To reset MPU, it is necessary to hold /RESET signal input at "0" level for at least three clocks.

Z84C13/C15 Only. If Reset output is disabled, /RESET must be active for at least three clock cycles for the CPU to properly accept it. Otherwise, the on-chip reset circuit extends /RESET signal to at least a minimum of 16-clock cycles.

(2) Releasing the MPU from the HALT state by the interrupt signal in IDLE1/2 Mode and STOP Mode, depends upon the HALT state and the internal system clock. They will stop unless an interrupt signal is accepted during the execution of NOP instruction, even when the internal system clock is restarted by the interrupt signal input. In particular, care must be taken when /INT is used.

Other precautions are identical to those for the Z84C00. Refer to the data sheet for the Z84C00.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage on Vcc with respect to Vss .....-0.3V to +7.0V
Voltages on all inputs
with respect to Vss .....-0.3V to Vcc+0.3V
Operating Ambient
Temperature .....See Ordering Information
Storage Temperature .....-65 °C to + 150 °C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature range is:
E = -40°C to 100°C
Voltage Supply Range:
+4.50V ≤ Vcc ≤ + 5.50V

All AC parameters assume a load capacitance of 100 pf. Add 10 ns delay for each 50 pf increase in load up to a maximum of 150 pf for the data bus and 100 pf for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pf.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

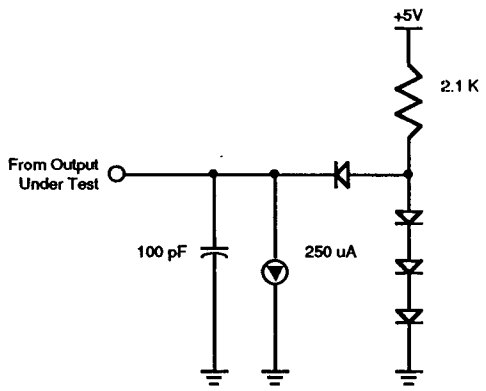


Figure 58. Standard Test Load

CAPACITANCE

Guaranteed by design and characterization

Symbol	Parameter	Min	Max	Unit
C_{CLOCK}	Clock Capacitance	35	pF	
C_{IN}	Input Capacitance	5	pF	
C_{OUT}	Output Capacitance	15	pF	

DC CHARACTERISTICS

V_{CC}=5.0V ± 10%, unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Condition
V_{OLC}	Clock Output High Voltage	V_{CC}-0.6		V	-2.0mA
V_{OHC}	Clock Output Low Voltage		0.4	V	+2.0mA
V_{IHC}	Clock Input High Voltage	V_{CC}-0.6		V	
V_{ILC}	Clock Input Low Voltage		0.4	V	
V_{IH}	Input High Voltage	2.2	V_{CC}	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{OL}	Output Low Voltage		0.4 [5]	V	I_{LO}=2.0mA
V_{OH1}	Output High Voltage	2.4		V	I_{OH}=-1.6mA
V_{OH2}	Output High Voltage	V_{CC}-0.8 [5]		V	I_{OH}=-250µA
I_{CC1}	Power Supply Current				V_{CC}=5V
	XTALIN =10MHz		50	mA	V_{IH}=V_{CC}-0.2V
	XTALIN = 6MHz		30	mA	V_{IL}=0.2V
I_{CC2}	Power Supply Current (STOP Mode)		50	µA	V_{CC}=5V
I_{CC3}	Power Supply Current (IDLE1 Mode)				V_{CC}=5V
	XTALIN =10MHz		6	mA	V_{IH}=V_{CC}-0.2V
	XTALIN = 6MHz		4	mA	V_{IL}=0.2V
I_{CC4}	Power Supply Current (IDLE2 Mode)				V_{CC}=5V
	XTALIN =10MHz		TBD [1]	mA	V_{IH}=V_{CC}-0.2V
	XTALIN = 6MHz		TBD [1]	mA	V_{IL}=0.2V
I_{LI}	Input Leakage Current	-10	10 [4]	µA	V_{IN}=0.4V to V_{CC}
$I_{L(SY)}$	SYNC pin Leakage Current	-40	10	µA	V_{OUT}=0.4V to V_{CC}
I_{LO}	3-state Output Leakage Current in Float	-10	10 [2]	µA	V_{OUT}=0.4V to V_{CC}
I_{OHD}	Darlington Drive Current				V_{OH}=1.5V
	(Port B and CTC ZC/TO)	-1.5		mA	REXT = 390 Ohms

Notes:

[1] Measurements made with outputs floating.

[2] A15-A0, D7-D0, /MREQ, /IORQ, /RD and /WR.

[3] I_{CC2} Standby Current is guaranteed when the /HALT pin is low in STOP mode.

[4] All Pins except XTALI, where I_{LI}=±25µA.

[5] A15-A0, D7-D0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1 and /BUSACK.

Table C. Timing for on-chip peripheral access from external bus master and daisy chain timing (See Figure 53(a))

No	Symbol	Parameter	Z84C1306 Z84C1506 Min	Z84C1306 Z84C1506 Max	Z84C1310 Z84C1510 Min	Z84C1310 Z84C1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
1	TsA(Rlf)	Address Setup Time to /RD, /IORQ Fall	50		40		30		ns	
2	TsRI(Cr)	/RD, /IORQ Rise to Clock Rise Setup	60		50		40		ns	
3	Th	Hold time for Specified Setup	15		15		10		ns	
4	TdCr(DO)	Clock Rise to Data out delay		100		80	60		ns	
5	TdRIr(DOz)	/RD, /IORQ Rise to Data Out Float Delay		75		60	50		ns	
6	ThRDr(D)	/M1, /RD, /IORQ Rise to Data Hold	15	40	15	30		20	ns	[C1]
7	TsD(Cr)	Data In to Clock Rise Setup Time	30		25		15		ns	
8	TdIOf(DOI)	/IORQ Fall to Data Out Delay (INTACK cycle)		95		95	70		ns	
9	ThIOr(D)	/IORQ Rise to Data Hold	15		15		10		ns	
10	ThIOr(A)	/IORQ Rise to Address Hold	15		15		10		ns	
11	TsWIf(Cr)	/IORQ, /WR setup time to Clock Rise New parameter	20		20		15		ns	[C2]
12	ThWRr(Cr)	Clock Rise to /IORQ, /WR Rise hold time	0		0		0		ns	[C2]
13	TsM1f(Cr)	/M1 Fall to Clock Rise Setup Time	40		40		15		ns	
14	TsM1r(Cf)	/M1 Rise to Clock Rise Setup Time (/M1 cycle)	-15		-15		-10		ns	
15	TdM1f(IEOf)	/M1 Fall to IEO Fall delay (Interrupt Immediately Preceding /M1 Fall)		140		80		60	ns	
20	TdCf(IEOr)	Clock Fall to IEO Rise Delay	50		40			30	ns	
21	TdCf(IEOf)	Clock Fall to IEO Rise Delay		90		75		50	ns	

Notes:
[C1] For I/O write to PIO, CTC and SIO.
[C2] For I/O Write to system control registers.
[C3] For daisy-chain timing, please refer to the note on Page 356.

Table F. SIO Timing (See Figures 53(a) and 56)

No	Symbol	Parameter	Z84C1306 Z84C1506 Min	Z84C1306 Z84C1506 Max	Z84C1310 Z84C1510 Min	Z84C1310 Z84C1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
1	TwPh	Pulse Width (High)	150		120		80		ns	
2	TwPl	Pulse Width (Low)	150		120		80		ns	
3	TcTxC	/TxC Cycle Time	250		200		120		ns	[F1]
4	TwTxCH	/TxC Width (High)	85		80		55		ns	
5	TwTxCL	/TxC Width (Low)	85		80		55		ns	
6	TrTxC	/TxC Rise Time		60		60		60	ns	
7	TfTxC	/TxC Fall Time		60		60		60	ns	
8	TdTxCf(TxD)	/TxC Fall to TxD Delay		160		120		40	ns	
9	TdTxCf(W/RRf) (Ready Mode)	/TxC Fall to /W//RDY Fall Delay	5	9	5	9	5	8	TcC	
10	TdTxCf(INTf)	/TxC Fall to /INT Fall Delay	5	9	5	9	5	9	TcC	
11	TcRxC	/RxC Cycle Time	250		200		120		ns	[F1]
12	TwRxCh	/RxC Width (High)	85		80		55		ns	
13	TwRxCl	/RxC Width (Low)	85		80		55		ns	
14	TrRxC	/RxC Rise Time		60		60		60	ns	
15	TfRxC	/RxC Fall Time		60		60		60	ns	
16	TsRxD(RxCr)	RxD to /RxC Rise Setup Time (X1 Mode)	0		0		0		ns	
17	ThRxCr(RxD)	/RxC Rise to RxD Hold Time (X1 Mode)	80		60			40	ns	
18	TdRxCr(W/RRf)	/RxC Rise to /W//RDY Fall Delay (Ready Mode)	10	13	10	13	10	13	TcC	
19	TdRxCr(INTf)	/RxC Rise to /INT Fall Delay	10	13	10	13	10	13	TcC	
20	TdRxCr(SYNCf)	/RxC Rise to /SYNC Fall Delay (Output Modes)	4	7	4	7	4	7	TcC	
21	TsSYNCf(RxCr)	/SYNC Fall to /RxC Rise Setup (External Sync Modes)	-100		-100		-100		ns	[F2]
22	TdIOf(W/RRf)	/IORQ Fall or Valid Address to /W//RDY Delay (Wait Mode)		130		110		40	ns	[F2]
23	TdCr(W/RRf)	Clock Rise to /W//RDY Delay (Ready Mode)		85		85		40	ns	[F2]
24	TdCf(W/Rz)	Clock Fall to /W//RDY Float Delay (Wait Mode)		90		80		40	ns	[F2]

Notes:
[F1] In all modes, the System Clock rate must be at least five times the maximum data rate.
[F2] Parameters 22 to 24 are on Figure 53a.