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### Understanding [Embedded - Microprocessors](#)

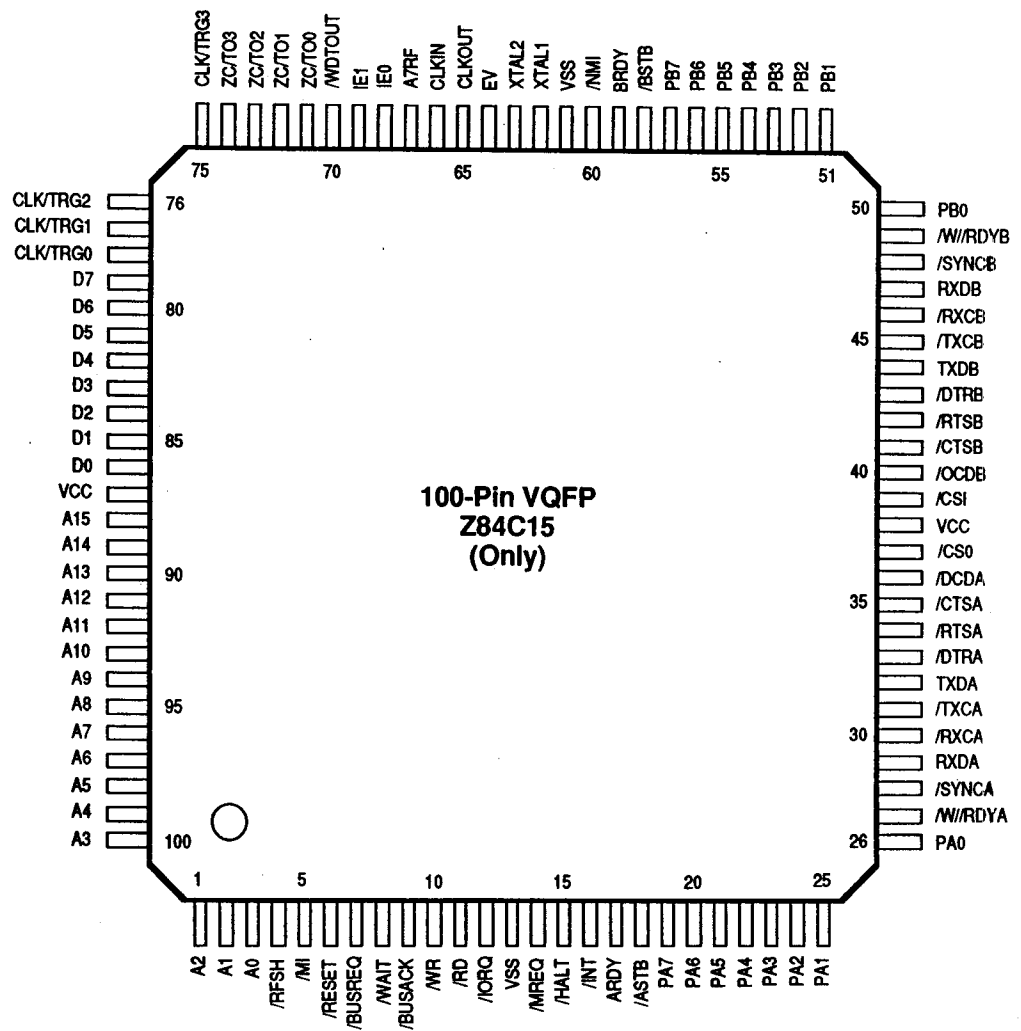
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	Z80
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8401510fec">https://www.e-xfl.com/product-detail/zilog/z8401510fec</a>



**Z84C15 Pin-out Assignments**

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## CPU SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
A0-A15	16-1(x13), 6-1, 100-91(x15)	I/O	16-bit address bus. Specifies I/O and memory addresses to be accessed. During the refresh period, addresses for refreshing are output. The bus is an input when the external master is accessing the on-chip peripherals.
D0-D7	83-76(x13), 89-82(x15)	I/O	8-bit bidirectional data bus. When the on-chip CPU is accessing on-chip peripherals, these lines are set to output and hold the data to/from on-chip peripherals.
/RD	30(x13), 14(x15)	I/O	Read signal. CPU read signal for accepting data from memory or I/O devices. When an external master is accessing the on-chip peripherals, it is an input signal.
/WR	20(x13), 13(x15)	I/O	Write Signal. This signal is output when data, to be stored in a specified memory or peripheral LSI, is on the MPU data bus. When an external master is accessing the on-chip peripherals, it is an input signal.
/MREQ	23(x13), 17(x15)	I/O, 3-State	Memory request signal. When an effective address for memory access is on the address bus, "0" is output. When an external master is accessing the on-chip peripherals, it is a tri-state signal.
/IORQ	21(x13), 15(x15)	I/O	I/O request signal. When addresses for I/O are on the lower 8 bits (A7-A0) of the address bus in the I/O operation, "0" is output. In addition, the /IORQ signal is output with the /M1 signal at the time of interrupt acknowledge cycle to inform peripheral LSI of the state of the interrupt response vector is when put on the data bus. When an external master is accessing the on-chip peripherals, it is an input signal.
/M1	17(x13), 8(x15)	I/O	Machine cycle "1". /MREQ and "0" are output together in the operation code fetch cycle. /M1 is output for every opcode fetch when a two byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with /IORQ. It is 3-stated in EV mode.

## SYSTEM CONTROL SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, 3-State	Function
/CS1 (C13/C15 only)	40(x13), 42(x15)	Out	Chip Select 1. Used to access external memory or I/O devices. This pin has been assigned to "ICT" pin on Z84013/015. This signal is decoded only from A15-A12 without control signals. Refer to "Functional Description" on-chip select signals for further explanation.
/WDTOUT	61(x13), 73(x15)	Out(013/015), Open Drain(C13/C15)	Watch Dog Timer Output signal. Output pulse width depends on the externally connected pin.
/RESET	28(x13), 9(x15)	Input(013/015), I/O (Open Drain) (C13/C15)	Reset signal. /RESET signal is used for initializing MPU and other devices in the system. Also used to return from the steady state in the STOP or IDLE modes.

**Note:** For the Z84013/Z84015 the /RESET must be kept in active state for a period of at least three system clock cycles.

**Note:** For the Z84C13/Z84C15, during the power-up sequence, the /RESET becomes an Open drain output and the Z84C13/C15 will drive this pin to "0" for 25 to 75 msec after the power supply passes through approx. 2.2V and then reverts to input. If it receives the /RESET signal after power-on sequence, it will drive /RESET pin for 16-processor clock cycles depending on the status of Reset Output Disable bit in Misc Control Register. If this Reset output is disabled, it must be kept in active state for a period of at least three system clock cycles. Note, that if using Z84C13/C15 in a Z84013/015 socket, modification may be required on the reset circuit since this pin is "pure input pin" on the Z84013/015. Also, the /RESET pin doesn't have internal pull-up resistors and therefore requires external pull-ups. For more details on the device, please refer to "Functional Description."

XTAL1	63(x13), 65(x15)	In	Crystal oscillator connecting terminal. A parallel resonant crystal is recommended. If external clock source is used as an input to the CGC unit, supply clock goes into this terminal. If external clock is supply to CLKIN pin (without CGC unit), this terminal must be connected to "0" or "1".
XTAL2	63(x13), 66(x15)	Out	Crystal oscillator connecting terminal.
CLKIN	67(x13), 69(x15)	In	Single-phase System Clock Input.
CLKOUT	66(x13), 68(x15)	Out	Single-phase clock output from on-chip Clock Generator/Controller.
EV	58(x13), 67(x15)	In	Evaluator signal. When "1" is applied to this pin, IPC is put in Evaluation mode.

**Note:** For the Z84013/015, together with /BUSREQ, the EV signal puts the IPC into the evaluation mode. When this signal becomes active, the status of /M1, /HALT and /RFSH change to input. When using Z84013/015 as an evaluator chip, the CPU is electrically disconnected after one machine cycle is executed with the EV signal "1" and the /BUSREQ signal "0". It follows the instructions from the other CPU (of ICE). Upon receiving /BUSREQ; A15-A0, /MREQ, /IORQ, /RD and /WR are changed to input and D7-D0 changes its direction. /BUSACK is NOT 3-stated so it should be disconnected by an externally connected circuit. For details, please refer to "Functional Description" on EV mode.

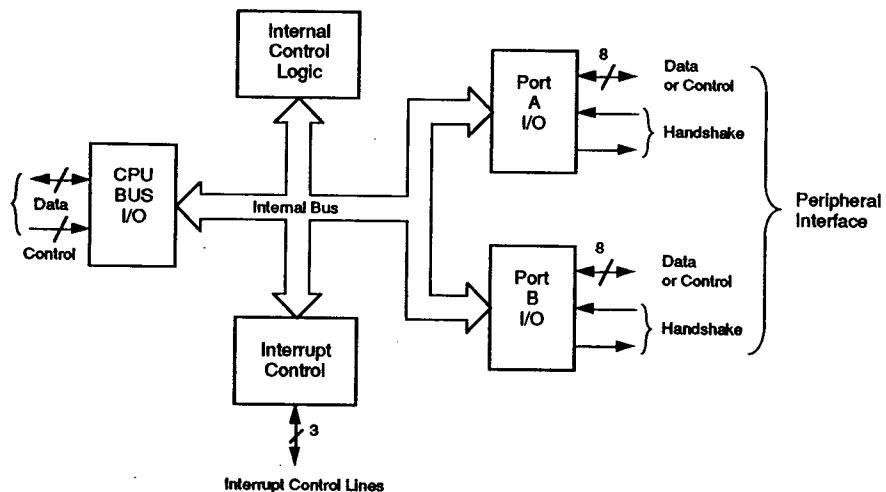


Figure 6. PIO Block Diagram

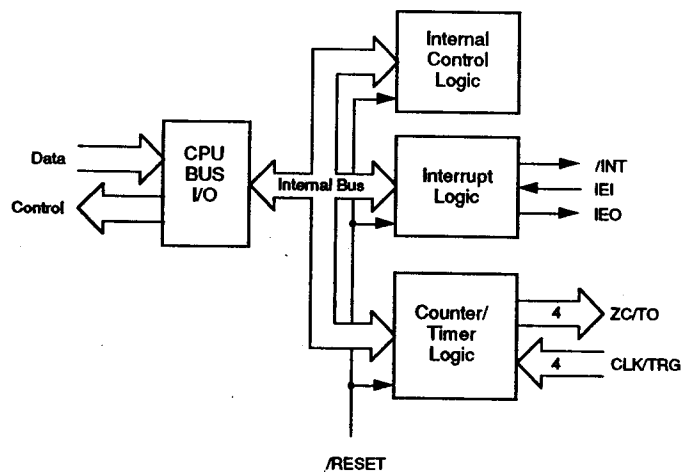


Figure 7. CTC Block Diagram

#### Z84C4x Serial I/O Logic Unit

This logic unit provides the user with two separate multi-protocol serial I/O channels that are completely compatible with the Z84C4x SIO. Their basic functions as serial-to-parallel and parallel-to-serial converters can be programmed by a CPU for a broad range of serial communications applications. Each channel, designated Channel A and Channel B, is capable of supporting all common

asynchronous and synchronous protocols (Monosync, Bisync, and SDLC/HDLC, byte or bit oriented - Figure 8).

**Z84C13/C15 Only.** As an enhancement to the Z84013/015, the Z84C13/C15 can handle a 32-bit CRC on Channel A and Schmitt-trigger inputs on the /TxC and /RxC pins of both channels.

power-up, and boundary address is undefined. These features are controlled via the I/O control registers located at I/O address EEh and EFh. **Note that a glitch may be observed on these pins because address decode logic is decoding only A15-A12, without any control signals.** For more detail, please refer to the "Programming" section."

#### Other functional features (Z84C13/C15 Only)

For more system design flexibility, the Z84C13/C15 has the following unique features. These features are controlled by MCR (Misc. Control Register) which is indirectly accessed via the System Control Register Pointer (SCRIP, I/O address EEh), and System Control Data Port (SCDP, I/O address EFh). For more details, please refer to the "Programming" section.

- Clock Divide-by-one option
- Reset Output Disable
- 32-bit CRC Generation/Checking

**Clock Divide-by-One Option.** This feature is programmed through Bit D4 of MCR. Upon Power-On reset, the Clock from on-chip CGC is passed through a divide-by-two circuit. By setting this bit to one, the divide-by-two circuit is bypassed so the clock on the CLKOUT pin is equal to X'tal input. If the clock is applied to the CLKIN pin from external clock source, the status of this bit is ignored. Upon Power-on Reset, it is cleared to 0. For details, please refer to "Programming" section.

**Reset Output Disable.** This feature is programmed by Bit D3 of MCR. If this bit is cleared to "0", the /RESET pin becomes "Open-drain output" and is driven to "0" for 16-clock cycles from the falling edge of /RESET input. This feature is for the cases where /RESET is used to get out from the "HALT" state. If this bit is set to one, the on-chip reset circuit will not drive /RESET pin.

**32-bit CRC Generation/Checking.** This feature is programmed by Bit D2 of MCR. By setting this bit to one, Channel A of SIO is set to use the 32-bit CRC generator/checker instead of the original 16-bit CRC generator/checker in synchronous communication modes. The polynomial to be used in this mode is the one for the protocols

such as V.42, and is  $(X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1)$ . Upon Power-on Reset, this bit is cleared to 0.

#### Evaluation Mode

The IPC has a built evaluation (or development) mode feature which allows the users to utilize standard Z80 development systems conveniently. This mode virtually replaces the on-chip Z80 CPU with the external CPU. In this mode, the on-chip CPU is electrically disconnected from internal bus and all 3-state signals (A15-0, D7-0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1 and /RFSH; for C13/C15, /BUSREQ as well) are tri-stated, or changed to input. This allows the development system CPU to take over and use the internal I/O registers of the IPC exactly as if the CPU was on-chip.

**Z84013/015 Only.** When this signal is active, the /M1, /HALT and /RFSH pins are put in the high-impedance state. In using the Z84013/015 as an evaluator chip, the CPU is electrically disconnected (put in high-impedance state) after one machine cycle is executed with the EV signal being "1" and the /BUSREQ signal being "0". Then, on-chip resources can be accessed from the outside. /BUSACK is disconnected by an externally connected circuit.

**Z84C13/C15 Only.** If the EV pin is tied to Vcc on Power-up, the Z84C13/C15 enters into an evaluation mode. In this mode, the internal CPU is immediately disconnected from the internal bus and all 3-state signals mentioned above are tri-stated, or changed to input. Note that the /WAIT pin became the OUTPUT pin in EV mode, and the Wait State Generator generates wait states only as programmed. If the target application board has a separate wait state generator, modification of the target may be required. /BUSACK is 3-stated in this mode.

The Z84C13/C15 behaves similarly to the situation where in regular operation, the /BUSREQ signal is asserted by an external master causing all 3-state signals to be tri-stated by the Z84C13/C15 during T1 of the following machine cycle. The /BUSREQ approach was not used for the evaluation mode to avoid significant external circuitry to work around the time period before the external CPU uses the bus for Z84C13/C15 accesses.

## PROGRAMMING

#### I/O address assignment

The IPC's on-chip peripherals' I/O addresses are listed in Table 1. They are fully decoded from A7-A0 and have no image. The registers with Z84C13/C15 located at I/O Ad-

dress EEh and EFh are the registers to control enhanced features to Z84013/015, and not assigned on Z84C013/015.

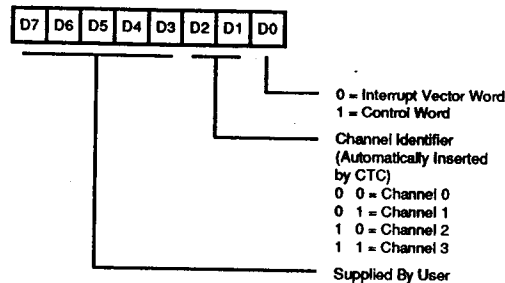
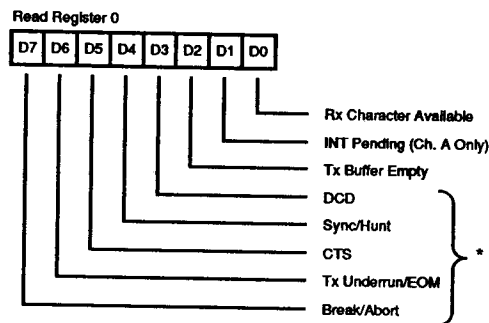


Figure 19. CTC Interrupt Vector Word

## SIO REGISTERS

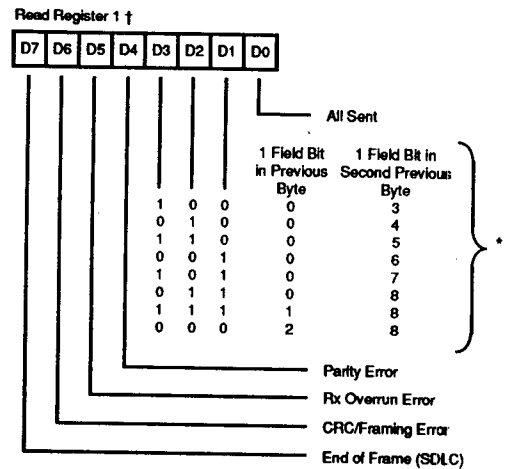
For more detailed information, refer to the SIO Technical Manual.

**Read Registers.** The SIO channel B contains three read registers while channel A contains only two that are read to obtain status information. To read the contents of a register (rather than RR0), the program must first write a pointer to WR0 in exactly the same manner as a write operation. The next I/O read cycle will place the contents of the selected read registers onto the data bus (Figure 20a, b, c).



\* Used With "External/Status Interrupt" Modes

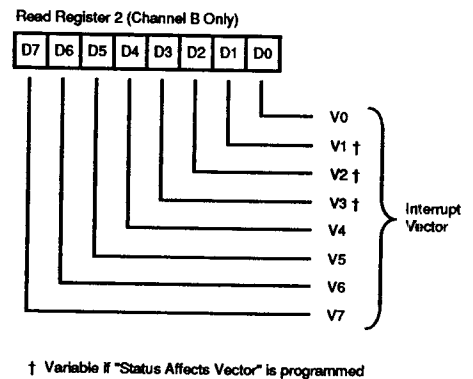
Figure 20a. SIO Read Register 0



\* Residue data for eight Rx bits/character programmed

† Used with special receive condition mode

Figure 20b. SIO Read Register 1



† Variable if "Status Affects Vector" is programmed

Figure 20c. SIO Read Register 2

**Write Registers.** The SIO Channel B contains eight write registers while Channel A contains only seven that are programmed to configure the operating mode characteristics of each channel. With the exception of WR0, programming the write registers is a two step operation. The first operation is a pointer written to WR0 which points to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel (Figure 21).

## INTERRUPT PRIORITY REGISTER (INTPR; I/O address F4h)

This register (write only) is provided to determine the interrupt priority for the CTC, SIO and the PIO (Figure 24).

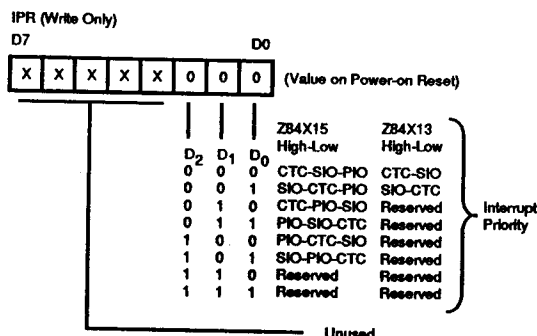


Figure 24. Interrupt Priority Register

Bit D7-D3. Unused

Bit D2-D0. This field specifies the order of the interrupt daisy chain. Upon Power-on Reset, this field is set to "000".

	Z84C15 High - Low	Z84C13 High - Low
000	CTC-SIO-PIO	CTC-SIO
001	SIO-CTC-PIO	SIO-CTC
010	CTC-PIO-SIO	Reserved
011	PIO-SIO-CTC	Reserved
100	PIO-CTC-SIO	Reserved
101	SIO-PIO-CTC	Reserved
110	Reserved	Reserved
111	Reserved	Reserved

## REGISTERS FOR SYSTEM CONFIGURATION

(The following registers are not available on Z84013/015.) There are four indirectly accessible registers to determine System configuration with the Z84C13/C15. These indirectly accessible registers are: Wait State Control Register (WCR, Control Register 00h), Memory Wait Boundary Register (MWBR, Control Register 01h), Chip Select Boundary Register (CSBR, Control Register 02h) and Misc. Control Register (MCR, Control Register 03h). To access these registers, Z84C13/C15 writes "register number to be accessed" to the System Control Register Pointer (SCRIP,

I/O address EEh), and then accesses the target register through the System Control Data Port (SCDP, I/O address EFh). The pointer which writes into SCRIP is kept until modified.

**System Control Register Pointer (SCRIP, I/O address EEh)**  
This register stores the pointer to access System Control Registers (WCR, MWBR, CSBR and MCR). This register is Read/Write and it holds the pointer value until modified. Upon Power-on Reset, all bits are cleared to zero. The pointer value, other than 00h to 03h is reserved and is not written. Upon Power-on Reset, this register is set to "00h" (Figure 25).

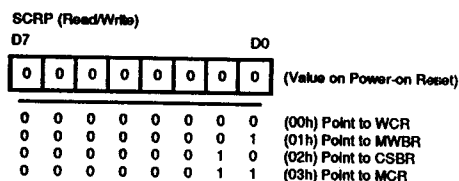


Figure 25. System Control Register Pointer

**System Control Data Port (SCDP, I/O address EFh)**  
This register is to access WCR, MWBR, CSBR and MCR (Figure 26).

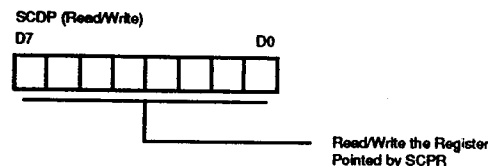


Figure 26. System Control Data Port

**Wait State Control Register (WCR, Control Register 00h)**  
This register can be accessed through SCDP with the pointer value 00h in SCRIP (Figure 27). To maintain compatibility with the Z84013/015, the Z84C13/C15 inserts the maximum number of wait states (set all bits of this register to one) for fifteen /M1 cycles after Power-on Reset. It automatically clears the contents of this register (move to no-wait state insertion) on the trailing edge of the 16th /M1 signal unless software has programmed a value. If automatic wait state insertion is needed, the wait state is programmed within this time period. A read to WCR during this period will return FFh, unless programmed.



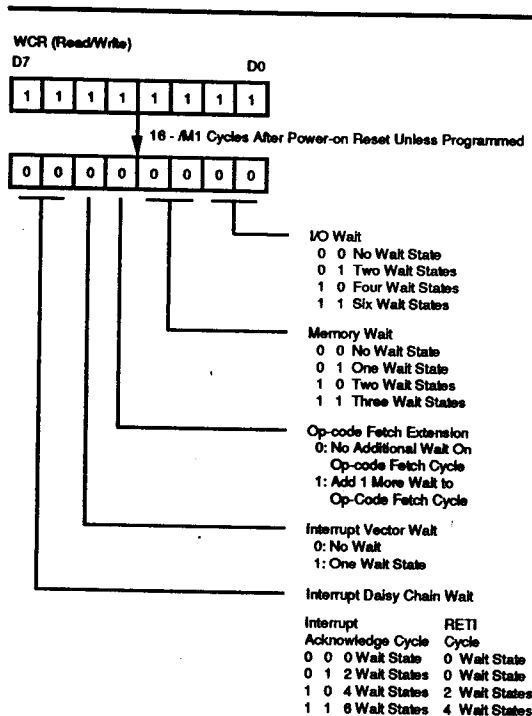


Figure 27. Wait State Control Register

This register has the following fields:

**Bit 7-6. Interrupt Daisy Chain Wait.** This 2-bit field specifies the number of wait states to be inserted during an Interrupt Daisy Chain settle period of the Interrupt Acknowledge cycle, which is /IORQ falls after the settling period from /M1 going active "0". Also, this field controls the number of wait states inserted during the RETI (Return From Interrupt) cycle. If specified to insert 4 or 6 wait states during Interrupt Acknowledge cycle, the Wait state generator also inserts wait states during RETI fetch sequence. This sequence is formed with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts 1 wait state if op-code followed by EDh is NOT 4Dh, and inserts 2 or 4 wait states, respectively, if the following op-code is 4Dh.

Interrupt Acknowledge	RETI cycle
00 - No Wait states	No Wait states
01 - 2 Wait states	No Wait states
10 - 4 Wait states	2 Wait states
11 - 6 Wait states	4 Wait states

For fifteen /M1 cycles from Power-on Reset, bits 7-6 are set to "11". They clear to "00" on the trailing edge of the 16th /M1 signal unless programmed.

**Bit 5. Interrupt Vector Wait.** While this bit is set to one, the wait state generator inserts one wait state after the /IORQ signal goes active during the Interrupt acknowledge cycle. This gives more time for the vector read cycle. While this bit is cleared to zero, no wait state is inserted (standard timing). For fifteen /M1 cycles from Power-on Reset, this bit is set to "1", then cleared to "0" on the trailing edge of the 16th /M1 signal, unless programmed.

**Bit 4. Opcode Fetch Extension.** If this bit is set to "1", one additional wait state is inserted during the Op-code fetch cycle in addition to the number of wait states programmed in the Memory Wait field. For fifteen /M1 cycles from Power-on Reset, this bit is set to "1", then cleared to "0" on the trailing edge of the 16th /M1 signal, unless programmed.

**Bit 3-2. Memory Wait States.** This 2-bit field specifies the number of wait states to be inserted during memory Read/Write transactions.

- 00 - No Wait states
- 01 - 1 Wait states
- 10 - 2 Wait states
- 11 - 3 Wait states

For fifteen /M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the 16th /M1 signal, unless programmed.

**Bit 1-0. I/O Wait states.** This 2-bit field specifies the number of wait states to be inserted during I/O transactions.

- 00 - No Wait states
- 01 - 2 Wait states
- 10 - 4 Wait states
- 11 - 6 Wait states

For fifteen /M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the 16th /M1 signal, unless programmed. For the accesses to the on-chip I/O registers, no Wait states are inserted regardless of the programming of this field.

#### Memory Wait Boundary Register (MWBR, Control Register 01h)

This register specifies the address range to insert memory wait states. When accessed memory addresses are within this range, the Memory Wait State generator inserts Memory Wait States specified in the Memory Wait field of WCR (Figure 28).

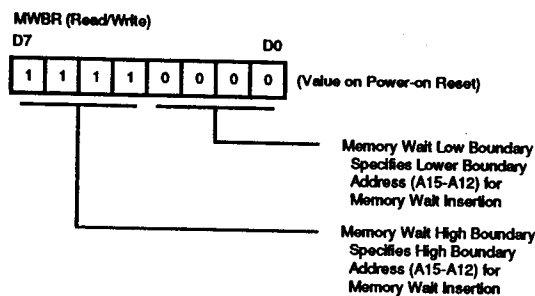


Figure 28. Memory Wait Boundary Register

**Bit D7-D4. Memory Wait High Boundary.** This field specifies A15-A12 of the upper address boundary for Memory Wait.

**Bit D3-D0. Memory Wait Low Boundary.** This field specifies A15-12 of the lower address boundary for Memory Wait.

Memory Wait states are inserted for the address range:

$(D7-D4 \text{ of MWBR}) \geq A15-A12 \geq (D3-D0 \text{ of MWBR})$

This register is set to "F0h" on Power-on Reset, which specifies the address range for Memory Wait as "0000h to FFFFh".

#### Chip Select Boundary Register (CSBR, Control Register 02h)

This register specifies the address range for each chip select signal. When accessed memory addresses are within this range, chip select signals are active (Figure 29).

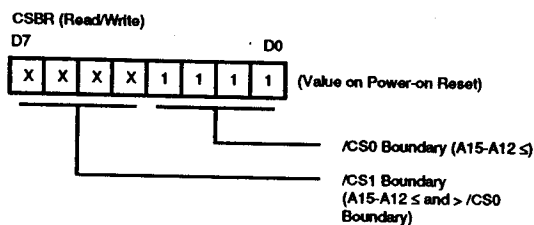


Figure 29. Chip Select Boundary Register

**D7-D4. /CS1 Boundary Address.** These bits specify the boundary address range for /CS1. The bit values are ignored on power-up as the /CS1 enable bit is off. The /CS1 is asserted if the address lines A15-12 have an address value greater than the programmed value for /CS0, and less than or equal to the programmed value in these bits.

**D3-D0. /CS0 Boundary Address.** These bits specify the boundary address range for /CS0. /CS0 is asserted if the address lines A15-12 have an address value less than or equal to the programmed boundary value. The /CS0 enable bit in the MCR must be set to 1. Upon Power-up reset, these bits come up as all 1's so that /CS0 is asserted for all addresses.

Chip Select signals are active for the address range:

/CS0:  $(D3-D0 \text{ of CSBR}) \geq A15-A12 \geq 0$

/CS1:  $(D7-D4 \text{ of CSBR}) \geq A15-A12 > (D3-D0 \text{ of CSBR})$

This register is set to "xxxx1111b" on Power-on Reset, which specifies the address range of /CS0 for "0000h to FFFFh" (all Memory location) and /CS1 "undefined."

#### Misc Control Register (MCR, Control Register 03h)

This register specifies miscellaneous options on this device (Figure 30).

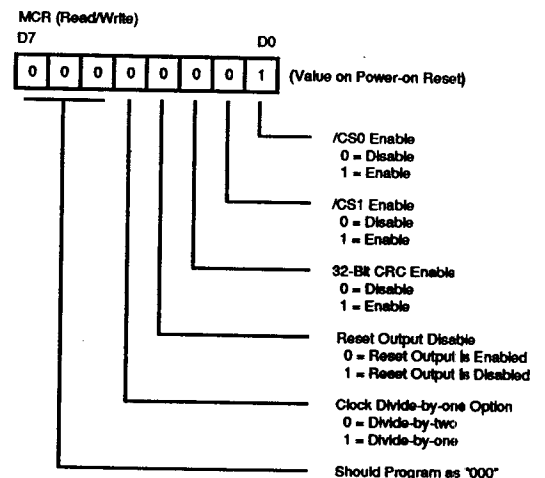


Figure 30. Misc Control Register

**Bit D7-D5. Reserved.** These three bits are reserved and are always programmed as "000".

**Bit D4. Clock Divide-by-one option.** "0"-Disable, "1"-enable. On-chip CGC unit has divide-by-two circuit. By setting this bit to one, this circuit is bypassed and CLKOUT is equal to X'tal oscillator frequency (or external clock input on the XTAL1 pin). This bit has no effect when the on-chip CGC unit is not in use and the external system clock is fed from CLKIN pin. Upon Power-on Reset, this bit is cleared to 0 and the clock is divided by two.

**Bit D3. Reset Output Disable.** "0"-Reset output is enabled, "1"-Reset output is disabled. This bit controls the /RESET signal and is driven out when reset input is used to take the Z84C13/C15 out of the "Halt" state. The reset pulse is driven out for 16-clock cycles from the falling edge of /RESET input, unless this bit is set. Upon Power-on reset, this bit is cleared to 0.

**Bit D2. 32-Bit CRC enable.** "0"-Normal mode (16-bit CRC) "1"-32-bit CRC generation/Checking is enabled on SIO Channel A. This bit determines if the 32-bit CRC feature is enabled on Channel A of the SIO. If this bit is 0, the SIO is in a normal mode of operation. If this bit is set to 1, a normal CRC generator/checker is replaced with a 32-bit CRC generator/checker. Upon Power-on Reset, this bit is clear to "0".

**Bit D1. /CS1 Enable.** "0"-Disable, "1"-Enable. This bit enables /CS1 output. While this bit is "0", /CS1 is forced to "1". While this bit is "1", /CS1 carries the address range specified in the CSBR. Upon Power-on Reset, this bit is cleared to "0".

**Bit D0. /CS0 Enable.** "0"-Disable, "1"-Enable. This bit enables /CS0 output. While this bit is "0", /CS1 pin is forced

to "1". While this bit is "1", the /CS0 carries address range specified in the CSBR. Upon Power-on Reset, this bit is set to "1".

#### Operation modes

There are four kinds of operation modes available for the IPC in connection with clock generation; RUN Mode, IDLE1/2 Modes and STOP Mode.

The Operation mode is effective when the HALT instruction is executed. Restart of the MPU from the stopped state under IDLE1/2 Mode or STOP mode is affected by inputting either /RESET or interrupt (/NMI or /INT). The mode selection of these power-down modes is made by programming the HALTM field (Bit D4-3) of WDTMR.

#### Setting Halt Mode

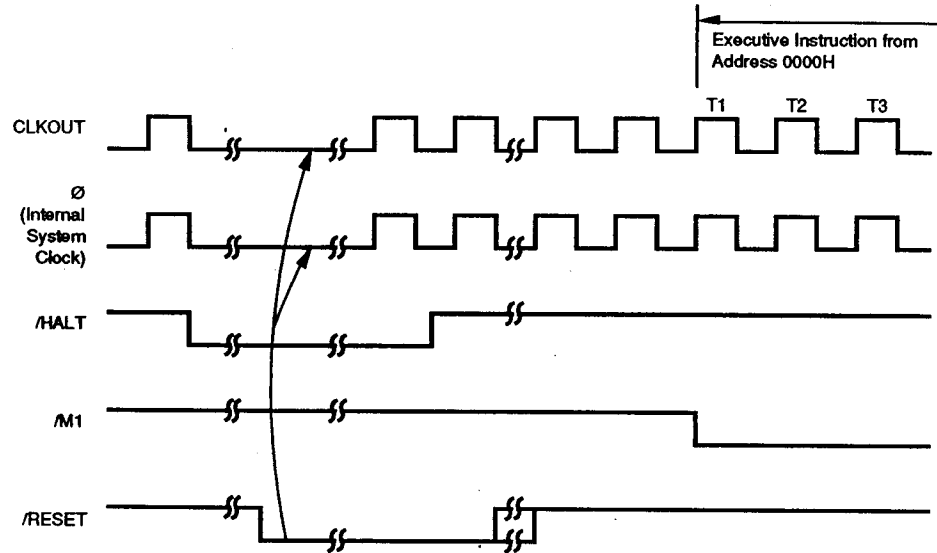
Duplicate control is provided to prevent the stopping of the WDT operation caused by the halt mode setting an error due to program runaway. As described in the programming section, changing the Halt Mode field of WDTMR is in two steps. First, write "DBh" to WDTCR followed by a write to the WDTMR with the value in HALTM. Table 2 has descriptions of each mode, and Table 3 has device status in the Halt state.

**Table 2. Power-down Modes**  
(When using on-chip CGC unit; CLKOUT and CLKIN are tied together)

Operation Mode	WDTMR Bit D4	Bit D3	Description at HALT State
RUN Mode	1	1	The IPC continues the operation and continuously supplies a clock to the outside.
IDLE1 Mode	0	0	The internal oscillator's operation is continued. Clock output (CLKOUT) as well as internal clock to the CPU, PIO, SIO, CTC and the Watch Dog Timer is stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
IDLE2 Mode	0	1	The internal oscillator and the CTC's operation continues and supplies clock to the outside on the CLKOUT pin continuously. But the internal clock to the CPU, PIO, SIO and the Watch Dog Timer is stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
STOP Mode	1	0	All operations of the internal oscillator, clock (CLK) output, internal clock to the CPU, PIO, CTC, SIO and the Watch Dog Timer are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.

**Z84C13/C15 Only.** The /RESET pulse is stretched to a minimum of 16 cycles and driven out of the Z84C13/C15 on the /RESET pin if Reset output is enabled (bit D3 of MCR is cleared to "0"). Setting bit D3 disables the driving out of

/RESET. The values in the control registers (WDTMR, SCRIP, WCR, MWBR, CSBR and MCR) are initialized to the default value on /RESET.



**Figure 40. Halt Release Operation Timing By Reset in STOP Mode**

**Start-up Time at Time of Restart (STOP Mode).** When the MPU is released from the halt state by accepting an interrupt request, it executes an interrupt service routine. Therefore, when an interrupt request is accepted, it starts generating clock on the CLKOUT pin, after a start-up time, by the internal counter  $[(2^{14} + 2.5) \text{ TcC (TcC: Clock Cycle)}]$ . This obtains a stabilized oscillation for operation.

Further, in case of restart by the /RESET signal, the internal counter does not operate.

**Evaluation operation.** Each of the CPU signals (A15-0, D7-0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1, /RFSH) can be 3-stated by activating the EV pin. The Z84C13/C15 enhances the counter part by eliminating the requirement of /BUSREQ to go active.

**Instruction set.** The instruction set of the IPC is the same for the Z84C00. For details, refer to the data sheet of the Z84C00 Technical Manual.

## AC TIMING

The following section describes the timing of the IPC. The numbers appearing in the figures refer to the parameters on Table A - F.

### CPU Timing

Parameters referenced in Figure 41 through Figure 48 appear in Table A.

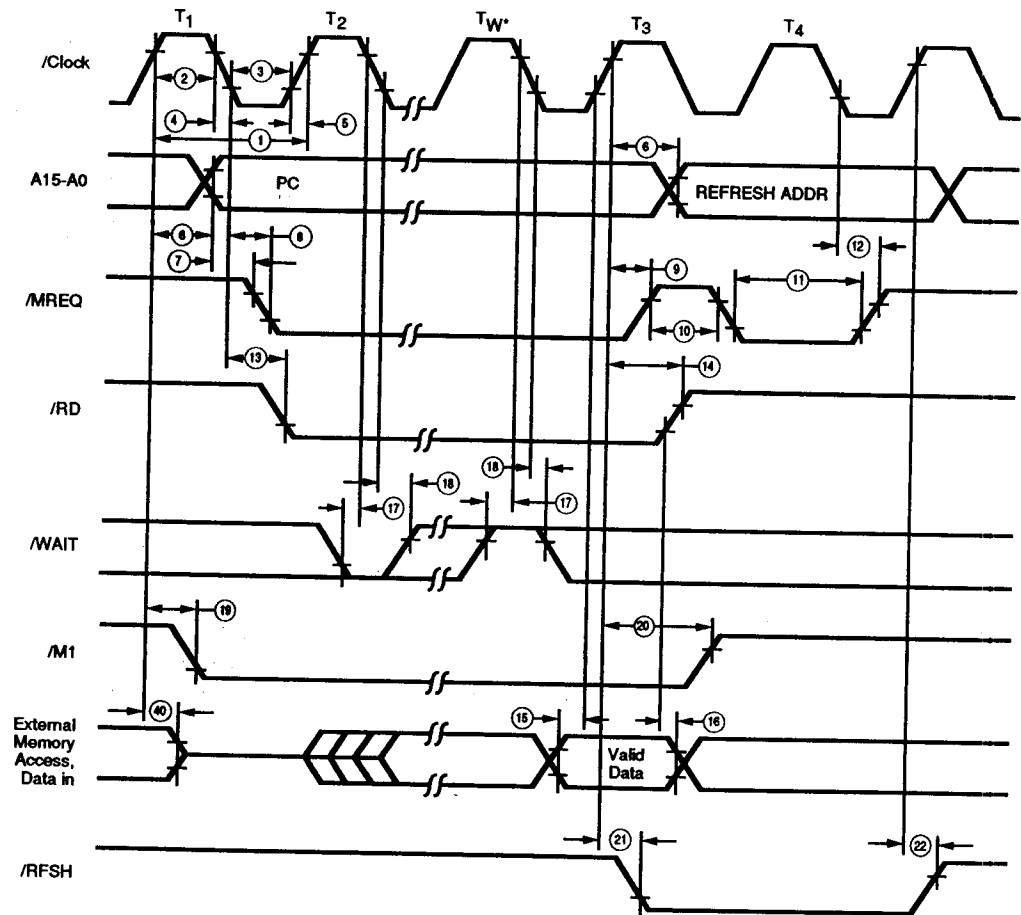
The IPC's CPU executes instructions by proceeding through the following specific sequence of operations:

Memory read or write  
I/O device read or write  
Interrupt acknowledge

The basic clock period is referred to as a Time or Cycle and three or more T cycles make up a machine cycle (e.g., M1, M2 or M3). Machine cycles are extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

**Instruction Op-code Fetch.** The CPU places the contents of the Program Counter (PC) on the address bus at the start of the cycle (Figure 41). Approximately one-half clock cycle later, /MREQ goes active. When active, /RD indicates that the memory data can be enabled onto the CPU data bus.

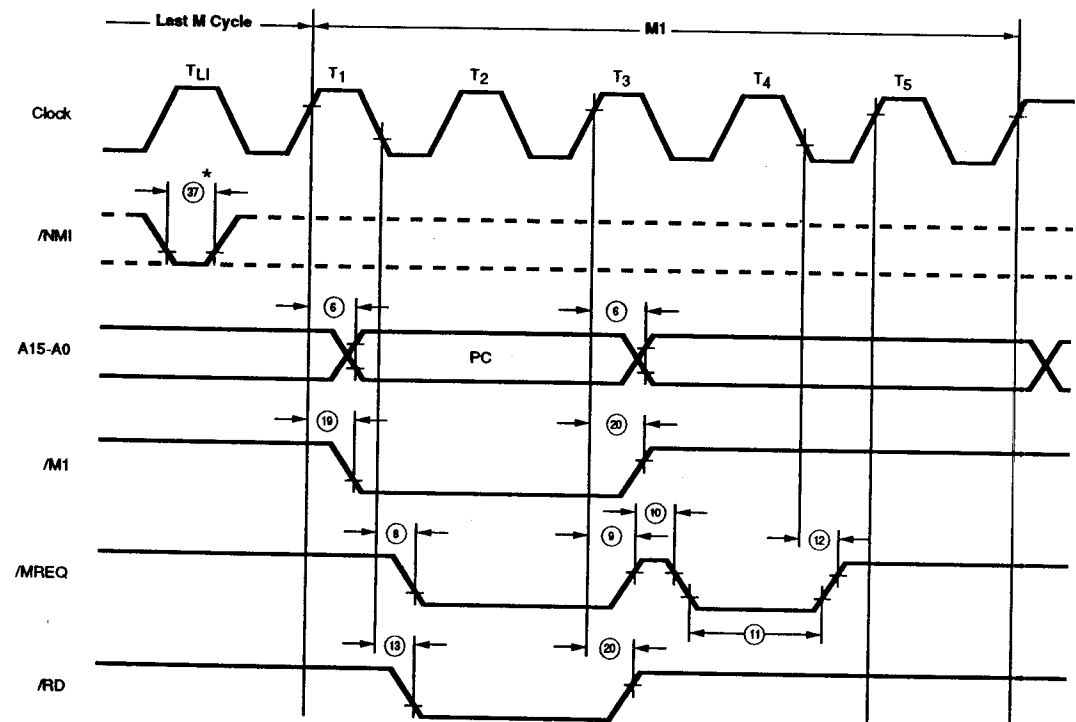
The CPU samples the /WAIT input with the falling edge of clock state T2. During clock states T3 and T4 of an M1 cycle, dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction.



**Figure 41. Instruction Op-code Fetch**  
(See Table A)

**Non-Maskable Interrupt Request Cycle.** /NMI is sampled at the same time as the maskable interrupt input /INT, but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal

memory read operation except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the /NMI service routine located at the address 0066H (Figure 45).

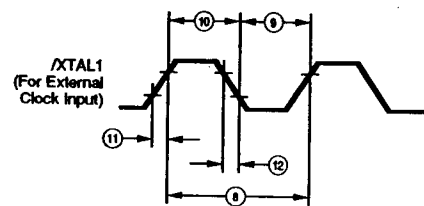


\* Although /NMI is an asynchronous input, to guarantee its being recognized on the following machine cycle, /NMI's falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T<sub>L1</sub>).

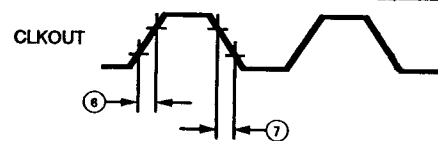
**Figure 45. Non-Maskable Interrupt Request Operation**  
(See Table A)



**Figure 51. Clock Restart Timing (IDLE1/2 Mode)**  
(See Table B)



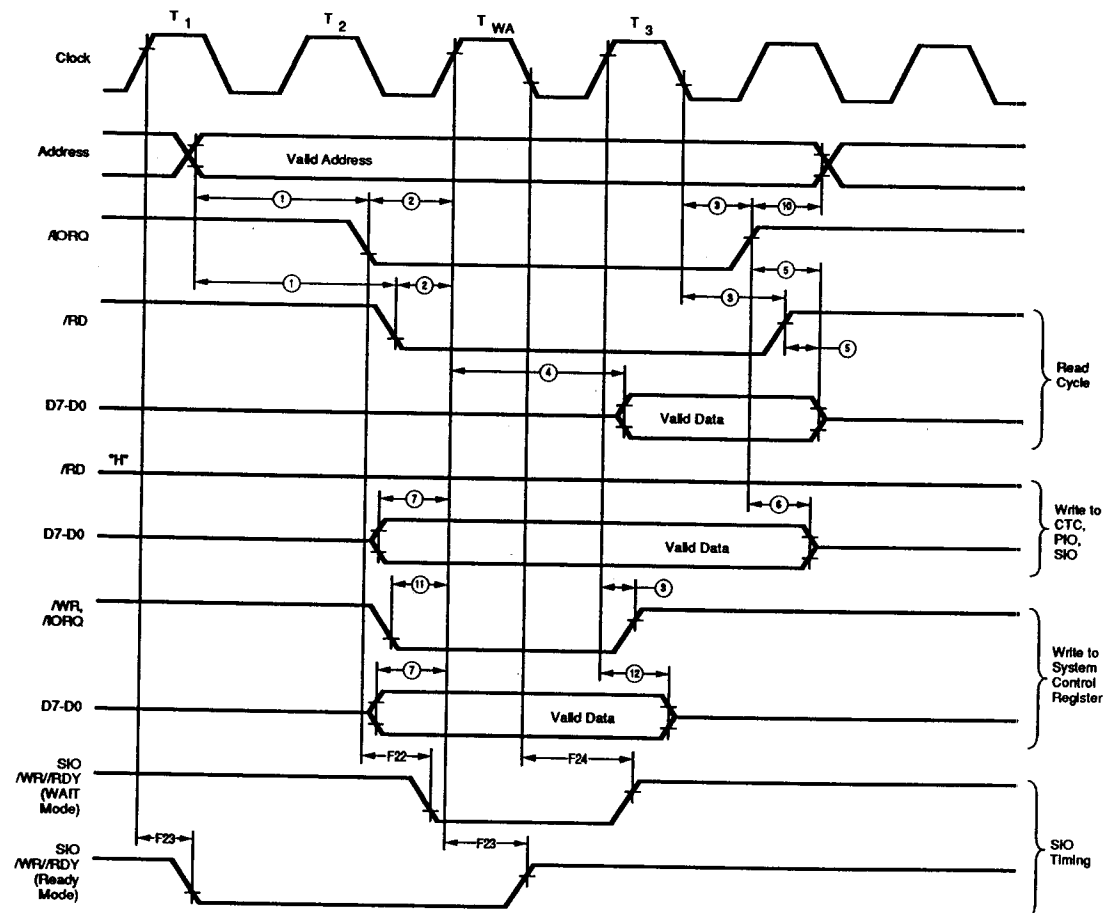
(a) XTAL1 Timing for External Clock Input



(b) CLKOUT Timing

Figure 52. Clock Timing  
(See Table B)

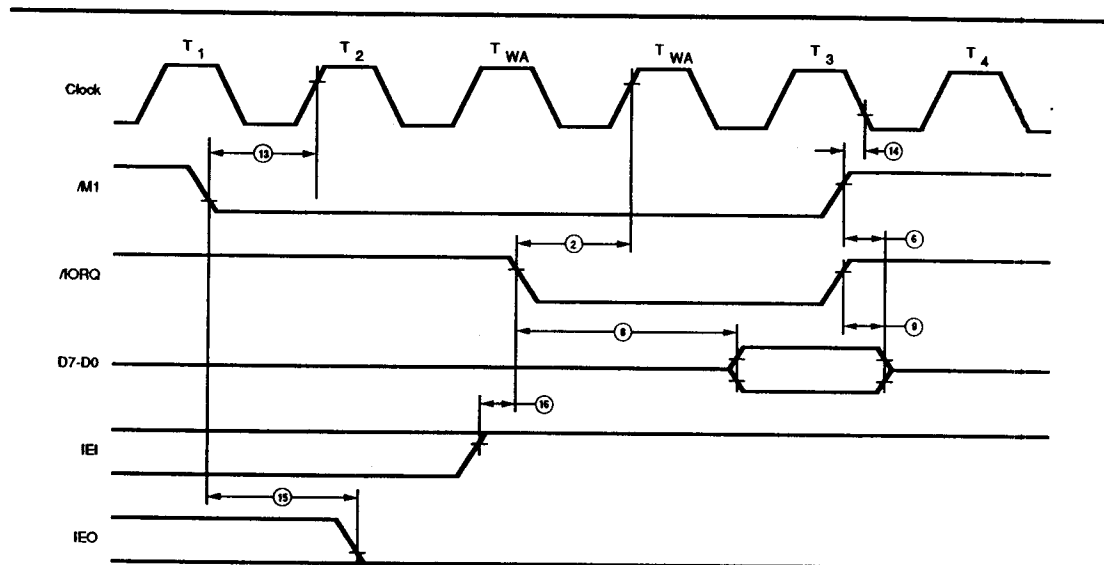
On-chip peripheral access from External Bus master. The timing for the on-chip I/O device access from the external bus master is shown in Figure 53. This timing also applies to the timing during EV mode of operation.



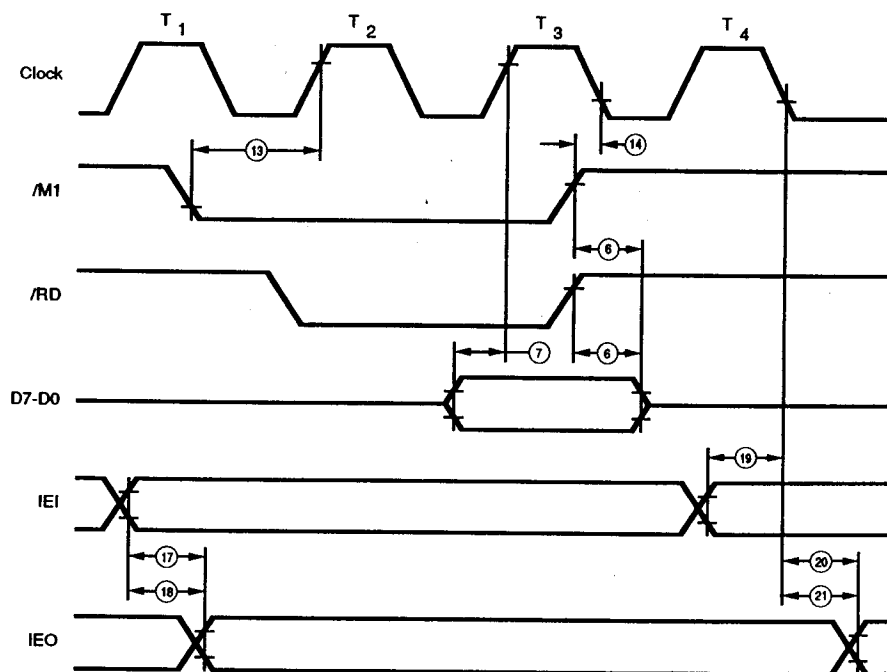
(a) On-chip peripheral I/O access from External Bus master  
(See Tables C and F)

Figure 53. On-chip Peripheral Timing from External Bus master





(b) Interrupt Acknowledge Cycle Timing for On-chip peripheral from External Bus master  
(See Table C)

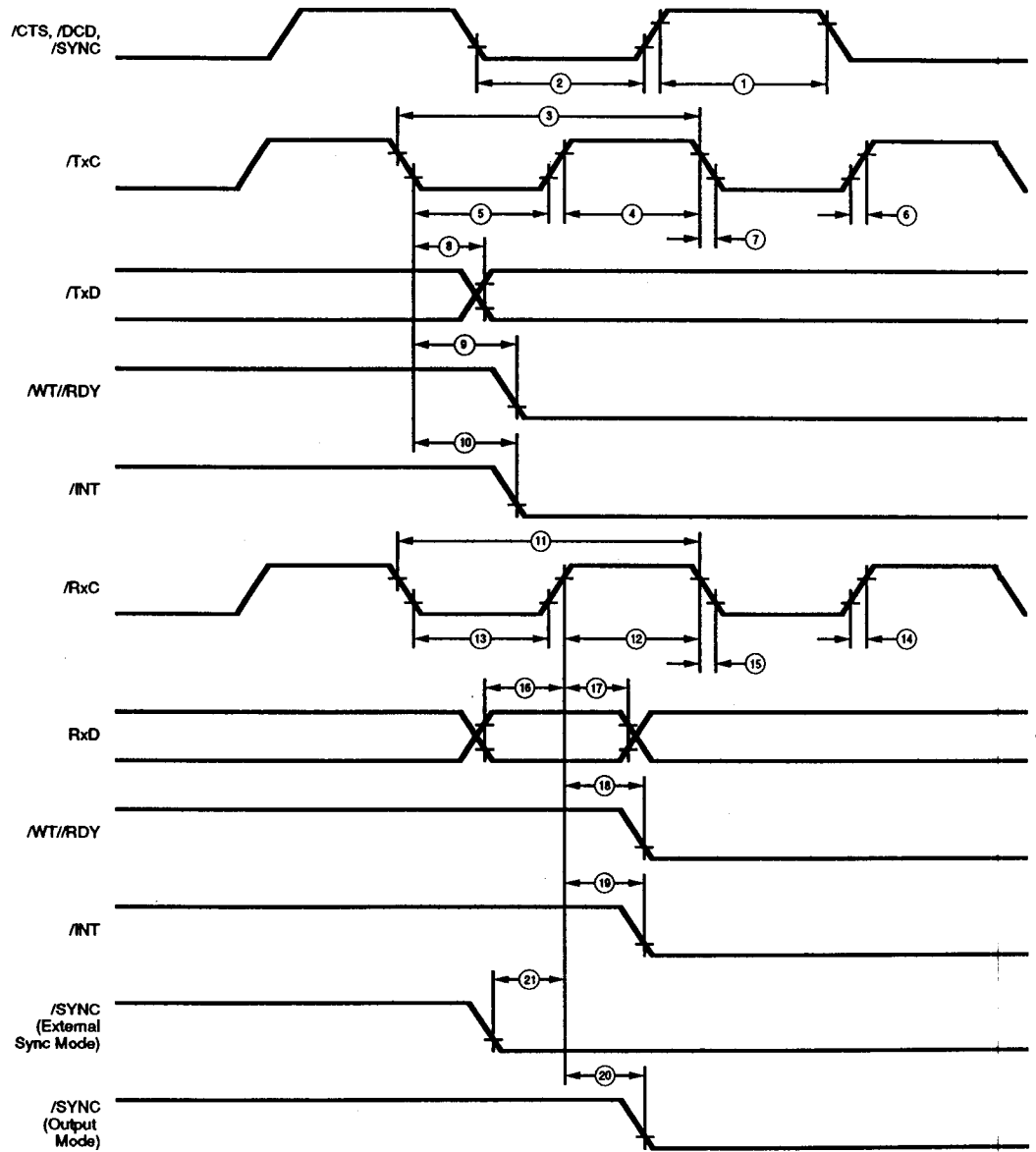


(c) Op-code fetch Cycle Timing for On-chip peripheral from External Bus master  
(See Table C)

Figure 53. On-chip Peripheral Timing from External Bus master (Continued)

# SIO Timing

Figure 56 shows the timing for on-chip SIO.



**Figure 56. SIO Timing**  
(See Table F)

## STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature range is:

E = -40°C to 100°C

Voltage Supply Range:

$+4.50V \leq V_{CC} \leq +5.50V$

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pF.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

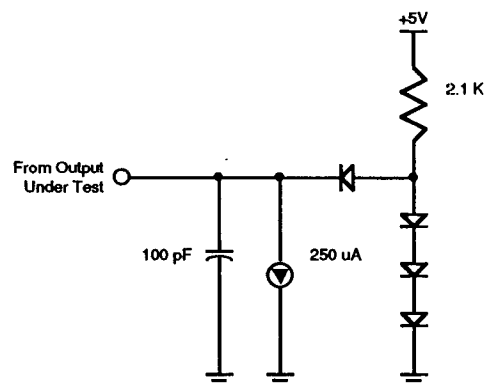


Figure 58. Standard Test Load

## CAPACITANCE

Guaranteed by design and characterization

Symbol	Parameter	Min	Max	Unit
$C_{\text{clock}}$	Clock Capacitance	35	pF	
$C_{\text{IN}}$	Input Capacitance	5	pF	
$C_{\text{OUT}}$	Output Capacitance	15	pF	

**Table F. SIO Timing** (See Figures 53(a) and 56)

No	Symbol	Parameter	Z84C1306 Z84C1506		Z84C1310 Z84C1510		Z84C1316* Z84C1516		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	TwPh	Pulse Width (High)	150		120		80		ns	[F1]
2	TwPl	Pulse Width (Low)	150		120		80		ns	
3	TcTxC	/TxC Cycle Time	250		200		120		ns	
4	TwTxCH	/TxC Width (High)	85		80		55		ns	
5	TwTxCL	/TxC Width (Low)	85		80		55		ns	
6	TrTxC	/TxC Rise Time		60		60		60	ns	[F1]
7	TfTxC	/TxC Fall Time		60		60		60	ns	
8	TdTxCl(TxD)	/TxC Fall to TxD Delay		160		120		40	ns	
9	TdTxCl(W/RRf) (Ready Mode)	/TxC Fall to /W//RDY Fall Delay	5	9	5	9	5	8	TcC	
10	TdTxCl(INTf)	/TxC Fall to /INT Fall Delay	5	9	5	9	5	9	TcC	
11	TcRxC	/RxC Cycle Time	250		200		120		ns	[F1]
12	TwRxCh	/RxC Width (High)	85		80		55		ns	
13	TwRxCl	/RxC Width (Low)	85		80		55		ns	
14	TrRxC	/RxC Rise Time		60		60		60	ns	
15	TfRxC	/RxC Fall Time		60		60		60	ns	
16	TsRxD(RxCr)	RxD to /RxC Rise Setup Time (X1 Mode)	0		0		0		ns	[F1]
17	ThRxCr(RxD)	/RxC Rise to RxD Hold Time (X1 Mode)	80		60			40	ns	
18	TdRxCr(W/RRf)	/RxC Rise to /W//RDY Fall Delay (Ready Mode)	10	13	10	13	10	13	TcC	
19	TdRxCr(INTf)	/RxC Rise to /INT Fall Delay	10	13	10	13	10	13	TcC	
20	TdRxCr(SYNCf)	/RxC Rise to /SYNC Fall Delay (Output Modes)	4	7	4	7	4	7	TcC	
21	TsSYNCf(RxCr)	/SYNC Fall to /RxC Rise Setup (External Sync Modes)	-100		-100		-100		ns	[F2]
22	TdIOf(W/RRf)	/IORQ Fall or Valid Address to /W//RDY Delay (Wait Mode)		130		110		40	ns	[F2]
23	TdCr(W/RRf)	Clock Rise to /W//RDY Delay (Ready Mode)		85		85		40	ns	[F2]
24	TdCl(W/Rz)	Clock Fall to /W//RDY Float Delay (Wait Mode)		90		80		40	ns	[F2]

**Notes:**

[F1] In all modes, the System Clock rate must be at least five times the maximum data rate.

[F2] Parameters 22 to 24 are on Figure 53a.

## AC CHARACTERISTICS (Continued)

Table G. Watch Dog Timer Timing (See Figure 57)

No	Symbol	Parameter	Z84C1306 Z84C1506		Z84C1310 Z84C1510		Z84C1316* Z84C1516		Units
			Min	Max	Min	Max	Min	Max	
1	TdC(WDTf)	Clock Rise to /WDTOUT Fall Delay		160		160		160	ns
2	TdCr(WbTc)	Clock Rise to /WDTOUT Rise Delay		165		165		160	ns
3	TcWDT	/WDTOUT Cycle Time							
		WDTP = 00	(Typ)2 <sup>16</sup> TcC		(Typ)2 <sup>16</sup> TcC		(Typ)2 <sup>16</sup> TcC		ns
		WDTP = 01	(Typ)2 <sup>16</sup> TcC		(Typ)2 <sup>16</sup> TcC		(Typ)2 <sup>16</sup> TcC		ns
		WDTP = 10	(Typ)2 <sup>20</sup> TcC		(Typ)2 <sup>20</sup> TcC		(Typ)2 <sup>20</sup> TcC		ns
		WDTP = 11	(Typ)2 <sup>22</sup> TcC		(Typ)2 <sup>22</sup> TcC		(Typ)2 <sup>22</sup> TcC		ns

### Notes:

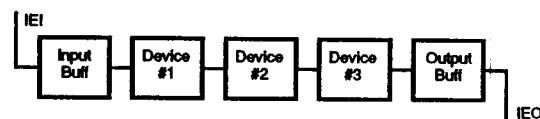
- \* In all modes, the System Clock rate must be at least five times the maximum data rate.  
RESET must be active a minimum of one complete clock cycle.

[1] Units equal to System Clock Periods.

[2] Units in nanoseconds (ns).

### Additional information for note [C3]

Parameter #15, 16, 17 and 18 of Table C. These parameters are daisy-chain timing and calculated values, and vary depending on the inside daisy-chain configuration, which is specified in the Interrupt Priority Register. Inside the IPC, the daisy chain can be figured as follows:



Internal Daisy Chain Configuration

No	Parameter	6 MHz		10 MHz		16 MHz*		Units
		Min	Max	Min	Max	Min	Max	
15	TdM1(IEO)		160		100		100	ns
16	TsIEI(IEO) (PIO at #3)	160		100		100		ns
	(CTC at #3)	160		100		100		ns
	(SIO at #3)	160		100		100		ns
17	TdIEI(IEOf)		120		70		100	ns
18	TdIEI(IEOr)		120		70		100	ns

To calculate IPC daisy-chain timing, it can be treated as if there are Z80 PIO, CTC and SIO with Input buffer and look ahead circuit on the chain. Following are the calculation formulas:

Parameter Table C, #15, /M1 falling to IEO delay  
 $TsM1(IEO) = \text{Max}[TdM1(IEO)\#1, TdM1(IEO)\#2, TdM1(IEO)\#3] + (\text{look-ahead gate Delay})$

Parameter Table C, #16, IEI to /IORQ falling setup time  
 $TsIEI(IEO) = TdIEI(IEO)\#1 + TdIEI(IEO)\#2 + TsIEI(IEO)\#3 + (\text{Input Buffer delay})$

Parameter Table C, #17, IEI falling to IEO falling delay  
 $TdIEI(IEOf) = \text{Max}[TdIEI(IEOf)PIO, TdIEI(IEOf)CTC, TdIEI(IEOf)SIO] + (\text{Input Buffer delay}) + (\text{look-ahead gate Delay})$

Parameter Table C, #18, IEI rising to IEO rising delay (After ED decode)  
 $TdIEI(IEOr) = TdIEI(IEOr)PIO + TdIEI(IEOr)CTC + TdIEI(IEOr)SIO + (\text{Input Buffer delay}) + (\text{look-ahead gate Delay})$

\* Where TdIEI(IEO) is worse number between TdIEI(IEOr) and TdIEI(IEOf)