Zilog - Z8401510FEC00TR Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8401510fec00tr

CPU SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
A0-A15	16-1(x13), 6-1, 100-91(x15)	I/O	16-bit address bus. Specifies I/O and memory addresses to be accessed. During the refresh period, addresses for refreshing are output. The bus is an input when the external master is accessing the on-chip peripherals.
D0-D7	83-76(x13), 89-82(x15)	I/O	8-bit bidirectional data bus. When the on-chip CPU is accessing on-chip peripherals, these lines are set to output and hold the data to/from on-chip peripherals.
/RD	30(x13), 14(x15)	I/O	Read signal. CPU read signal for accepting data from memory or I/O devices. When an external master is accessing the on-chip peripherals, it is an input signal.
/WR	20(x13), 13(x15)	I/O	Write Signal. This signal is output when data, to be stored in a specified memory or peripheral LSI, is on the MPU data bus. When an external master is accessing the on-chip peripherals, it is an input signal.
/MREQ	23(x13), 17(x15)	I/O, 3-State	Memory request signal. When an effective address for memory access is on the address bus, "0" is output. When an external master is accessing the on-chip peripherals, it is an tri-state signal.
/IORQ	21(x13), 15(x15)	I/O	I/O request signal. When addresses for I/O are on the lower 8 bits (A7-A0) of the address bus in the I/O operation, "0" is output. In addition, the /IORQ signal is output with the /M1 signal at the time of interrupt acknowledge cycle to inform peripheral LSI of the state of the interrupt response vector is when put on the data bus. When an external master is accessing the on-chip peripherals, it is an input signal.
/M1	17(x13), 8(x15)	I/O	Machine cycle "1". /MREQ and "0" are output together in the operation code fetch cycle. /M1 is output for every opcode fetch when a two byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with /IORQ. It is 3-stated in EV mode.

The following pins have different functions between 013/015 and C13/C15

Pin Name	Pin # X13	Pin # X15	Function
/RESET	28	9	Functionality is different.
/WAIT	19	15	Functionality is different.
EV	58	67	Functionality is different.
/WDTOUT	61	73	Push-pull output on Z84013/015, Open drain on Z84 C13/C15
ICT	40, 42	42, 40	(Test pin) on Z84013/015; /CS0 and /CS1 on Z84C13/15.
TxCA, TxCB, RxCA and RxCB	35, 36, 50, 51	33, 34, 48, 49	On Z84C13/15; these signals have Schmitt-triggered inputs.
/BUSACK	29	12	In EV mode, 3-stated on Z84C13/15; remains active on Z84013/015.

FUNCTIONAL DESCRIPTION

Figure 5(a) shows the functional block diagram of the Z84013/015 and Figure 5(b) shows the functional block diagram of the Z84C13/C15. As described earlier, the only difference between the Z84x13 and the Z84x15 is the PIO not being available on the Z84x13.

Functionally, the on-chip SIO, PIO (not available on Z84x13), CTC, and the Z80 CPU are the same as the discrete devices. Therefore, for detailed description of each individual unit, refer to the Product Specification/Technical Manual of each discrete product.

The following subsections describe each individual functional unit of the IPC.

Z84C00/01 Logic Unit
The CPU provides all the capabilities and pins of the Zilog Z80 CPU. This allows 100% software compatibility with existing Z80 software. In addition, it has the pin called "A7RF" to extend DRAM refresh address to 8-bits. Refer to "Z84C01 Z80 CPU with CGC" Product Specification.

Z84C20 Parallel Input/Output Logic Unit (Z84x15 Only)
This logic unit provides both TTL- and CMOS- compatible interfaces between peripheral devices and a CPU through the use of two 8-bit parallel ports (Figure 6). The CPU configures the logic to interface to a wide range of peripheral devices with no external logic. Typical devices that are compatible with this interface are keyboards, printers, and EPROM/PAL programmers.

The parallel ports (designated Port A and Port B) are byte wide and completely compatible with the Z84C20 PIO. These two ports have several modes of operation; input, output, bi-directional, or bit control mode. Each port has two handshake signals (RDY and /STB) which are used to control data transfers. The RDY (ready) indicates that the port is ready for data transfer while /STB (strobe) is an input to the port that indicates when data transfer has occurred. Each of the ports can be programmed to interrupt the CPU upon the occurrence of specified status conditions, and generate unique interrupt vectors when the CPU responds (for more information on the operation of this portion of the logic, please refer to the Z84C20 PIO Product Specification and Technical Manual).

Z84C30 Counter/Timer Logic Unit
This logic unit provides the user with four individual 8-bit Counter/Timer Channels that are compatible with the Z84C30 CTC (Figure 7). The Counter/Timers can be programmed by the CPU for a broad range of counting and timing applications. Typical applications include event counting, interrupt and interval counting, and serial baud rate clock generation.

Each of the Counter/Timer Channels, designated Channels 0-3, have an 8-bit prescaler (when used in timer mode) and its own 8-bit counter to provide a wide range of count resolution. Each of the channels have their own Clock/Trigger input to quantify the counting process and an output to indicate zero crossing/timeout conditions. With only one interrupt vector programmed into the logic unit, each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.

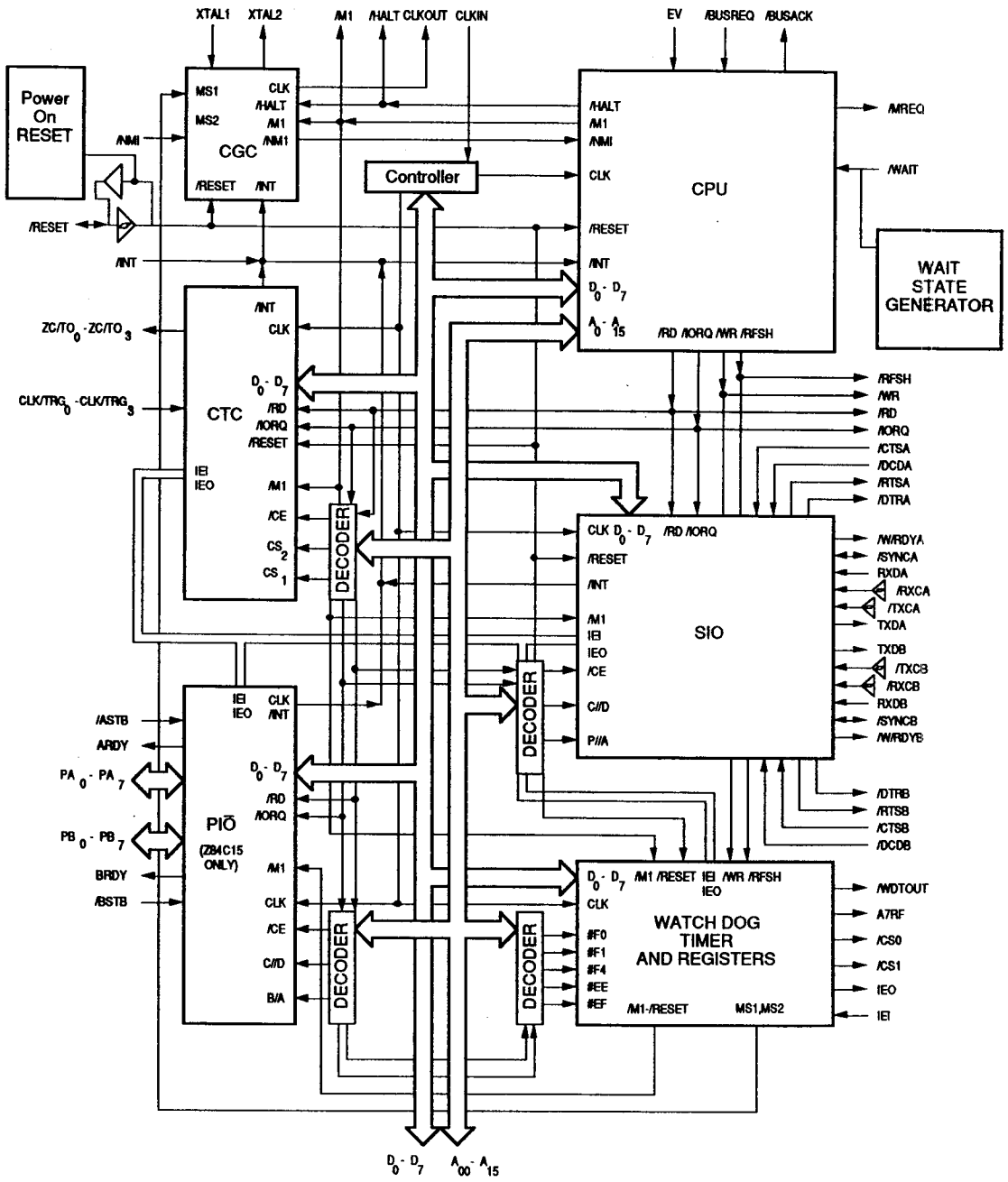


Figure 5(b). Block Diagram for 84C13/C15 IPC

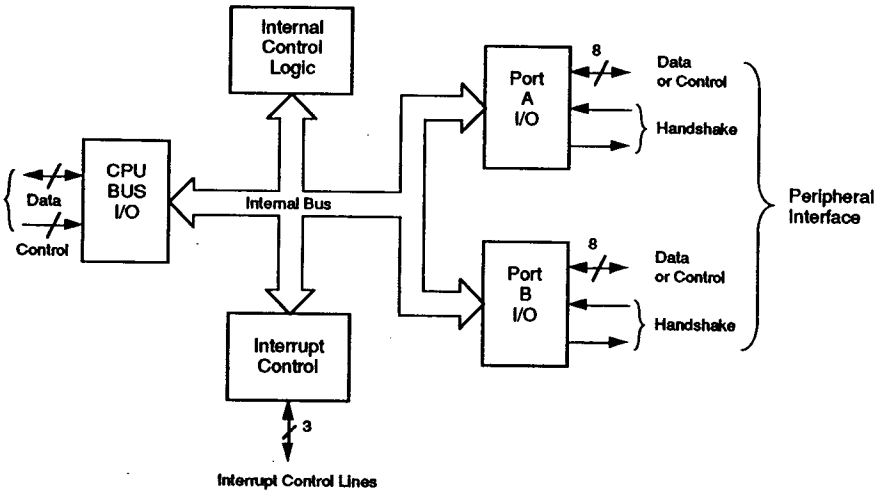


Figure 6. PIO Block Diagram

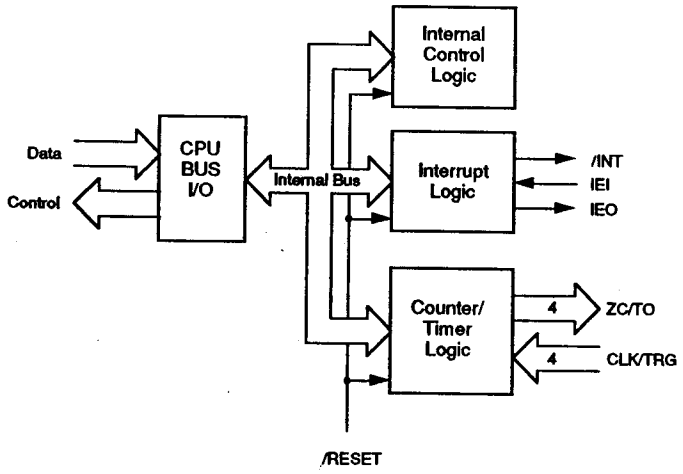


Figure 7. CTC Block Diagram

Z84C4x Serial I/O Logic Unit

This logic unit provides the user with two separate multiprotocol serial I/O channels that are completely compatible with the Z84C4x SIO. Their basic functions as serial-to-parallel and parallel-to-serial converters can be programmed by a CPU for a broad range of serial communications applications. Each channel, designated Channel A and Channel B, is capable of supporting all common asynchronous and synchronous protocols (Monosync, Bisync, and SDLC/HDLC, byte or bit oriented - Figure 8).

Z84C13/C15 Only. As an enhancement to the Z84013/015, the Z84C13/C15 can handle a 32-bit CRC on Channel A and Schmitt-trigger inputs on the /TxC and /RxC pins of both channels.

Recommended characteristics of the crystal and the values for the capacitor are as follows (the values will change with crystal frequency).

- Type of crystal: Fundamental, parallel type crystal (AT cut is recommended).
- Frequency tolerance: Application dependent.
- CL, Load capacitance: Approximately 22pf (acceptable range is 20-30pf).
- Rs, equivalent-series resistance: ≤ 150 ohms.
- Drive level: 10mW (for ≤ 10MHz crystal); 5mW (for ≥ 10MHz crystal).
- $C_{IN} = C_{OUT} = 33pF$.

Power-On Reset Logic Unit (Z84C13/C15 Only)
The Z84C13/C15 has the enhanced feature of a Power-on Reset Circuit. During the power-up sequence, the open-drain gate of the on-chip power-on Reset circuit drives /RESET pin to "0" for 25 to 75 msec after the power supply passes through approx. 2.2V. After the termination of the "Power-on Reset" cycle, the open-drain gate of the on-chip Power-on Reset circuit stops to drive the /RESET pin. It is required to have external pull-up register on the /RESET pin.

If it receives /RESET input from outside after the power-on sequence and while the Reset Output Disable bit in Misc Control Register is cleared to "0", it will drive the /RESET pin for 16-processor clock cycles from the falling edge of the external /RESET input. Otherwise, the /RESET pin must be kept in the active state for a period of at least 3 system clock cycles.

If there are power-on reset circuits outside of this device, drive this pin with OPEN-DRAIN type gates with pull-up resisters because /RESET signal is driven low for the period mentioned above during the Power-on sequence. If the external Power-on Reset circuit has push-pull type drivers and they drive the /RESET pin to "1" during that period, it may cause damage. In particular, when using Z84C13/C15 in the Z84013/015 socket, modification may be required on the external reset circuit.

Wait State Generator Unit (Z84C13/C15 Only)
The Z84C13/C15 has the enhanced feature of a Wait State Generator circuit. It is capable of generating /WAIT signals to the CPU internally. The status of the External /WAIT input line is sampled after the insertion of software wait states, except for the wait state's insertion of Interrupt Daisy Chain Wait (for this cycle, insertion of a wait state is not simple).

The Wait State Control Register can be programmed to generate multiple Wait states during different CPU cycles listed as follows.

Memory Wait and Opcode wait. The Wait State Generator can put 0 to 3 wait states in memory accesses. Additionally, one added wait state can be inserted during an /M1 (Opcode fetch) cycle, because /M1 cycle's timing requirement is tighter than memory Read/Write cycles. It generates wait states to the Memory Access in a specified address range, which is programmed in the Memory Wait Boundary Register.

I/O Wait. The Wait State generator can put 0, 2, 4 or 6 wait states in I/O accesses. Regardless of the programming of this field, no I/O wait states are inserted for accesses to on-chip peripherals.

Interrupt Vector Wait. During Interrupt acknowledge cycle, the Wait State Generator can insert one wait state after /IORQ goes active, to extend the time between /IORQ fall to vector fetch by CPU. It allows a slow vector response device.

Interrupt Daisy Chain Wait and RETI sequence extension. During Interrupt acknowledge cycle, the Wait State Generator can insert 0, 2, 4 or 6 wait states between /M1 falling to /IORQ falling edge, to extend the time required to settle daisy chain. This allows a longer daisy chain. Also, this field controls the number of wait states inserted during RETI (Return From Interrupt) cycle. If specified to insert 4 or 6 wait states during Interrupt Acknowledge cycle, Wait State Generator also inserts wait states during RETI fetch sequence. This sequence is generated with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts 2 or 4 wait states, respectively, if op-code followed by EDh is 4Dh. One wait state if the following op-code is not 4Dh.

Chip Select Signals (Z84C13/C15 Only)
The Z84C13/C15 has an enhanced feature of adding two chip select (/CS0, /CS1) pins. Both signals are originally IC test pins (ICT) on the Z84013/015. The boundary value for each Chip Select Signal is 4 bits wide, and compare with A15-A12 of the address. Each Chip Select Signal goes active when:

/CS0: (D3-D0 of CSBR) ≥ A15-A12 ≥ 0
/CS1: (D7-D4 of CSBR) ≥ A15-A12 > (D3-D0 of CSBR)

(Where CSBR is the contents of Chip Select Boundary Register.)

There is also a separate /CS enable bit. /CS0 is enabled on power-up with a boundary value of "F" causing /CS0 to go active for all memory accesses. /CS1 is disabled on

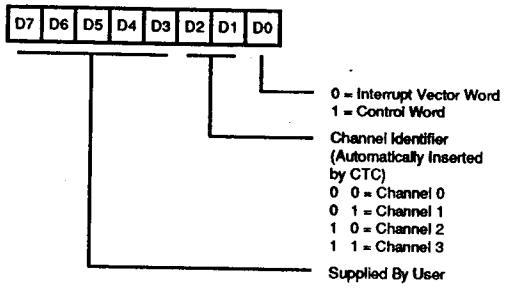


Figure 19. CTC Interrupt Vector Word

SIO REGISTERS

For more detailed information, refer to the SIO Technical Manual.

Read Registers. The SIO channel B contains three read registers while channel A contains only two that are read to obtain status information. To read the contents of a register (rather than RR0), the program must first write a pointer to WR0 in exactly the same manner as a write operation. The next I/O read cycle will place the contents of the selected read registers onto the data bus (Figure 20a, b, c).

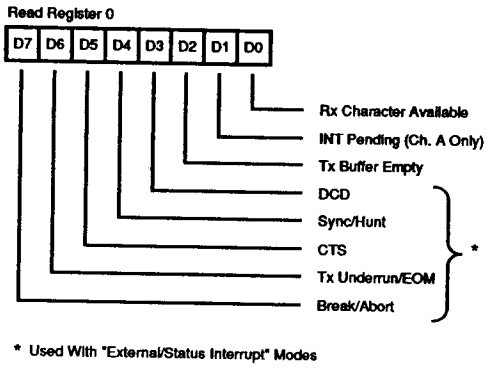


Figure 20a. SIO Read Register 0

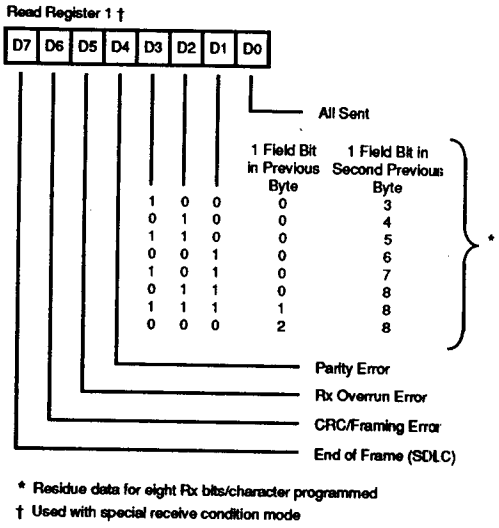


Figure 20b. SIO Read Register 1

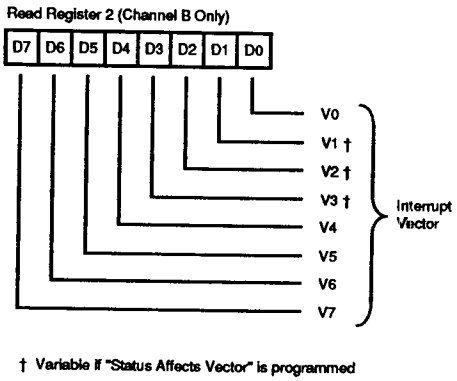


Figure 20c. SIO Read Register 2

Write Registers. The SIO Channel B contains eight write registers while Channel A contains only seven that are programmed to configure the operating mode characteristics of each channel. With the exception of WR0, programming the write registers is a two step operation. The first operation is a pointer written to WR0 which points to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel (Figure 21).

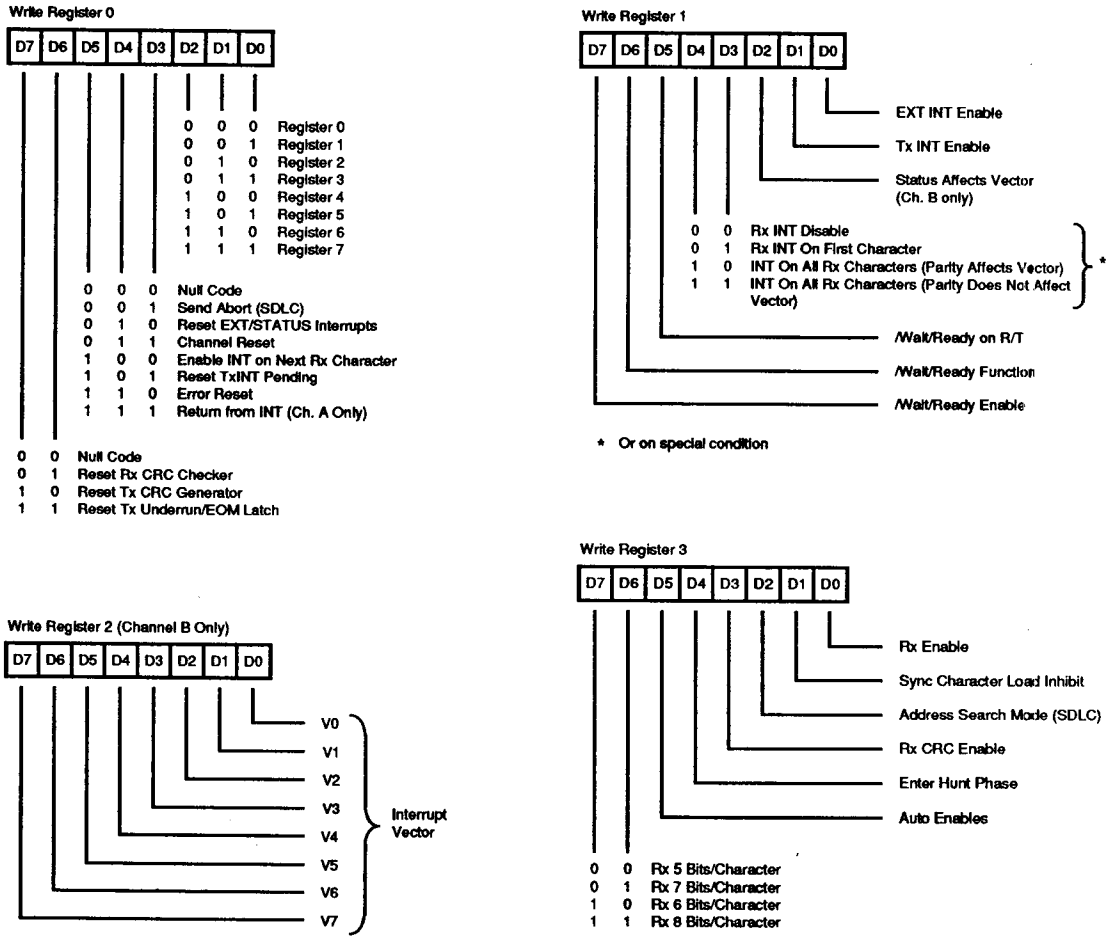


Figure 21. SIO Write Registers

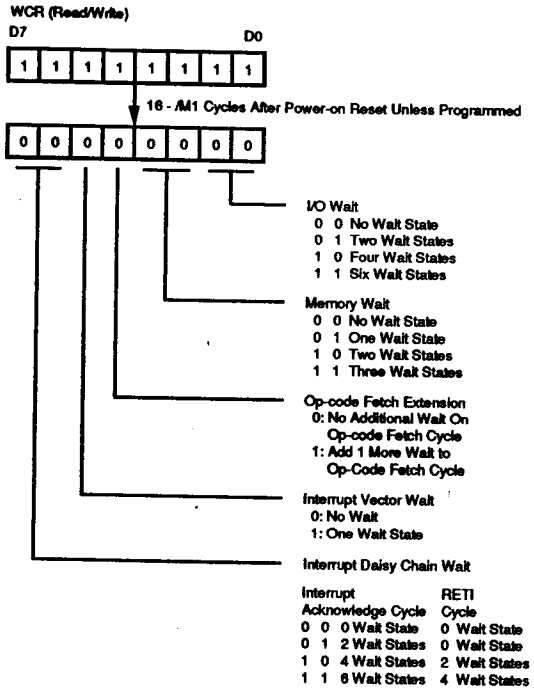


Figure 27. Wait State Control Register

This register has the following fields:

Bit 7-6. *Interrupt Daisy Chain Wait.* This 2-bit field specifies the number of wait states to be inserted during an Interrupt Daisy Chain settle period of the Interrupt Acknowledge cycle, which is/IORQ falls after the settling period from /M1 going active "0". Also, this field controls the number of wait states inserted during the RETI (Return From Interrupt) cycle. If specified to insert 4 or 6 wait states during Interrupt Acknowledge cycle, the Wait state generator also inserts wait states during RETI fetch sequence. This sequence is formed with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts 1 wait state if op-code followed by EDh is NOT 4Dh, and inserts 2 or 4 wait states, respectively, if the following op-code is 4Dh.

Interrupt Acknowledge	RETI cycle
00 - No Wait states	No Wait states
01 - 2 Wait states	No Wait states
10 - 4 Wait states	2 Wait states
11 - 6 Wait states	4 Wait states

For fifteen /M1 cycles from Power-on Reset, bits 7-6 are set to "11" . They clear to "00" on the trailing edge of the 16th /M1 signal unless programmed.

Bit 5. *Interrupt Vector Wait.* While this bit is set to one, the wait state generator inserts one wait state after the /IORQ signal goes active during the Interrupt acknowledge cycle. This gives more time for the vector read cycle. While this bit is cleared to zero, no wait state is inserted (standard timing). For fifteen /M1 cycles from Power-on Reset, this bit is set to "1", then cleared to "0" on the trailing edge of the 16th /M1 signal, unless programmed.

Bit 4. *Opcode Fetch Extension.* If this bit is set to "1", one additional wait state is inserted during the Op-code fetch cycle in addition to the number of wait states programmed in the Memory Wait field. For fifteen /M1 cycles from Power-on Reset, this bit is set to "1", then cleared to "0" on the trailing edge of the 16th /M1 signal, unless programmed.

Bit 3-2. *Memory Wait States.* This 2-bit field specifies the number of wait states to be inserted during memory Read/ Write transactions.

00 - No Wait states
01 - 1 Wait states
10 - 2 Wait states
11 - 3 Wait states

For fifteen /M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the16th /M1 signal, unless programmed.

Bit 1-0. *I/O Wait states.* This 2-bit field specifies the number of wait states to be inserted during I/O transactions.

00 - No Wait states
01 - 2 Wait states
10 - 4 Wait states
11 - 6 Wait states

For fifteen /M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the16th /M1 signal, unless programmed. For the accesses to the on-chip I/O registers, no Wait states are inserted regardless of the programming of this field.

Memory Wait Boundary Register (MWBR, Control Register 01h)

This register specifies the address range to insert memory wait states. When accessed memory addresses are within this range, the Memory Wait State generator inserts Memory Wait States specified in the Memory Wait field of WCR (Figure 28).

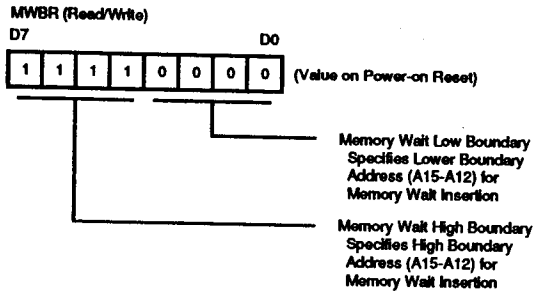


Figure 28. Memory Wait Boundary Register

Bit D7-D4. *Memory Wait High Boundary.* This field specifies A15-A12 of the upper address boundary for Memory Wait.

Bit D3-D0. *Memory Wait Low Boundary.* This field specifies A15-12 of the lower address boundary for Memory Wait.

Memory Wait states are inserted for the address range:

(D7-D4 of MWBR) ≥ A15-A12 ≥ (D3-D0 of MWBR)

This register is set to "F0h" on Power-on Reset, which specifies the address range for Memory Wait as "0000h to FFFFh".

Chip Select Boundary Register (CSBR, Control Register 02h)

This register specifies the address range for each chip select signal. When accessed memory addresses are within this range, chip select signals are active (Figure 29).

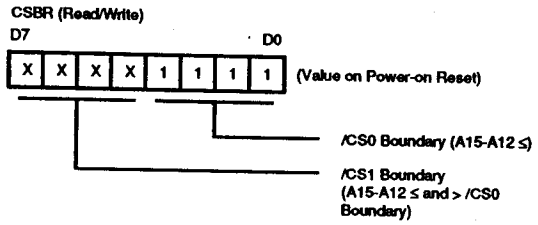


Figure 29. Chip Select Boundary Register

D7-D4. */CS1 Boundary Address.* These bits specify the boundary address range for /CS1. The bit values are ignored on power-up as the /CS1 enable bit is off. The /CS1 is asserted if the address lines A15-12 have an address value greater than the programmed value for /CS0, and less than or equal to the programmed value in these bits.

D3-D0. */CS0 Boundary Address.* These bits specify the boundary address range for /CS0. /CS0 is asserted if the address lines A15-12 have an address value less than or equal to the programmed boundary value. The /CS0 enable bit in the MCR must be set to 1. Upon Power-up reset, these bits come up as all 1's so that /CS0 is asserted for all addresses.

Chip Select signals are active for the address range:

/CS0: (D3-D0 of CSBR) ≥ A15-A12 ≥ 0
/CS1: (D7-D4 of CSBR) ≥ A15-A12 > (D3-D0 of CSBR)

This register is set to "xxxx1111b" on Power-on Reset, which specifies the address range of /CS0 for "0000h to FFFFh" (all Memory location) and /CS1 "undefined."

Misc Control Register (MCR, Control Register 03h)

This register specifies miscellaneous options on this device (Figure 30).

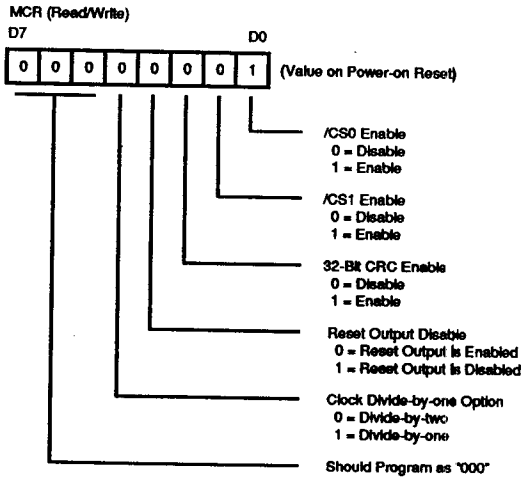


Figure 30. Misc Control Register

Bit D7-D5. *Reserved.* These three bits are reserved and are always programmed as "000".

Bit D4. *Clock Divide-by-one option.* "0"-Disable, "1"-enable. On-chip CGC unit has divide-by-two circuit. By setting this bit to one, this circuit is bypassed and CLKOUT is equal to X'tal oscillator frequency (or external clock input on the XTAL1 pin). This bit has no effect when the on-chip CGC unit is not in use and the external system clock is fed from CLKIN pin. Upon Power-on Reset, this bit is cleared to 0 and the clock is divided by two.

In RUN Mode, output from the CGC unit (CLKOUT) is not stopped and the internal system clock (Ø) continues even after the halt instruction is executed. Therefore, until the halt state is released by the interrupt signal (/NMI or /INT) or /RESET signal, MPU continues to execute HALT instructions (internally executing NOP instructions).

IDLE1 Mode (HALTM=00). Shown in Figure 32 is the basic timing when the halt instruction is executed in IDLE1 Mode.

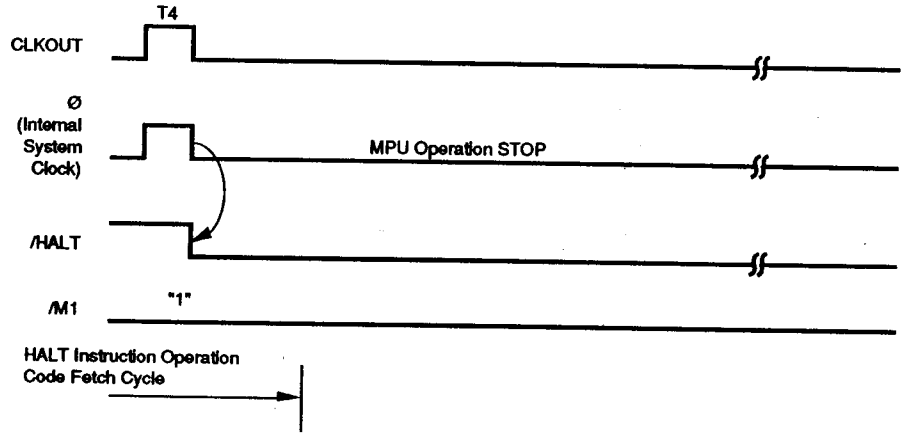


Figure 32. IDLE1 Mode Timing
(At Halt Instruction Execution)

In IDLE1 Mode, the internal oscillator continues to operate, but clock output (CLKOUT) is stopped at T4 Low state of HALT instruction execution. Then all components in the MPU stop their operation. This mode is not supported when the CGC unit is inactive and the external clock is fed from CLKIN pin; CLKOUT should be connected to CLKIN.

IDLE2 Mode (HALTM=01). Shown in Figure 33 is the basic timing when the halt instruction is executed in IDLE2 Mode.

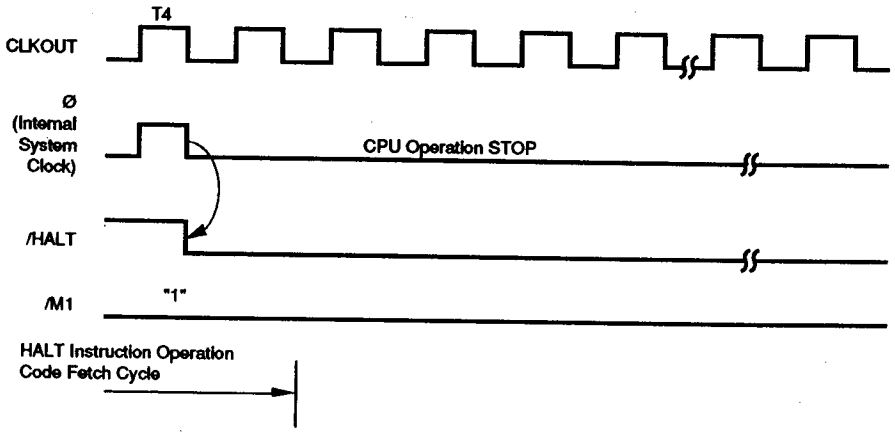


Figure 33. IDLE2 Mode Timing
(At Halt Instruction Execution)

In IDLE2 Mode, the internal oscillator and clock output (CLKOUT) continue to operate. The internal system clock, fed from CLKIN to the components other than CTC is stopped at the T4 Low state of HALT instruction execution.

STOP Mode (HALTM=10). Shown in Figure 34 is the basic timing when the halt instruction is executed in STOP Mode.

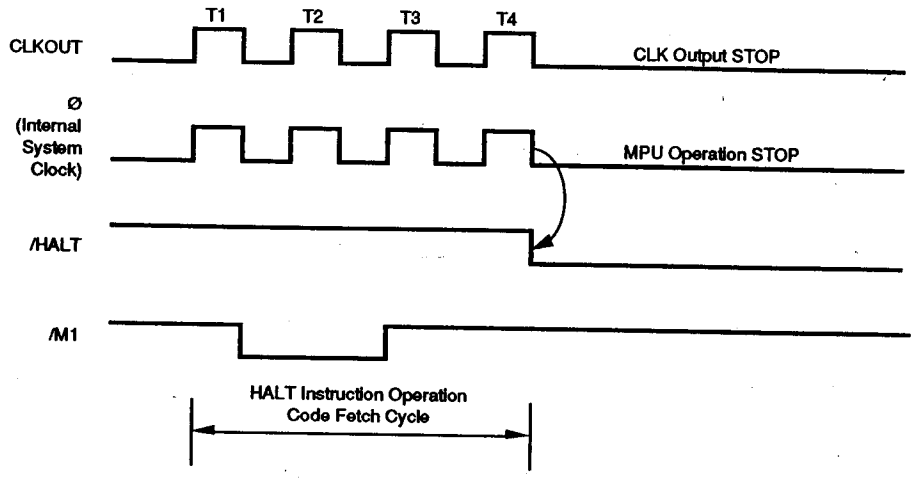


Figure 34. STOP Mode Timing
(At Halt Instruction Execution)

In STOP Mode, the on-chip CGC unit is stopped at T4 Low state of HALT instruction execution. Therefore, clock output (CLKOUT), operation of Watch Dog Timer, CPU, PIO, CTC, SIO are stopped.

Release from Halt State. The halt state of the CPU is released when "0" is input to the /RESET signal and the MPU is reset or an interrupt request is accepted. An interrupt request signal is sampled at the leading edge of the last clock cycle (T4 state) of NOP instruction. In case of the maskable interrupt, interrupt will be accepted by an active /INT signal ("0" level). Also, the interrupt enable flip-flop is set to "1". The accepted interrupt process is started from the next cycle.

Further, when the internal system clock is stopped (IDLE1/2 Mode, STOP Mode), it is necessary first to restart the internal system clock. The internal system clock is restarted when /RESET or interrupt signal (/NMI or /INT) is asserted.

RUN Mode (HALTM=11). The halt release operation is enabled by interrupt request in RUN Mode (Figure 35).

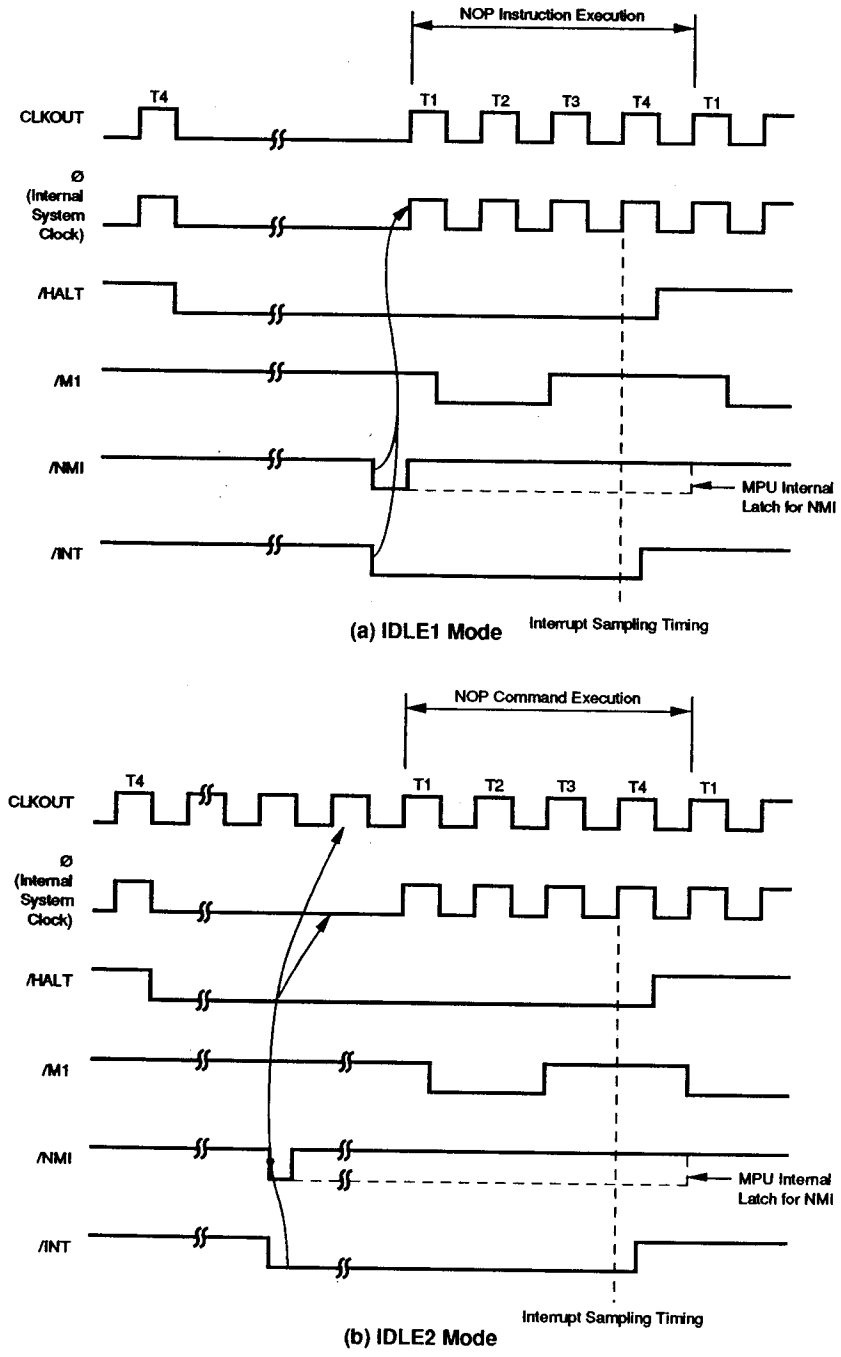
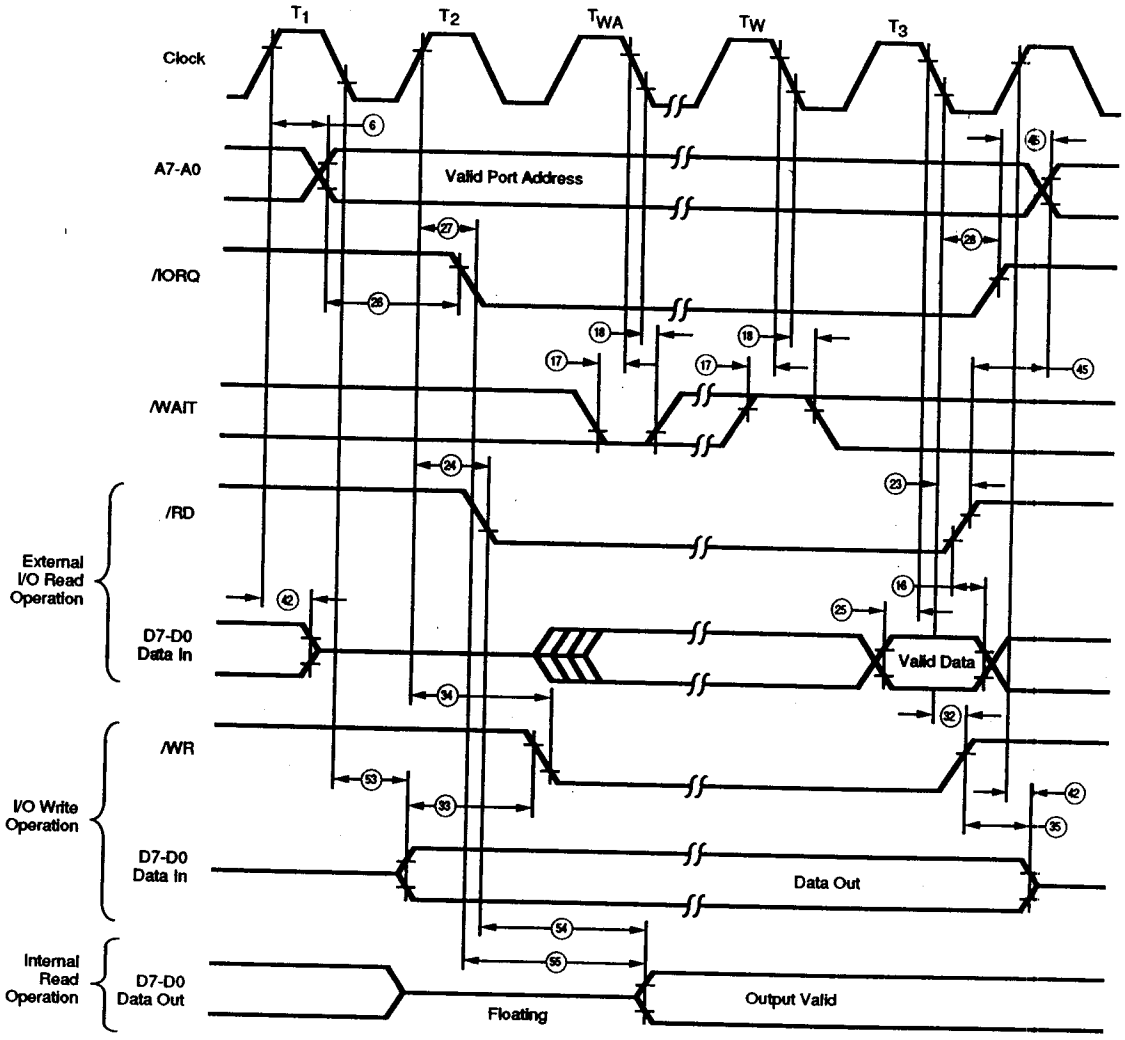


Figure 37. Halt Release Operation Timing By Interrupt Request Signal in IDLE1/2 Mode

Input or Output Cycles. Figure 43 shows the timing for an I/O read or I/O write operation. During I/O operations, the CPU automatically inserts a single Wait state (T_{WA}). This extra Wait state allows sufficient time for an I/O port to decode the address from the port address lines.

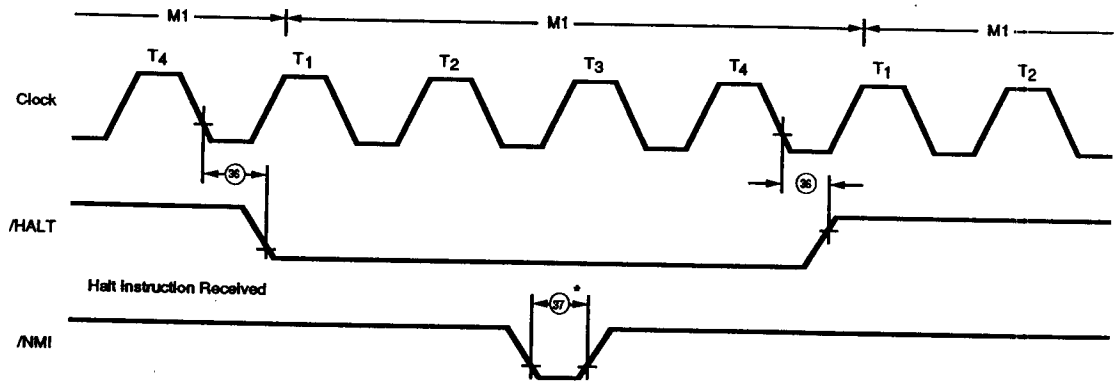
When the CPU is accessing the on-chip I/O registers (PIO, CTC, SIO and system control registers), the data from/to these registers also appears on the data bus, or data bus is output during I/O cycle.



Note: T_{WA} = One wait cycle automatically inserted by CPU

Figure 43. Input or Output Cycle
(See Table A)

Halt acknowledge cycle. Figure 47 shows the timing for Halt acknowledge cycle.



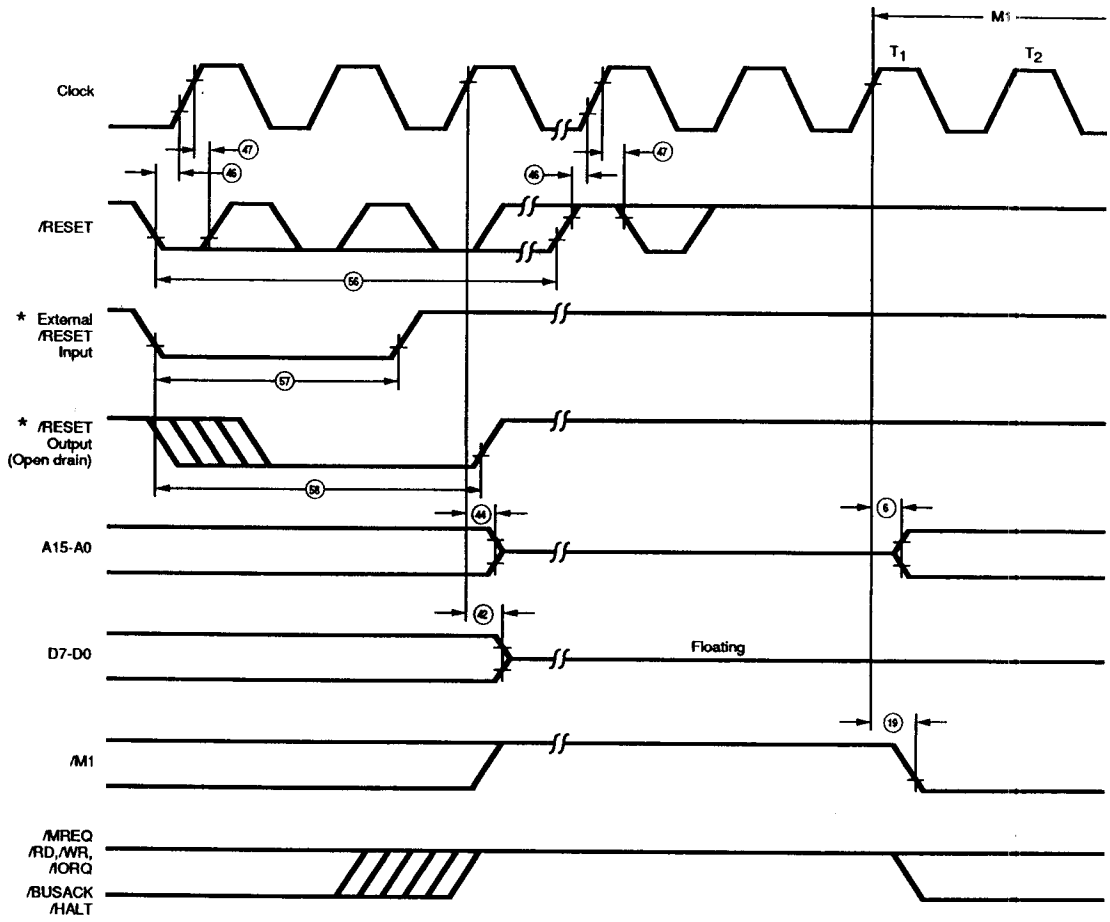
* Although /NMI is an asynchronous input, to guarantee its being recognized on the following machine cycle, /NMI's falling edge must occur no later than the rising edge of the clock preceding the last state of any instruction cycle (T_{LI}).

Figure 47. Halt Acknowledge
(See Table A)

Reset Cycle. /RESET must be active for at least three clock cycles for the CPU to properly accept it. As long as /RESET remains active, the address and data buses float, and the control outputs are inactive.

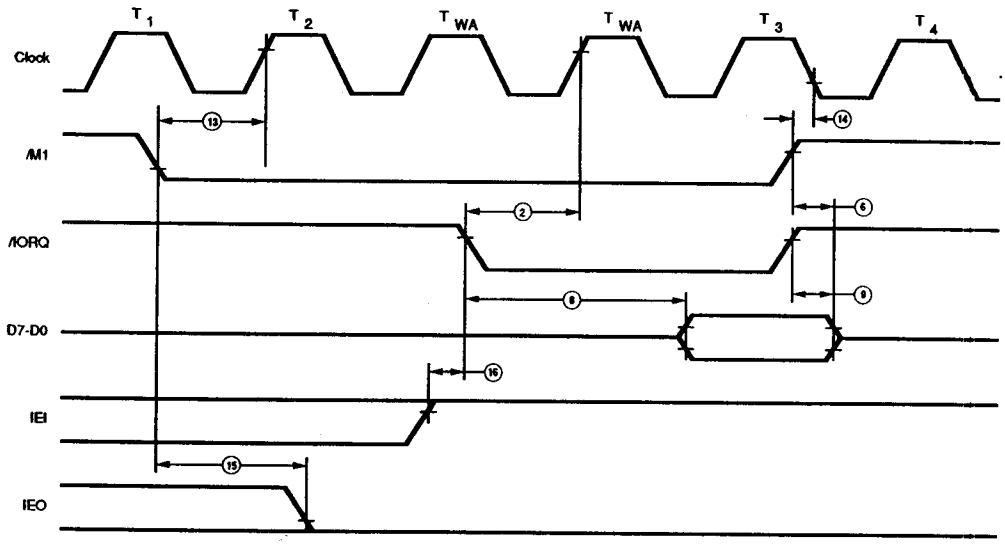
Once /RESET goes inactive, two internal T cycles are consumed before the CPU resumes normal processing operation. /RESET clears the PC register, so the first op-code fetch location is 0000H (Figure 48).

Z84C13/C15 Only. If Reset output is disabled, /RESET must be active for at least three clock cycles for the CPU to properly accept it. Otherwise, /RESET must be active for at least two clock cycles and the on-chip reset circuit extends /RESET signal to at least a minimum of 16-clock cycles.

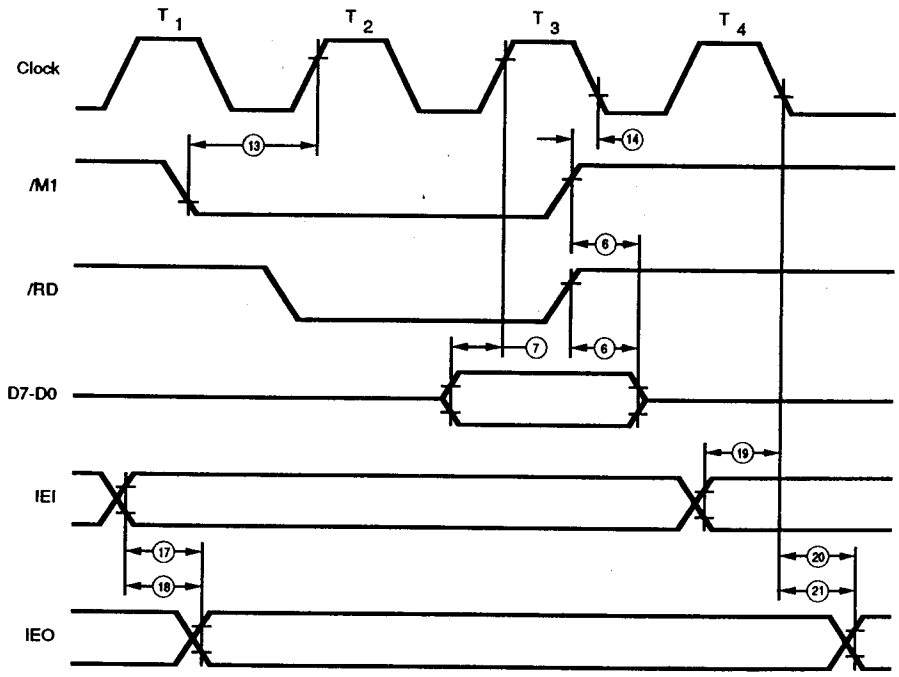


* 84C13/15 Only Reset Output is Enabled

Figure 48. Reset Cycle
(See Table A)



(b) Interrupt Acknowledge Cycle Timing for On-chip peripheral from External Bus master
(See Table C)



(c) Op-code fetch Cycle Timing for On-chip peripheral from External Bus master
(See Table C)

Figure 53. On-chip Peripheral Timing from External Bus master (Continued)

AC CHARACTERISTICS

Table A. CPU Timing (See Figure 41 to 48)

No	Symbol	Parameter	Z84X1306 Z84X1506 Min	Max	Z84X1310 Z84X1510 Min	Max	Z84C1316* Z84C1516 Min	Max	Unit	Note
1	TcC	Clock Cycle time	162**	DC	100**	DC	61	DC	nS	[A1]
2	TwCh	Clock Pulse Width (High)	65	DC	40	DC	20	DC	nS	[A1]
3	TwCl	Clock Pulse Width (Low)	65	DC	40	DC	20	DC	ns	[A1]
4	TfC	Clock Fall time		20		10		6	ns	[A1]
5	TrC	Clock Rise time		20		10		6	ns	[A1]
6	TdCr(A)	Address Valid from Clock Rise		90		65		55	ns	
7	TdA(MREQf)	Address Valid to /MREQ Fall	35**		0**		-15		ns	
8	TdCf(MREQf)	Clock Fall to /MREQ Fall Delay		70		55		40	ns	
9	TdCr(MREQr)	Clock Rise to /MREQ Rise Delay		70		55		40	ns	
10	TwMREQh	/MREQ Pulse Width (High)	65**		30**		10		ns	[A2]
11	TwMREQl	/MREQ Pulse Width (Low)	132**		75**		25		ns	[A2]
12	TdCf(MERQr)	Clock Fall to /MREQ Rise Delay		70		55		40	ns	
13	TdCf(RDf)	Clock Fall to /RD Fall Delay		80		65		40	ns	
14	TdCr(RDr)	Clock Rise to /RD Rise Delay		70		55		40	ns	
15	TsD(Cr)	Data Setup Time to Clock Rise	30		25		10		ns	
16	ThD(RDr)	Data Hold Time After /RD Rise	0		0		0		ns	
17	TsWAIT(Cf)	/WAIT Setup Time to Clock Fall	60		20		75		ns	
18	ThWAIT(Cf)	/WAIT Hold Time After Clock Fall	10		10		10		ns	
19	TdCr(M1f)	Clock Rise to /M1 Fall Delay		80		65		40	ns	
20	TdCr(M1r)	Clock Rise to /M1 Rise Delay		80		65		40	ns	
21	TdCr(RFSHf)	Clock Rise to /RFSH Fall Delay		110		80		60	ns	
22	TdCr(RFSHr)	Clock Rise to /RFSH Rise Delay		100		80		60	ns	
23	TdCf(RDr)	Clock Fall to /RD Rise Delay		70		55		40	ns	
24	TdCr(RDf)	Clock Rise to /RD Fall Delay		70		55		40	ns	
25	TsD(Cf)	Data Setup to Clock Fall During M2, M3, M4 or M5 Cycles	40		25		12		ns	
26	TdA(IORQf)	Address Stable Prior to /IORQ Fall	107**		50**		0		ns	
27	TdCr(IORQf)	Clock Rise to /IORQ Fall Delay		65		50		40	ns	
28	TdCf(IORQr)	Clock Fall to /IORQ Rise Delay		70		55		40	ns	
29	TdD(WRf)	Data Stable Prior to /WR Fall	22**		40**		-10		ns	
30	TdCf(WRf)	Clock Fall to /WR Fall Delay		70		55		40	ns	
31	TwWR	/WR Pulse Width	132**		75**		25		ns	
32	TdCf(WRr)	Clock Fall to /WR Rise Delay		70		55		40	ns	
33	TdD(WRf)IO	Data Stable Prior to /WR Fall	-55**		-10**		-30		ns	
34	TdCr(WRf)	Clock Rise to /WR Fall Delay		60		50		40	ns	
35	TdWRr(D)	Data Stable from /WR Fall	30**		10**		0	0	ns	
36	TdCf(HALT)	Clock Fall to /HALT 0 or 1		260		90		70	ns	
37	TwNMI	/MNI pulse Width	60		60		60		ns	
38	TsBUSREQ(Cr)	/BUSREQ Setup Time to Clock Rise	50		30		15		ns	
39	ThBUSREQ(Cr)	/BUSREQ Hold Time after Clock Rise	10		10		10		ns	
40	TdCr(BUSACKf)	Clock Rise to /BASACK Fall Delay		90		75		40	ns	

Table H. Footnote to Table A.

No	Symbol	Parameter	Z84X1306 Z84X1506	Z84X1310 Z84X1510	Z84C1316* Z84C1516
1	TcC	TwCh + TwCl + TrC + TfC			
7	TdA(MREQf)	TwCh + TfC	-50	-50	-45
10	TwMREQh	TwCh + TfC	-20	-20	-20
11	TwMREQl	TcC	-30	-25	-25
26	TdA(IORQf)	TcC	-55	-50	-50
29	TdD(WRf)	TcC	-140	-60	-60
31	TwWR	TcC	-30	-25	-25
33	TdD(WRf)	TwCl + TrC	-140	-60	-60
35	TdWRr(D)	TwCl + TrC	-55	-40	-25
45	TdCTr(A)	TwCl + TrC	-50	-30	-30
50	TdM1f(IORQf)	2TcC + TwCh + TfC	-50	-30	-30

AC CHARACTERISTICS (Continued)

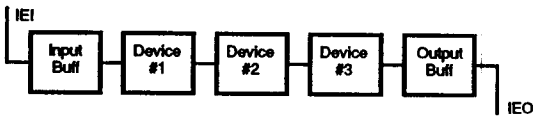
Table G. Watch Dog Timer Timing (See Figure 57)

No	Symbol	Parameter	Z84C1306 Z84C1506 Min	Z84C1306 Z84C1506 Max	Z84C1310 Z84C1510 Min	Z84C1310 Z84C1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Units
1	TdC(WDTf)	Clock Rise to /WDTOUT Fall Delay		160		160		160	ns
2	TdCr(WbTc)	Clock Rise to /WDTOUT Rise Delay		165		165		160	ns
3	TcWDT	/WDTOUT Cycle Time							
		WDTP = 00	(Typ)2^{16}TcC		(Typ)2^{16}TcC		(Typ)2^{16}TcC		ns
		WDTP = 01	(Typ)2^{18}TcC		(Typ)2^{18}TcC		(Typ)2^{18}TcC		ns
		WDTP = 10	(Typ)2^{20}TcC		(Typ)2^{20}TcC		(Typ)2^{20}TcC		ns
		WDTP = 11	(Typ)2^{22}TcC		(Typ)2^{22}TcC		(Typ)2^{22}TcC		ns

Notes:
* In all modes, the System Clock rate must be at least five times the maximum data rate.
RESET must be active a minimum of one complete clock cycle.
[1] Units equal to System Clock Periods.
[2] Units in nanoseconds (ns).

Additional information for note [C3]

Parameter #15, 16, 17 and 18 of Table C. These parameters are daisy-chain timing and calculated values, and vary depending on the inside daisy-chain configuration, which is specified in the Interrupt Priority Register. Inside the IPC, the daisy chain can be figured as follows:



Internal Daisy Chain Configuration

No	Parameter	6 MHz Min	6 MHz Max	10 MHz Min	10 MHz Max	16 MHz* Min	16 MHz* Max	Units
15	TdM1(IEO)		160		100		100	ns
16	TsIEI(IO) (PIO at #3)	160		100		100		ns
	(CTC at #3)	160		100		100		ns
	(SIO at #3)	160		100		100		ns
17	TdIEI(IEOf)		120		70		100	ns
18	TdIEI(IEOr)		120		70		100	ns

To calculate IPC daisy-chain timing, it can be treated as if there are Z80 PIO, CTC and SIO with Input buffer and look ahead circuit on the chain. Following are the calculation formulas:

Parameter Table C, #15, /M1 falling to IEO delay
TsM1(IEO) = Max[TdM1(IO)#1, TdM1(IO)#2, TdM1(IO)#3] + (look-ahead gate Delay)

Parameter Table C, #16, IEI to /IORQ falling setup time
TsIEI(IO) = TdIEI(IEO)#1 + TdIEI(IEO)#2 + TsIEI(IO)#3 + (Input Buffer delay)

Parameter Table C, #17, IEI falling to IEO falling delay
TdIEI(IEOf) = Max[TdIEI(IEOf)PIO, TdIEI(IEOf)CTC, TdIEI(IEOf)SIO] + (Input Buffer delay) + (look-ahead gate Delay)

Parameter Table C, #18, IEI rising to IEO rising delay (After ED decode) TdIEI(IEOr) = TdIEI(IEOr)PIO + TdIEI(IEOr)CTC + TdIEI(IEOr)SIO + (Input Buffer delay) + (look-ahead gate Delay)

* Where TdIEI(IEO) is worse number between TdIEI(IEOr) and TdIEI(IEOf)

	6MHz Min	Max	10MHz Min	Max	16MHz Min	Max
Input Buffer Delay	10nS		10nS		10 nS	
Look ahead gate delay	10nS		10nS		10 nS	

6MHz	PIO part Min	Max	CTC part Min	Max	SIO part Min	Max
TdM1(IEO)		90nS		130nS		150nS
TsIEI(IO)		90nS		100nS		70nS
TdIEI(IEOf)		100nS		90nS		50nS
TdIEI(IEOr)		130nS		90nS		50nS

10MHz	PIO part Min	Max	CTC part Min	Max	SIO part Min	Max
TdM1(IEO)		60nS		60nS		90nS
TsIEI(IO)		50nS		70nS		50nS
TdIEI(IEOf)		50nS		50nS		30nS
TdIEI(IEOr)		50nS		50nS		30nS

Preliminary

16MHz*	PIO part Min	Max	CTC part Min	Max	SIO part Min	Max
TdM1(IEO)		55nS		55nS		90nS
TsIEI(IO)		45nS		65nS		45nS
TdIEI(IEOf)		45nS		45nS		30nS
TdIEI(IEOr)		45nS		45nS		30nS

*** Note:**
16MHz is for C15 only.

If using an interrupt from only a portion of the IPC, these numbers are smaller than the values shown above. For more details about the "Z80 Daisy Chain Structure," please refer to the Application Note "Z80 Family Interrupt Structure" included in the Z80 Data book.