Zilog - Z8401510FEG Datasheet

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Z80
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8401510feg

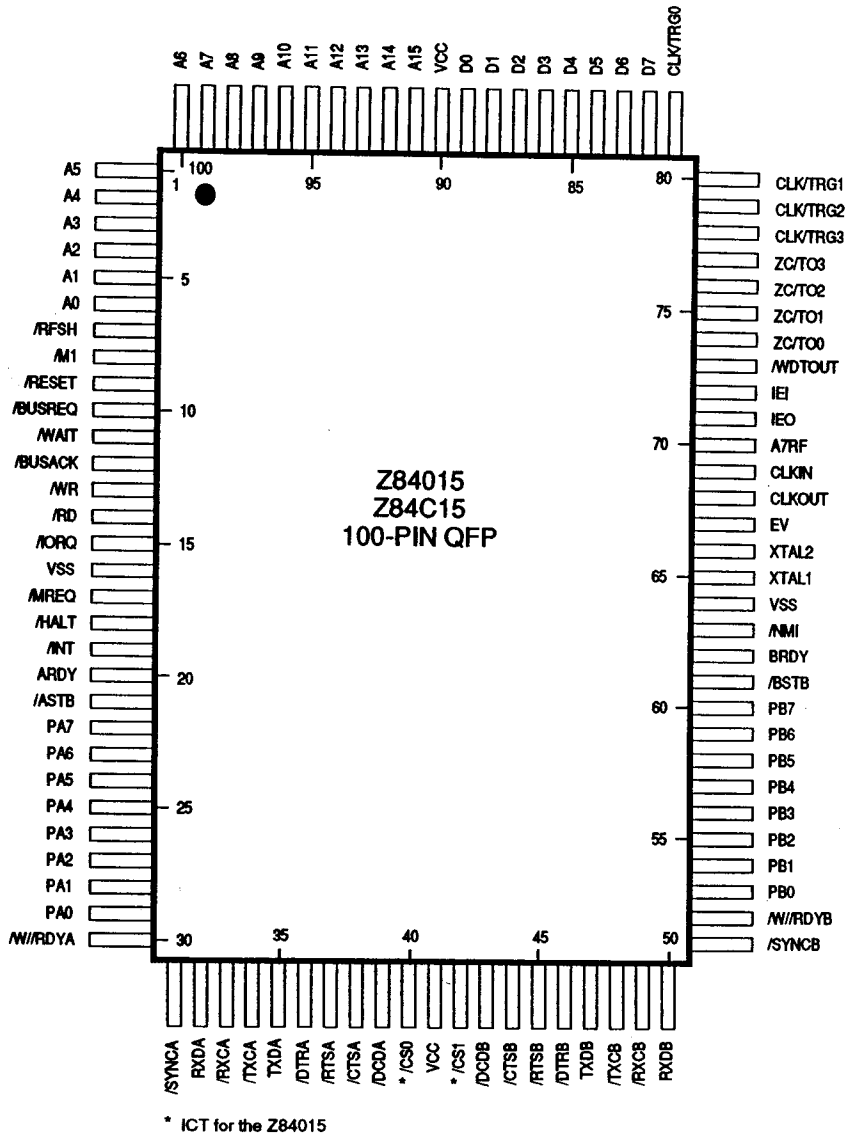


Figure 4. Z84015/Z84C15 Pin-out Assignments

PIN DEFINITIONS

The pin assignment for each device is shown in Figures 3 and 4. Following is the description on each pin. For the description and the pin number, if stated as "x13" or "x15", that applies to both Z84C13/Z84013 or Z84C15/Z84015. Otherwise, C13 for Z84C13, C15 for Z84C15, 013 for Z84013 and 015 for Z84015.

SYSTEM CONTROL SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, 3-State	Function
/CS1 (C13/C15 only)	40(x13), 42(x15)	Out	Chip Select 1. Used to access external memory or I/O devices. This pin has been assigned to "ICT" pin on Z84013/015. This signal is decoded only from A15-A12 without control signals. Refer to "Functional Description" on-chip select signals for further explanation.
/WDTOUT	61(x13), 73(x15)	Out(013/015), Open Drain(C13/C15)	Watch Dog Timer Output signal. Output pulse width depends on the externally connected pin.
/RESET	28(x13), 9(x15)	Input(013/015), I/O (Open Drain) (C13/C15)	Reset signal. /RESET signal is used for initializing MPU and other devices in the system. Also used to return from the steady state in the STOP or IDLE modes.

Note: For the Z84013/Z84015 the /RESET must be kept in active state for a period of at least three system clock cycles.

Note: For the Z84C13/Z84C15, during the power-up sequence, the /RESET becomes an Open drain output and the Z84C13/C15 will drive this pin to "0" for 25 to 75 msec after the power supply passes through approx. 2.2V and then reverts to input. If it receives the /RESET signal after power-on sequence, it will drive /RESET pin for 16-processor clock cycles depending on the status of Reset Output Disable bit in Misc Control Register. If this Reset output is disabled, it must be kept in active state for a period of at least three system clock cycles. Note, that if using Z84C13/C15 in a Z84013/015 socket, modification may be required on the reset circuit since this pin is "pure input pin" on the Z84013/015. Also, the /RESET pin doesn't have internal pull-up resistors and therefore requires external pull-ups. For more details on the device, please refer to "Functional Description."

XTAL1	63(x13), 65(x15)	In	Crystal oscillator connecting terminal. A parallel resonant crystal is recommended. If external clock source is used as an input to the CGC unit, supply clock goes into this terminal. If external clock is supply to CLKIN pin (without CGC unit), this terminal must be connected to "0" or "1".
XTAL2	63(x13), 66(x15)	Out	Crystal oscillator connecting terminal.
CLKIN	67(x13), 69(x15)	In	Single-phase System Clock Input.
CLKOUT	66(x13), 68(x15)	Out	Single-phase clock output from on-chip Clock Generator/Controller.
EV	58(x13), 67(x15)	In	Evaluator signal. When "1" is applied to this pin, IPC is put in Evaluation mode.

Note: For the Z84013/015, together with /BUSREQ, the EV signal puts the IPC into the evaluation mode. When this signal becomes active, the status of /M1, /HALT and /RFSH change to input. When using Z84013/015 as an evaluator chip, the CPU is electrically disconnected after one machine cycle is executed with the EV signal "1" and the /BUSREQ signal "0". It follows the instructions from the other CPU (of ICE). Upon receiving /BUSREQ; A15-A0, /MREQ, /IORQ, /RD and /WR are changed to input and D7-D0 changes its direction. /BUSACK is NOT 3-stated so it should be disconnected by an externally connected circuit. For details, please refer to "Functional Description" on EV mode.

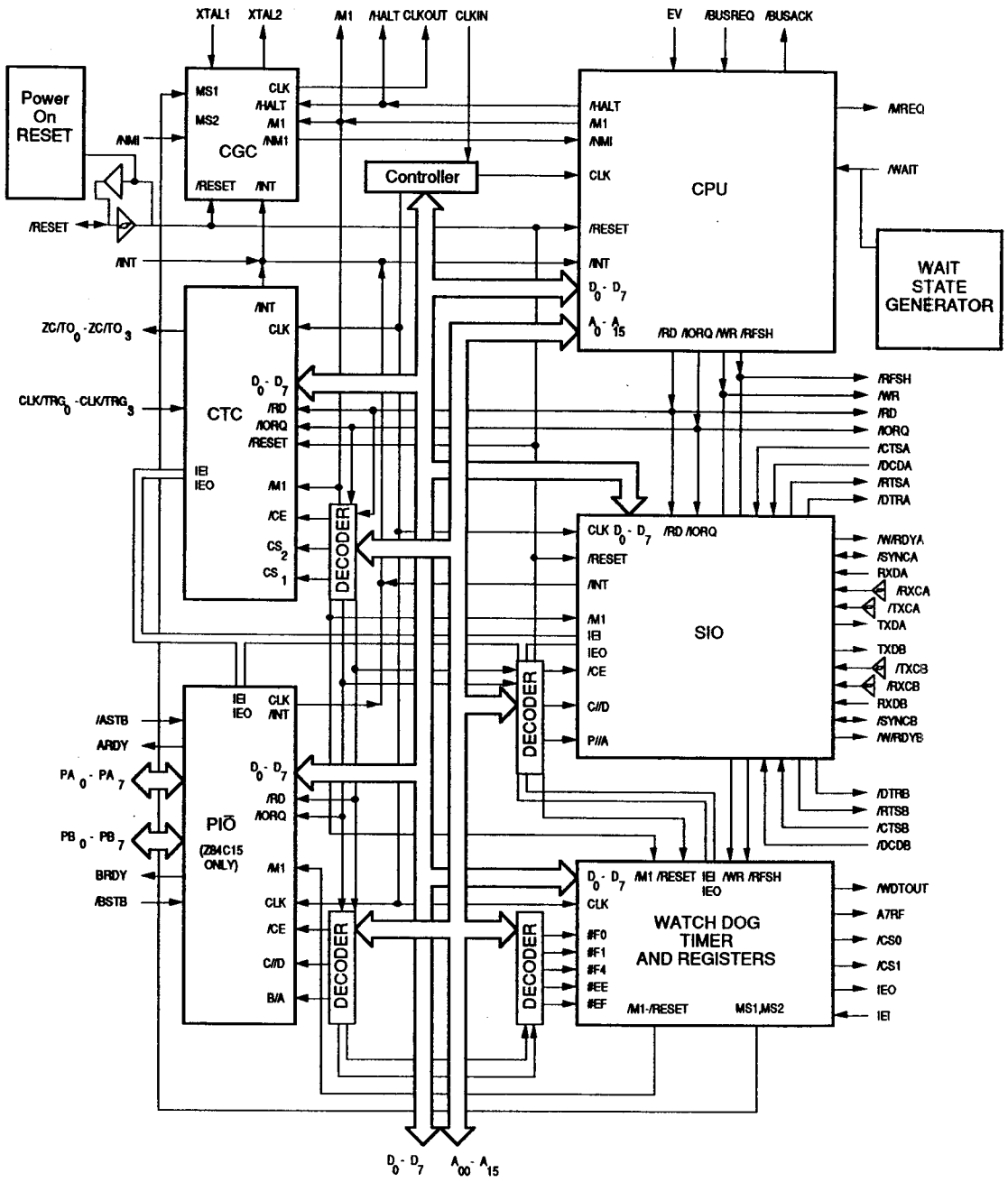


Figure 5(b). Block Diagram for 84C13/C15 IPC

Recommended characteristics of the crystal and the values for the capacitor are as follows (the values will change with crystal frequency).

- Type of crystal: Fundamental, parallel type crystal (AT cut is recommended).
- Frequency tolerance: Application dependent.
- CL, Load capacitance: Approximately 22pf (acceptable range is 20-30pf).
- Rs, equivalent-series resistance: ≤ 150 ohms.
- Drive level: 10mW (for ≤ 10MHz crystal); 5mW (for ≥ 10MHz crystal).
- $C_{IN} = C_{OUT} = 33pF$.

Power-On Reset Logic Unit (Z84C13/C15 Only)
The Z84C13/C15 has the enhanced feature of a Power-on Reset Circuit. During the power-up sequence, the open-drain gate of the on-chip power-on Reset circuit drives /RESET pin to "0" for 25 to 75 msec after the power supply passes through approx. 2.2V. After the termination of the "Power-on Reset" cycle, the open-drain gate of the on-chip Power-on Reset circuit stops to drive the /RESET pin. It is required to have external pull-up register on the /RESET pin.

If it receives /RESET input from outside after the power-on sequence and while the Reset Output Disable bit in Misc Control Register is cleared to "0", it will drive the /RESET pin for 16-processor clock cycles from the falling edge of the external /RESET input. Otherwise, the /RESET pin must be kept in the active state for a period of at least 3 system clock cycles.

If there are power-on reset circuits outside of this device, drive this pin with OPEN-DRAIN type gates with pull-up resisters because /RESET signal is driven low for the period mentioned above during the Power-on sequence. If the external Power-on Reset circuit has push-pull type drivers and they drive the /RESET pin to "1" during that period, it may cause damage. In particular, when using Z84C13/C15 in the Z84013/015 socket, modification may be required on the external reset circuit.

Wait State Generator Unit (Z84C13/C15 Only)
The Z84C13/C15 has the enhanced feature of a Wait State Generator circuit. It is capable of generating /WAIT signals to the CPU internally. The status of the External /WAIT input line is sampled after the insertion of software wait states, except for the wait state's insertion of Interrupt Daisy Chain Wait (for this cycle, insertion of a wait state is not simple).

The Wait State Control Register can be programmed to generate multiple Wait states during different CPU cycles listed as follows.

Memory Wait and Opcode wait. The Wait State Generator can put 0 to 3 wait states in memory accesses. Additionally, one added wait state can be inserted during an /M1 (Opcode fetch) cycle, because /M1 cycle's timing requirement is tighter than memory Read/Write cycles. It generates wait states to the Memory Access in a specified address range, which is programmed in the Memory Wait Boundary Register.

I/O Wait. The Wait State generator can put 0, 2, 4 or 6 wait states in I/O accesses. Regardless of the programming of this field, no I/O wait states are inserted for accesses to on-chip peripherals.

Interrupt Vector Wait. During Interrupt acknowledge cycle, the Wait State Generator can insert one wait state after /IORQ goes active, to extend the time between /IORQ fall to vector fetch by CPU. It allows a slow vector response device.

Interrupt Daisy Chain Wait and RETI sequence extension. During Interrupt acknowledge cycle, the Wait State Generator can insert 0, 2, 4 or 6 wait states between /M1 falling to /IORQ falling edge, to extend the time required to settle daisy chain. This allows a longer daisy chain. Also, this field controls the number of wait states inserted during RETI (Return From Interrupt) cycle. If specified to insert 4 or 6 wait states during Interrupt Acknowledge cycle, Wait State Generator also inserts wait states during RETI fetch sequence. This sequence is generated with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts 2 or 4 wait states, respectively, if op-code followed by EDh is 4Dh. One wait state if the following op-code is not 4Dh.

Chip Select Signals (Z84C13/C15 Only)
The Z84C13/C15 has an enhanced feature of adding two chip select (/CS0, /CS1) pins. Both signals are originally IC test pins (ICT) on the Z84013/015. The boundary value for each Chip Select Signal is 4 bits wide, and compare with A15-A12 of the address. Each Chip Select Signal goes active when:

/CS0: (D3-D0 of CSBR) ≥ A15-A12 ≥ 0
/CS1: (D7-D4 of CSBR) ≥ A15-A12 > (D3-D0 of CSBR)

(Where CSBR is the contents of Chip Select Boundary Register.)

There is also a separate /CS enable bit. /CS0 is enabled on power-up with a boundary value of "F" causing /CS0 to go active for all memory accesses. /CS1 is disabled on

Table 1. I/O Control Register Address

Address	Device	Channel	Register
10h	CTC	Ch 0	Control Register
11h	CTC	Ch 1	Control Register
12h	CTC	Ch 2	Control Register
13h	CTC	Ch 3	Control Register
18h	SIO	Ch. A	Data Register
19h	SIO	Ch. A	Control Register
1Ah	SIO	Ch. B	Data Register
1Bh	SIO	Ch. B	Control Register
1Ch	PIO	Port A	Data Register (Not with Z84x13)
1Dh	PIO	Port A	Command Register (Not with Z84x13)
1Eh	PIO	Port B	Data Register (Not with Z84x13)
1Fh	PIO	Port B	Command Register (Not with Z84x13)
F0h	Watch-Dog Timer		Master Register (WDTMR)
F1h	Watch-Dog Timer		Control Register (WDTCR)
F4h	Interrupt Priority Register		
EEh			System Control Register Pointer (SCRP) (Not with Z84013/015)
EFh			System Control Data Port (SCDP) (Not with Z84013/015)
	Through SCRP and SCDP		Control Register 00 - Wait State Control register (WCR) Control Register 01 - Memory Wait state Boundary Register (MWBR)
			Control Register 02 - Chip Select Boundary Register (CSBR) Control Register 03 - Misc. Control Register (MCR)

PIO REGISTERS

For more detailed information, please refer to the PIO Technical Manual. These registers are not in the Z84x13.

Interrupt Vector Word
The PIO logic unit is designed to work with the Z80 CPU in interrupt Mode 2. The interrupt word must be programmed if interrupts are used. Bit D0 must be a zero (Figure 11).

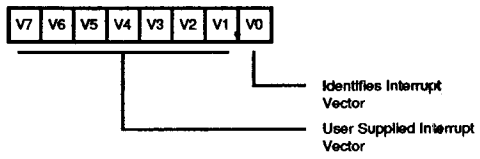


Figure 11. PIO Interrupt Vector Word

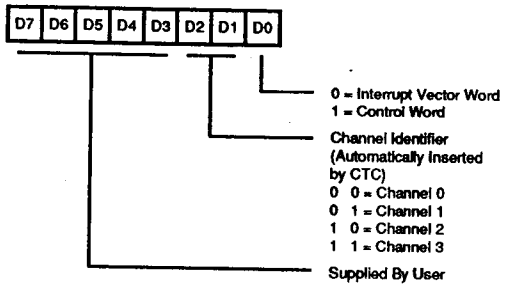


Figure 19. CTC Interrupt Vector Word

SIO REGISTERS

For more detailed information, refer to the SIO Technical Manual.

Read Registers. The SIO channel B contains three read registers while channel A contains only two that are read to obtain status information. To read the contents of a register (rather than RR0), the program must first write a pointer to WR0 in exactly the same manner as a write operation. The next I/O read cycle will place the contents of the selected read registers onto the data bus (Figure 20a, b, c).

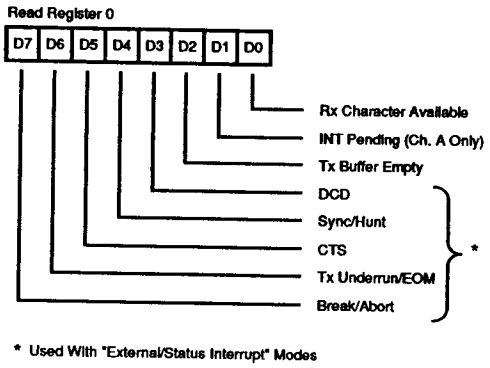


Figure 20a. SIO Read Register 0

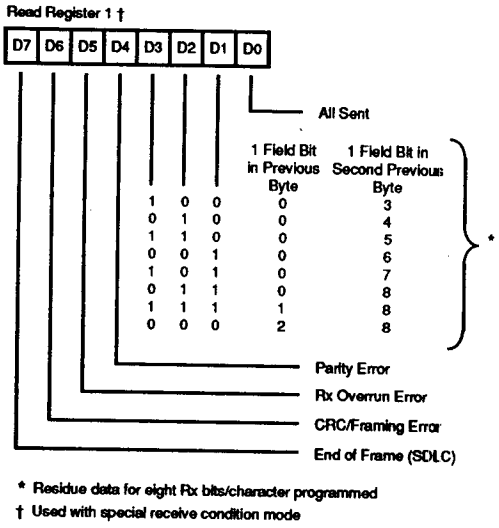


Figure 20b. SIO Read Register 1

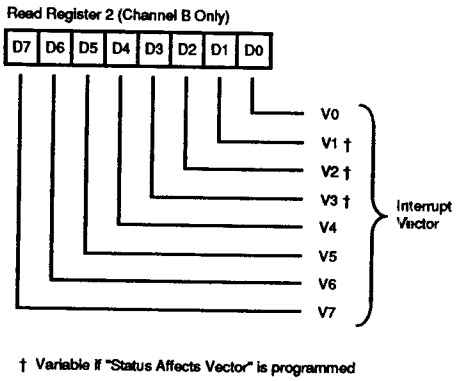


Figure 20c. SIO Read Register 2

Write Registers. The SIO Channel B contains eight write registers while Channel A contains only seven that are programmed to configure the operating mode characteristics of each channel. With the exception of WR0, programming the write registers is a two step operation. The first operation is a pointer written to WR0 which points to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel (Figure 21).

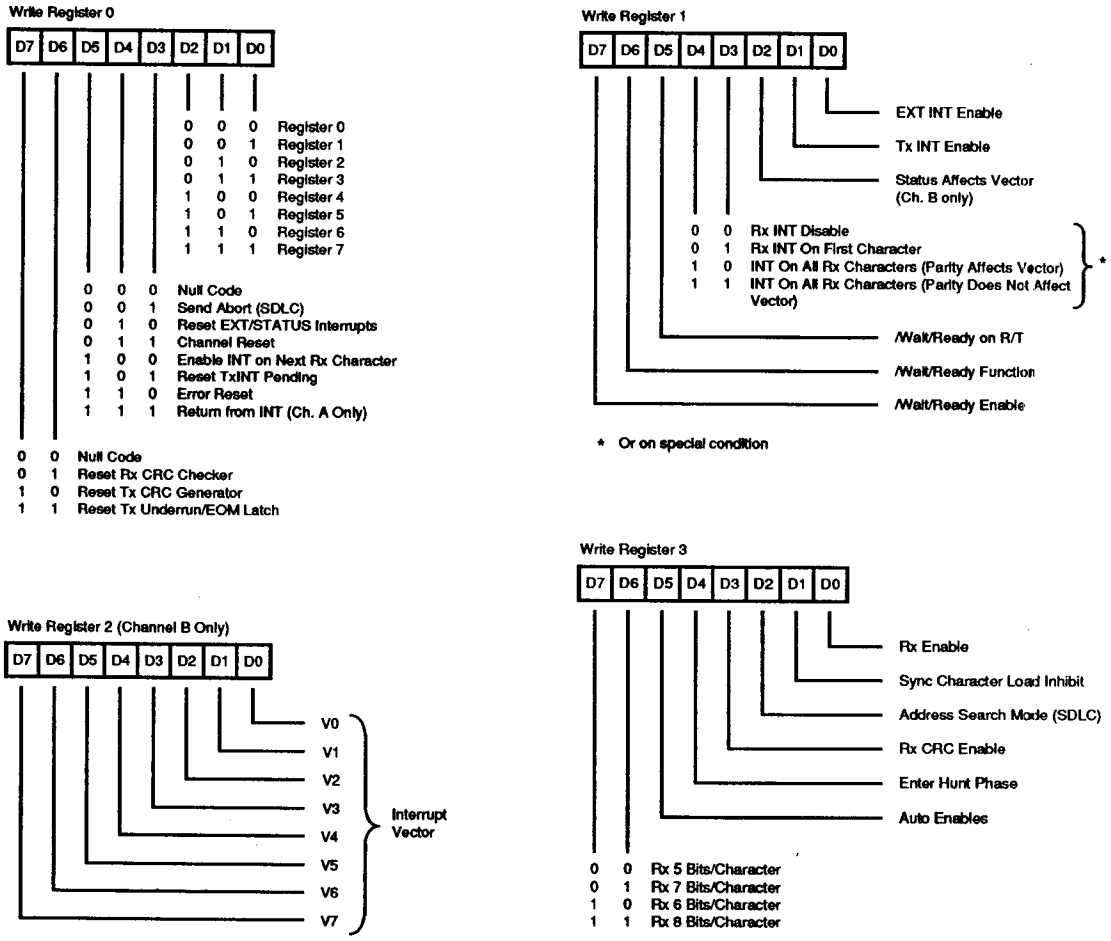


Figure 21. SIO Write Registers

Clearing the WDT. The WDT can be cleared by writing "4Eh" into the WDTCR.

Watch Dog Timer Master Register (WDTMR;I/O address F0h). This register controls the activities of the Watch Dog Timer and selects power-down mode of operation (Figure 22).

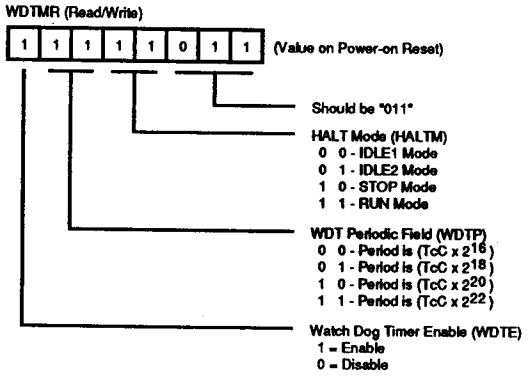


Figure 22. Watch Dog Timer Master Register

Bit D7. *Watch Dog Timer Enable* (WDTE). This bit controls the activities of Watch Dog Timer. The WDT can be enabled by setting this bit to "1". To disable WDT, write "0" to this bit followed by writing "B1h" in the WDT Command Register. Watch Dog Timer Logic has a "double key" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop, due to program run-away. Upon Power-on reset, this bit is set to "1" and the WDT is enabled.

Bit D6-D5. *WDT Periodic field* (WDTP). This two bit field determines the desired time period. Upon Power-on reset, this field sets to "11".

00 - Period is (TcC * 2^{16})
01 - Period is (TcC * 2^{18})
10 - Period is (TcC * 2^{20})
11 - Period is (TcC * 2^{22})

Bit D4-D3. *HALT mode* (HALTM). This two bit field specifies one of four power-down modes. To change this field, write "DBh" to the WDT command register, followed by a write to this register. For detailed descriptions of this field, please refer to the section "Mode of operations." Upon Power-on Reset, this field is set to 11, which specifies "RUN mode."

00 - IDLE 1 Mode
01 - IDLE 2 Mode
10 - STOP Mode
11 - RUN Mode

Bit D2-D0. *Reserved.* These three bits are reserved and should always be programmed as "011". A read to these bit returns "011".

Watch Dog Timer Command Register (WDTCR; I/O address F1h). In conjunction with the WDTMR, this register works as a "Second key" for the Watch Dog Timer. This register is write only (Figure 23).

Write B1h after clearing WDTE to "0" - Disable WDT.
Write 4Eh - Clear WDT.
Write DBh followed by a write to HALTM - Change Power-down mode.

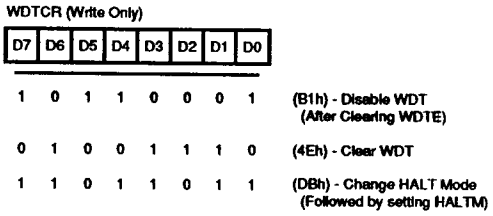


Figure 23. Watch Dog Timer Command Register

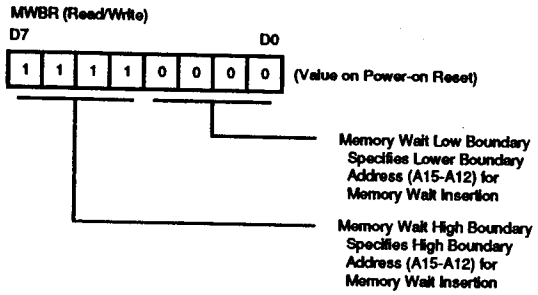


Figure 28. Memory Wait Boundary Register

Bit D7-D4. *Memory Wait High Boundary.* This field specifies A15-A12 of the upper address boundary for Memory Wait.

Bit D3-D0. *Memory Wait Low Boundary.* This field specifies A15-12 of the lower address boundary for Memory Wait.

Memory Wait states are inserted for the address range:

(D7-D4 of MWBR) ≥ A15-A12 ≥ (D3-D0 of MWBR)

This register is set to "F0h" on Power-on Reset, which specifies the address range for Memory Wait as "0000h to FFFFh".

Chip Select Boundary Register (CSBR, Control Register 02h)

This register specifies the address range for each chip select signal. When accessed memory addresses are within this range, chip select signals are active (Figure 29).

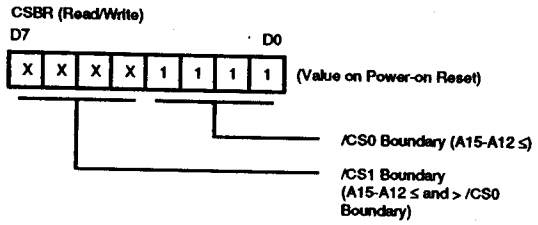


Figure 29. Chip Select Boundary Register

D7-D4. */CS1 Boundary Address.* These bits specify the boundary address range for /CS1. The bit values are ignored on power-up as the /CS1 enable bit is off. The /CS1 is asserted if the address lines A15-12 have an address value greater than the programmed value for /CS0, and less than or equal to the programmed value in these bits.

D3-D0. */CS0 Boundary Address.* These bits specify the boundary address range for /CS0. /CS0 is asserted if the address lines A15-12 have an address value less than or equal to the programmed boundary value. The /CS0 enable bit in the MCR must be set to 1. Upon Power-up reset, these bits come up as all 1's so that /CS0 is asserted for all addresses.

Chip Select signals are active for the address range:

/CS0: (D3-D0 of CSBR) ≥ A15-A12 ≥ 0
/CS1: (D7-D4 of CSBR) ≥ A15-A12 > (D3-D0 of CSBR)

This register is set to "xxxx1111b" on Power-on Reset, which specifies the address range of /CS0 for "0000h to FFFFh" (all Memory location) and /CS1 "undefined."

Misc Control Register (MCR, Control Register 03h)

This register specifies miscellaneous options on this device (Figure 30).

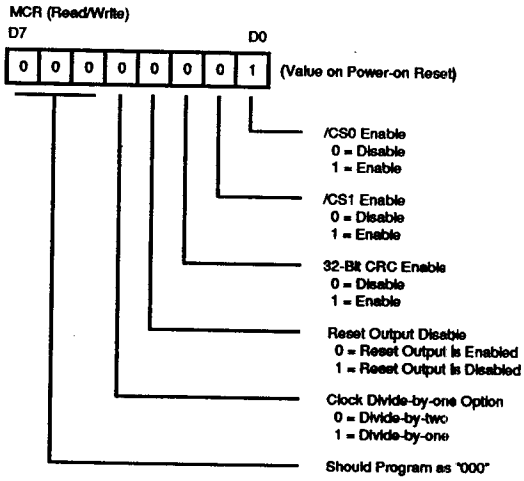


Figure 30. Misc Control Register

Bit D7-D5. *Reserved.* These three bits are reserved and are always programmed as "000".

Bit D4. *Clock Divide-by-one option.* "0"-Disable, "1"-enable. On-chip CGC unit has divide-by-two circuit. By setting this bit to one, this circuit is bypassed and CLKOUT is equal to X'tal oscillator frequency (or external clock input on the XTAL1 pin). This bit has no effect when the on-chip CGC unit is not in use and the external system clock is fed from CLKIN pin. Upon Power-on Reset, this bit is cleared to 0 and the clock is divided by two.

Table 3. Device status in Halt state
(When using on-chip CGC unit; CLKOUT and CLKIN are tied together)

Mode	CGC	CPU	CTC	PIO	SIO	WDT	CLKOUT
IDLE1	O	X	X	X	X	X	X
IDLE2	O	X	O	X	X	X	O
STOP	X	X	X	X	X	X	X
RUN	O	O	O	O	O	O	O

O: Operating
X: Stop

All of the operating modes listed here are valid with crystal input (Crystal connected between XTAL1/2 or external clock input on XTAL1). For the external clock on the CLKIN pin, only the IDLE2 and RUN modes are applicable.

TIMING

Basic Timing

The basic timing is explained here with emphasis placed on the halt function relative to the clock generator. The following items are identical to those for the Z84C00. Refer to the data sheet for the Z84C00.

- Operation code fetch cycle
- Memory Read/Write operation
- Input/Output operation
- Bus request/acknowledge operation
- Maskable interrupt request operation
- Non-Maskable interrupt request operation
- Reset Operation

Operation When HALT Instruction is Executed. When the CPU fetches a halt instruction in the operation code fetch cycle, /HALT goes active (Low) in synch with the falling edge of T4 state before the peripheral LSI and CPU stops the operation. After this, the system clock generation differs depending upon the operation mode (RUN Mode, IDLE1/2 Mode or STOP Mode). If the internal system clock is running, the CPU continues to execute NOP instruction even in the halt state.

RUN Mode (HALTM = 11). Shown in Figure 31 is the basic timing when the halt instruction is executed in RUN Mode.

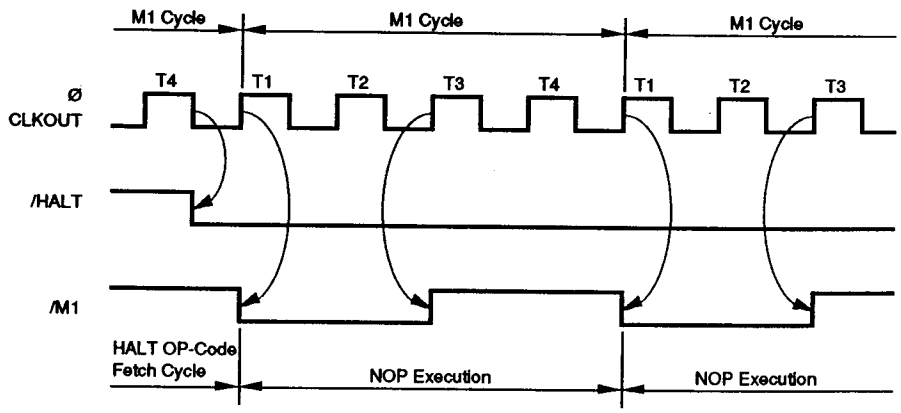


Figure 31. Timing of RUN Mode
(at Halt Instruction Command Execution)

In IDLE2 Mode, the internal oscillator and clock output (CLKOUT) continue to operate. The internal system clock, fed from CLKIN to the components other than CTC is stopped at the T4 Low state of HALT instruction execution.

STOP Mode (HALTM=10). Shown in Figure 34 is the basic timing when the halt instruction is executed in STOP Mode.

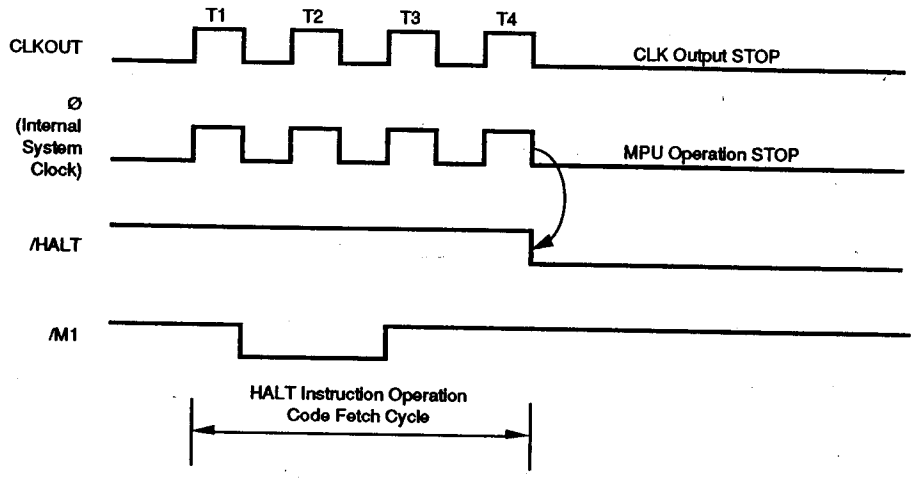


Figure 34. STOP Mode Timing
(At Halt Instruction Execution)

In STOP Mode, the on-chip CGC unit is stopped at T4 Low state of HALT instruction execution. Therefore, clock output (CLKOUT), operation of Watch Dog Timer, CPU, PIO, CTC, SIO are stopped.

Release from Halt State. The halt state of the CPU is released when "0" is input to the /RESET signal and the MPU is reset or an interrupt request is accepted. An interrupt request signal is sampled at the leading edge of the last clock cycle (T4 state) of NOP instruction. In case of the maskable interrupt, interrupt will be accepted by an active /INT signal ("0" level). Also, the interrupt enable flip-flop is set to "1". The accepted interrupt process is started from the next cycle.

Further, when the internal system clock is stopped (IDLE1/2 Mode, STOP Mode), it is necessary first to restart the internal system clock. The internal system clock is restarted when /RESET or interrupt signal (/NMI or /INT) is asserted.

RUN Mode (HALTM=11). The halt release operation is enabled by interrupt request in RUN Mode (Figure 35).

Z84C13/C15 Only. The /RESET pulse is stretched to a minimum of 16 cycles and driven out of the Z84C13/C15 on the /RESET pin if Reset output is enabled (bit D3 of MCR is cleared to "0"). Setting bit D3 disables the driving out of /RESET. The values in the control registers (WDTMR, SCRP, WCR, MWBR, CSBR and MCR) are initialized to the default value on /RESET.

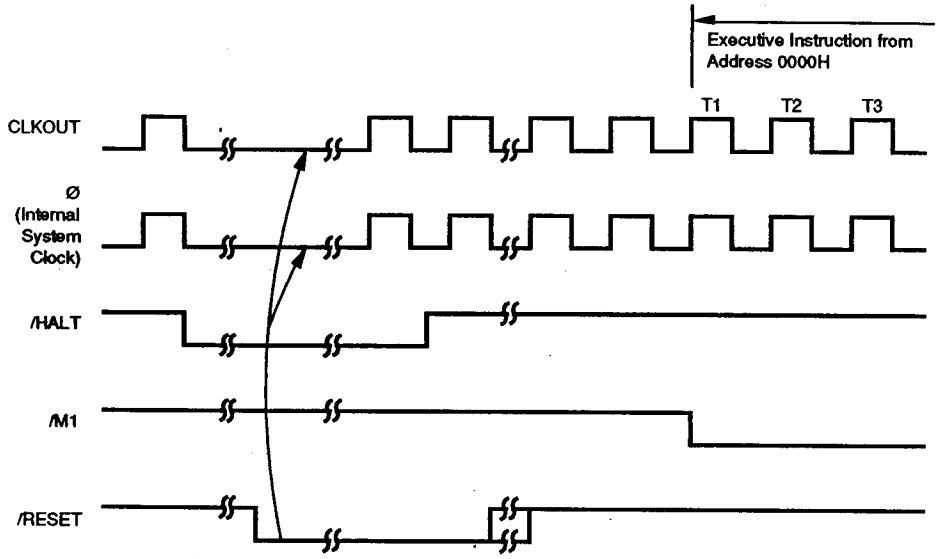


Figure 40. Halt Release Operation Timing By Reset in STOP Mode

Start-up Time at Time of Restart (STOP Mode). When the MPU is released from the halt state by accepting an interrupt request, it executes an interrupt service routine. Therefore, when an interrupt request is accepted, it starts generating clock on the CLKOUT pin, after a start-up time, by the internal counter [(2^{14}+2.5) TcC (TcC:Clock Cycle)]. This obtains a stabilized oscillation for operation.

Further, in case of restart by the /RESET signal, the internal counter does not operate.

Evaluation operation. Each of the CPU signals (A15-0, D7-0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1, /RFSH) can be 3-stated by activating the EV pin. The Z84C13/C15 enhances the counter part by eliminating the requirement of /BUSREQ to go active.

Instruction set. The instruction set of the IPC is the same for the Z84C00. For details, refer to the data sheet of the Z84C00 Technical Manual.

AC TIMING

The following section describes the timing of the IPC. The numbers appearing in the figures refer to the parameters on Table A - F.

CPU Timing
Parameters referenced in Figure 41 through Figure 48 appear in Table A.

The IPC's CPU executes instructions by proceeding through the following specific sequence of operations:

Memory read or write
I/O device read or write
Interrupt acknowledge

The basic clock period is referred to as a Time or Cycle and three or more T cycles make up a machine cycle (e.g., M1, M2 or M3). Machine cycles are extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

Memory Read or Write Cycles. Figure 42 shows the timing of memory read or write cycles other than an Op-code fetch (/M1) cycle. The /MREQ and /RD signals function like the Op-code fetch cycle.

In a memory write cycle, /MREQ also becomes active when the Address Bus is stable. The /WR line is active when the Data Bus is stable, so that it can be used directly as an R/W pulse to most semiconductor memories.

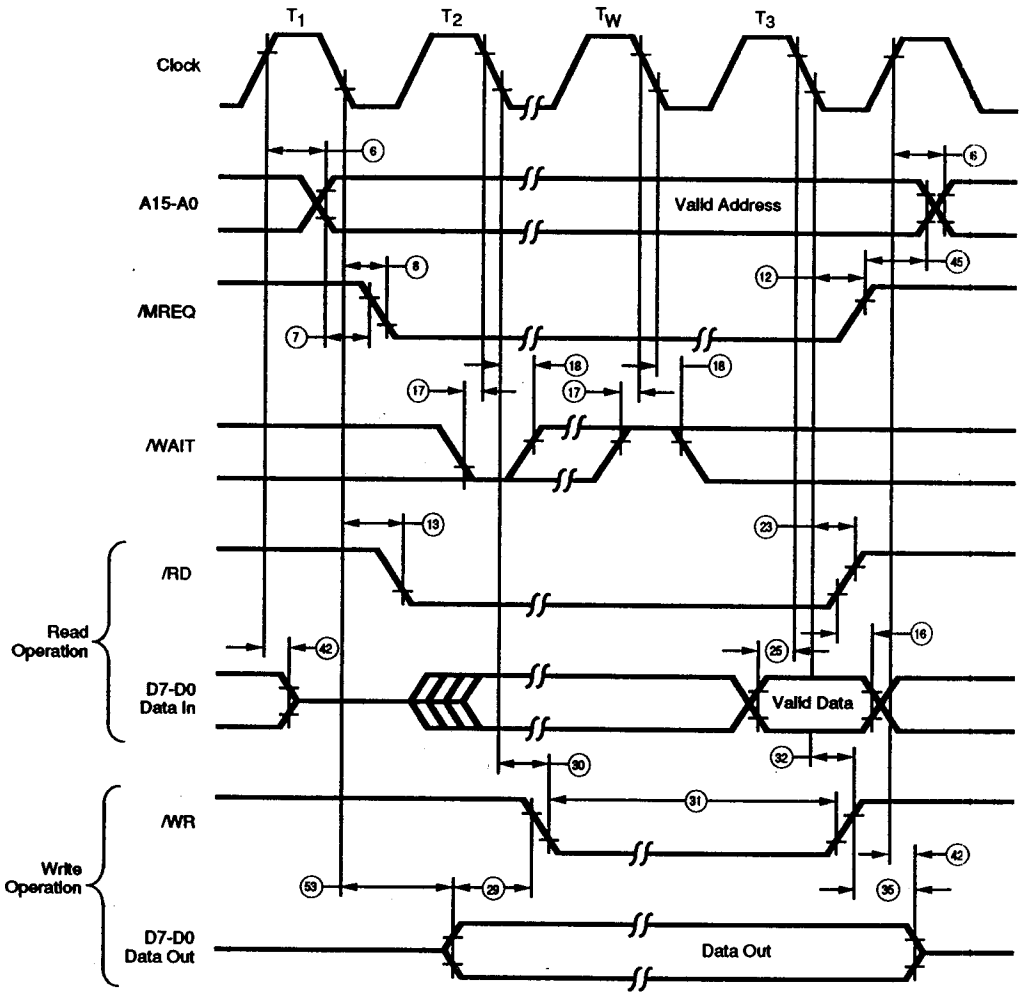
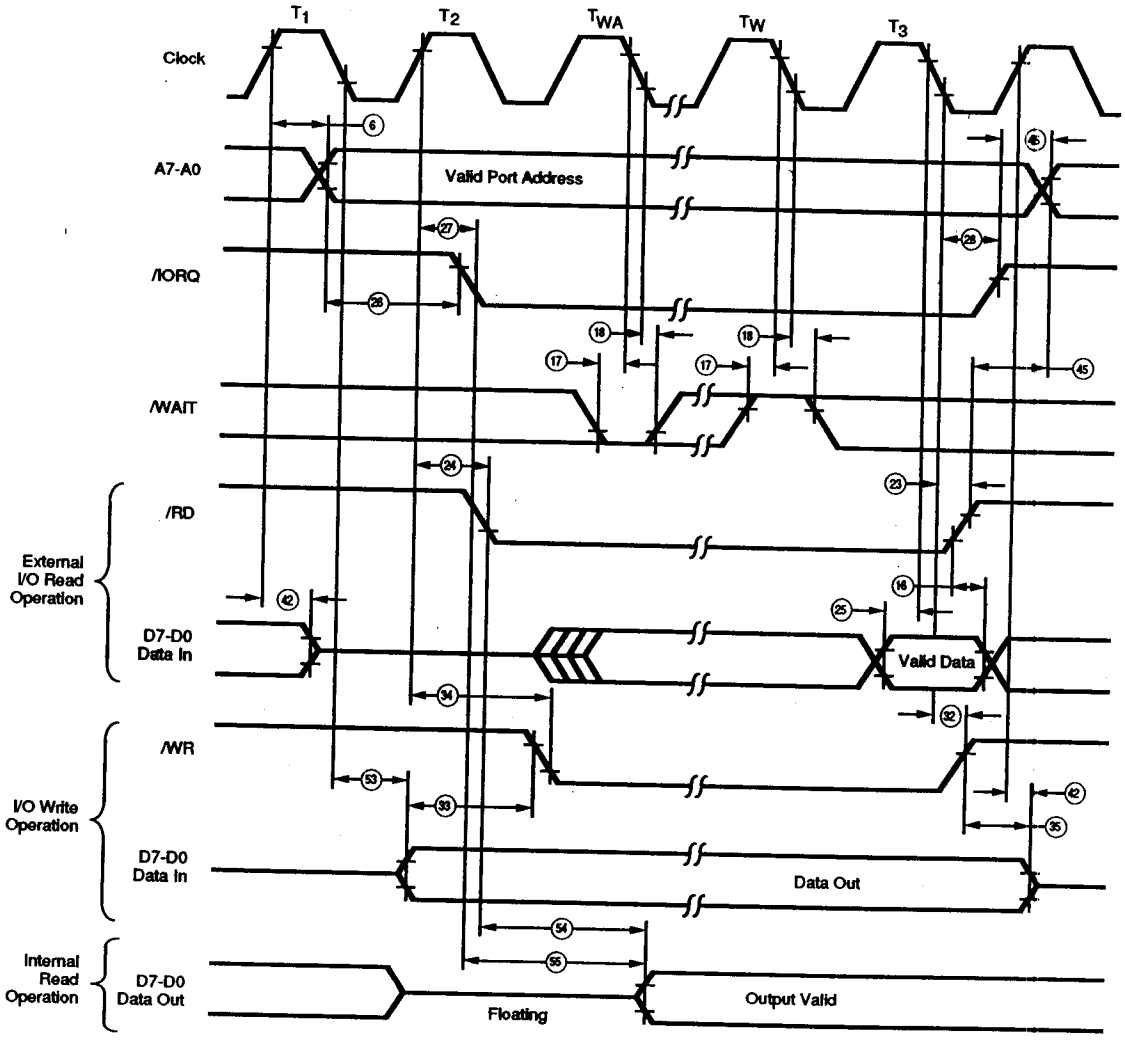


Figure 42. Memory Read or Write Cycle
(See Table A)

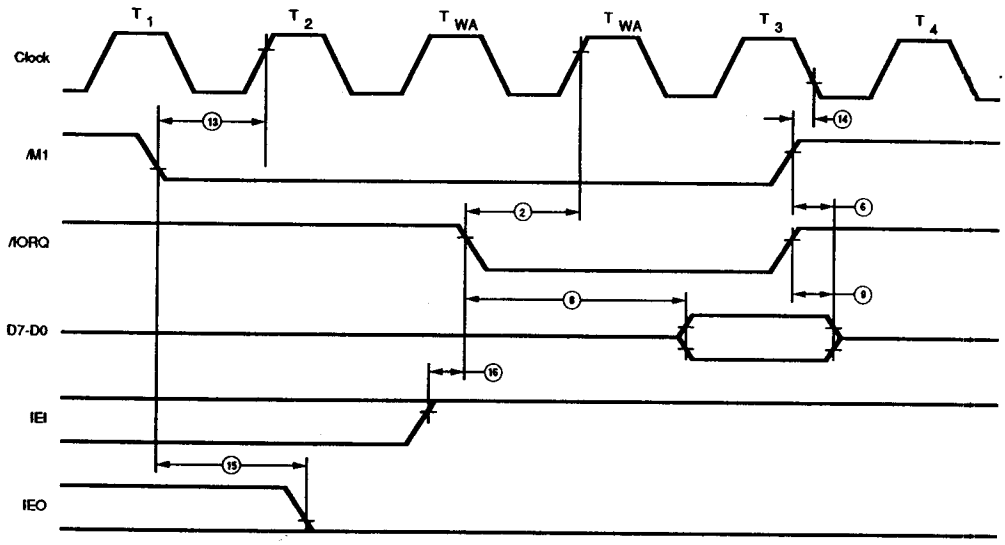
Input or Output Cycles. Figure 43 shows the timing for an I/O read or I/O write operation. During I/O operations, the CPU automatically inserts a single Wait state (T_{WA}). This extra Wait state allows sufficient time for an I/O port to decode the address from the port address lines.

When the CPU is accessing the on-chip I/O registers (PIO, CTC, SIO and system control registers), the data from/to these registers also appears on the data bus, or data bus is output during I/O cycle.

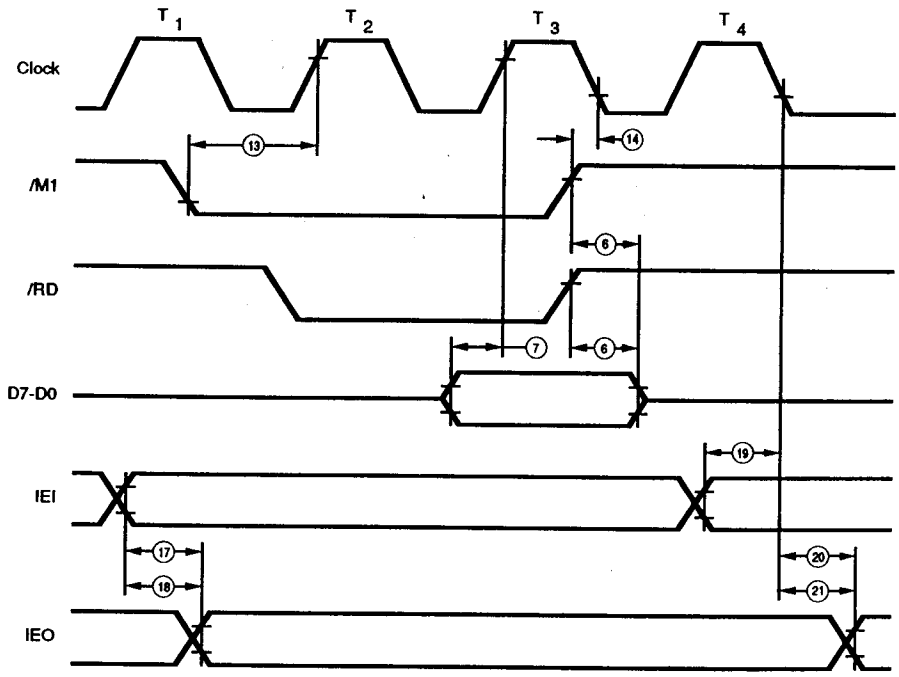


Note: T_{WA} = One wait cycle automatically inserted by CPU

Figure 43. Input or Output Cycle
(See Table A)



(b) Interrupt Acknowledge Cycle Timing for On-chip peripheral from External Bus master
(See Table C)



(c) Op-code fetch Cycle Timing for On-chip peripheral from External Bus master
(See Table C)

Figure 53. On-chip Peripheral Timing from External Bus master (Continued)

SIO Timing

Figure 56 shows the timing for on-chip SIO.

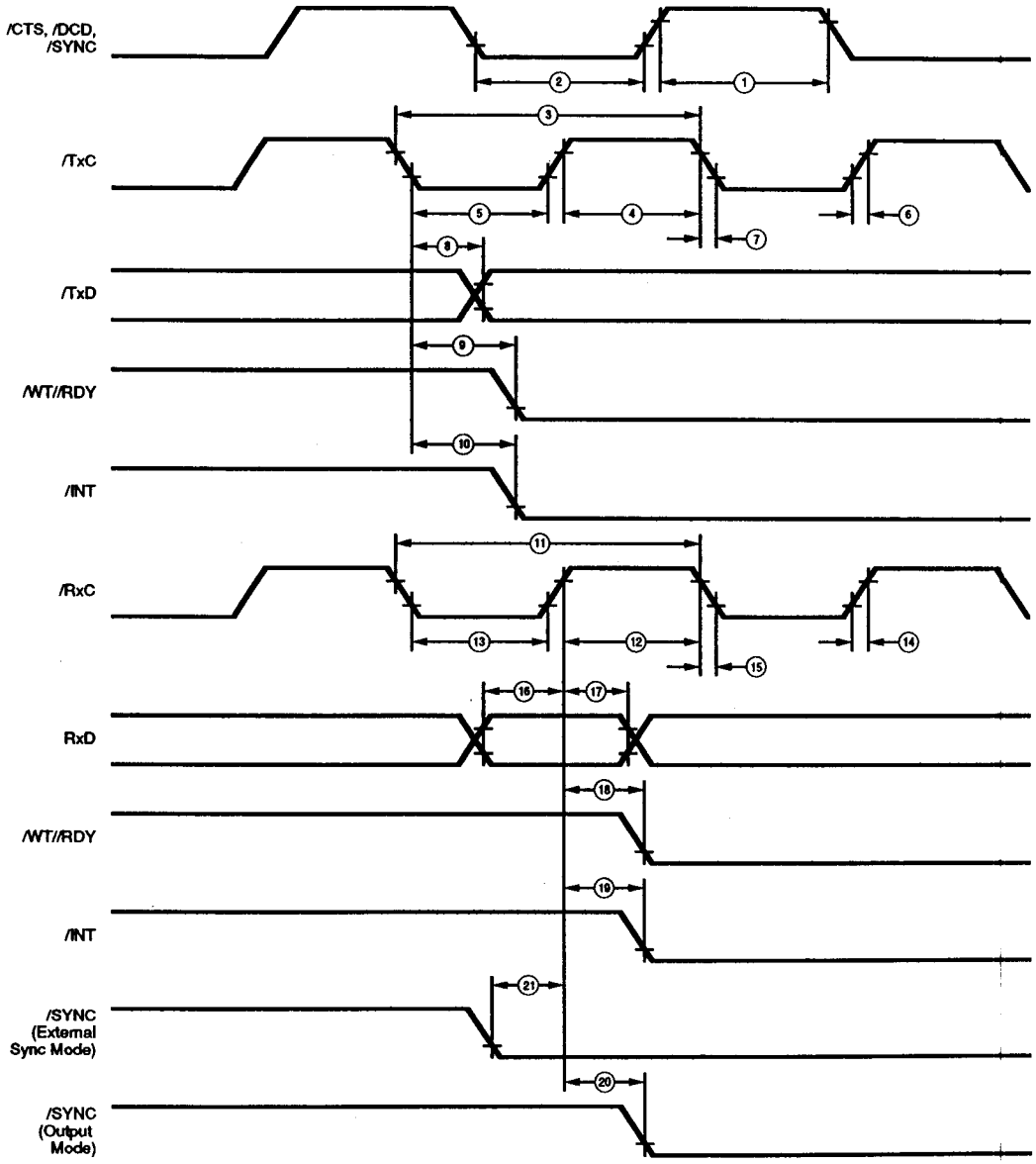


Figure 56. SIO Timing
(See Table F)

Watch-Dog Timer Timing
Figure 57 shows the timing for Watch-dog Timer.

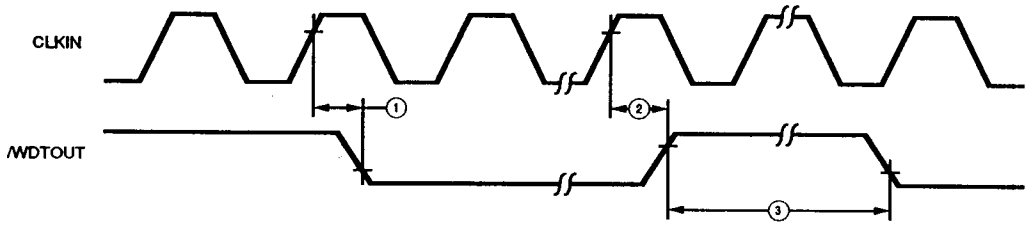


Figure 57. Watch-dog Timer Timing (See Table H)

PRECAUTIONS

(1) To release the HALT state by /RESET signal in STOP Mode, hold the /RESET signal at "0" until the output from the internal oscillator stabilizes.

Z84013/015 Only. To reset MPU, it is necessary to hold /RESET signal input at "0" level for at least three clocks.

Z84C13/C15 Only. If Reset output is disabled, /RESET must be active for at least three clock cycles for the CPU to properly accept it. Otherwise, the on-chip reset circuit extends /RESET signal to at least a minimum of 16-clock cycles.

(2) Releasing the MPU from the HALT state by the interrupt signal in IDLE1/2 Mode and STOP Mode, depends upon the HALT state and the internal system clock. They will stop unless an interrupt signal is accepted during the execution of NOP instruction, even when the internal system clock is restarted by the interrupt signal input. In particular, care must be taken when /INT is used.

Other precautions are identical to those for the Z84C00. Refer to the data sheet for the Z84C00.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage on Vcc with respect to Vss .....-0.3V to +7.0V
Voltages on all inputs
with respect to Vss .....-0.3V to Vcc+0.3V
Operating Ambient
Temperature .....See Ordering Information
Storage Temperature .....-65 °C to + 150 °C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS (Continued)

Table A. CPU Timing (Continued)

No	Symbol	Parameter	Z84X1306 Z84X1506 Min	Z84X1306 Z84X1506 Max	Z84X1310 Z84X1510 Min	Z84X1310 Z84X1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
41	TdCf(BUSACKr)	Clock Fall to /BASACK Rise Delay		90		75		40	ns	
42	TdCr(Dz)	Clock Rise to Data Float Delay		80		65		40	ns	
43	TdCr(CTz)	Clock Rise to Control Outputs Float Delay (/MREQ, /IORQ, /RD and /WR)		70		65		40	ns	
44	TdCr(Az)	Clock Rise to Address Float Delay		80		75		40	ns	
45	TdCTr(A)	Address Hold Time from /MREQ, /IORQ, /RD or /WR	35**		20**			0	ns	
46	TsRESET(Cr)	/RESET to Clock Rise Setup Time	60		40		15		ns	
47	ThRESET(Cr)	/RESET to Clock Rise Hold Time	10		10		10		ns	
48	TsINTf(Cr)	/INT Fall to Clock Rise Setup Time	70		50		15		ns	
49	ThINTr(Cr)	/INT Rise to Clock Rise Hold Time	10		10		10		ns	
50	TdM1f(IORQf)	/M1 Fall to /IORQ Fall Delay	359**		220**		100		ns	
51	TdCf(IORQf)	Clock Fall to /IORQ Fall Delay		70		55		45	ns	
52	TdCf(IORQr)	Clock Rise to /IORQ Rise Delay		70		55		45	ns	
53	TdCf(D)	Clock Fall to Data Valid Delay		130		110		75	ns	
54	TRDf(D)	/RD Fall to Output Data Valid		TBD		60		40	ns	
55	TdIORQ(D)	/IORQ Fall to Output Data Valid		TBD		70		45	ns	
56	TwRESET	/RESET Pulse Width 013/015, or C13/C15 with RESET Output Disabled	3TcC		3TcC		3TcC		ns	
57	TwRESEToe	/RESET Pulse Width RESET Output Enabled	2TcC		2TcC		2TcC		ns	
58	TwRESETdo	/RESET Drive Duration RESET Output Enabled	16TcC		16TcC		16TcC		ns	
59	TwRESETpor	/RESET drive duration on Power-On Sequence	10	75	10	75	10	75	ms	

Notes:

* 16 MHz Timings are preliminary and subject to change. Only C version

** For clock period other than the minimum shown, calculate parameters using the formula on Table H.

[A1] These parameters apply to the external Clock input on CLKIN pin. For the cases where external Clock is fed from XTAL1, please refer to Table B.

[A2] For loading >= 50 pF, decrease width by 10 ns for each additional 50 pF.

Table C. Timing for on-chip peripheral access from external bus master and daisy chain timing (See Figure 53(a))

No	Symbol	Parameter	Z84C1306 Z84C1506 Min	Z84C1306 Z84C1506 Max	Z84C1310 Z84C1510 Min	Z84C1310 Z84C1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
1	TsA(Rlf)	Address Setup Time to /RD, /IORQ Fall	50		40		30		ns	
2	TsRI(Cr)	/RD, /IORQ Rise to Clock Rise Setup	60		50		40		ns	
3	Th	Hold time for Specified Setup	15		15		10		ns	
4	TdCr(DO)	Clock Rise to Data out delay		100		80	60		ns	
5	TdRIr(DOz)	/RD, /IORQ Rise to Data Out Float Delay		75		60	50		ns	
6	ThRDr(D)	/M1, /RD, /IORQ Rise to Data Hold	15	40	15	30		20	ns	[C1]
7	TsD(Cr)	Data In to Clock Rise Setup Time	30		25		15		ns	
8	TdIOf(DOI)	/IORQ Fall to Data Out Delay (INTACK cycle)		95		95	70		ns	
9	ThIOr(D)	/IORQ Rise to Data Hold	15		15		10		ns	
10	ThIOr(A)	/IORQ Rise to Address Hold	15		15		10		ns	
11	TsWIf(Cr)	/IORQ, /WR setup time to Clock Rise New parameter	20		20		15		ns	[C2]
12	ThWRr(Cr)	Clock Rise to /IORQ, /WR Rise hold time	0		0		0		ns	[C2]
13	TsM1f(Cr)	/M1 Fall to Clock Rise Setup Time	40		40		15		ns	
14	TsM1r(Cf)	/M1 Rise to Clock Rise Setup Time (/M1 cycle)	-15		-15		-10		ns	
15	TdM1f(IEOf)	/M1 Fall to IEO Fall delay (Interrupt Immediately Preceding /M1 Fall)		140		80		60	ns	
20	TdCf(IEOr)	Clock Fall to IEO Rise Delay	50		40			30	ns	
21	TdCf(IEOf)	Clock Fall to IEO Rise Delay		90		75		50	ns	

Notes:
[C1] For I/O write to PIO, CTC and SIO.
[C2] For I/O Write to system control registers.
[C3] For daisy-chain timing, please refer to the note on Page 356.

AC CHARACTERISTICS (Continued)

Table D. PIO Timing (Z84x15 only) (See Figure 54)

No	Symbol	Parameter	Z84C1506 Min	Z84C1506 Max	Z84C1510 Min	Z84C1510 Max	Z84C1516* Min	Z84C1516* Max	Unit	Note
1	TslOr(Cr)	/IORQ Rise to Clock Fall Setup Time (To Activate RDY on Next Clock Cycle)	100		100		100		ns	
2	TdCf(RDYr)	Clock Fall to RDY Rise Delay		100		115		30	ns	[D2]
3	TdCf(RDYf)	Clock Fall to RDY Fall Delay		100		115		30	ns	[D2]
4	TwSTB	/STB Pulse Width	100		80		50		ns	[D1]
5	TsSTBr(Cr)	/STB Rise to Clock Fall Setup Time (To Activate RDY on Next Clock Cycle)	100		100		70		ns	[D2]
6	TdIOr(PD)	/IORQ Rise to Port Data Stable Delay (Mode 0)		140		120		100	ns	[D2]
7	TsPD(STBr)	Port Data to /STB Rise Setup Time (Mode 1)	140		75		30		ns	
8	ThPD(STBr)	Port Data to /STB Rise Hold Time (Mode 1)	15		15		15		ns	
9	TdSTBf(PD)	/STB Fall to Port Data Stable (Mode 2)		150		120		30	ns	[D2]
10	TdSTBr(PDz)	/STB Rise to Port Data Float Delay (Mode 2)		140		120		50	ns	
11	TdPD(INTf)	Port Data Match to /INT Fall Delay (Mode 3)		250		200		40	ns	
12	TdSTBr(INTf)	/STB Rise to /INT Fall Delay		290		220		75	ns	

Notes:
[D1] For Mode 2: TwSTB >TsPD(STB).
[D2] Increase these values by 2 ns for 10 pF increase in loading up to 100 pF Max.

Table E. CTC Timing (Figure 55)

No	Symbol	Parameter	Z84C1306 Z84C1506 Min	Z84C1306 Z84C1506 Max	Z84C1310 Z84C1510 Min	Z84C1310 Z84C1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
1	TdCr(INTf)	Clock Rise to /INT Fall Delay		(TcC+100)		(TcC+80)		(TcC+30)		[E1]
2	TsCTR(Cc)	CLK/TRG to Clock Rise Setup Time for Immediate Count	90		90		40		ns	[E2]
3	TsCTR(Ct)	CLK/TRG to Clock Rise Setup Time for Enabling of Prescalor on Following Clock Rise	90		90		40		ns	[E1]
4	TdCTR(INTf)	CLK/TRG to /INT Fall Delay TsCTR(C) Satisfied		(1)+(3)		(1)+(3)		(1)+(3)	ns	[E2]
		TsCTR(C) not Satisfied		TcC+(1)+(3)		TcC+(1)+(3)		TcC+(1)+(3)	ns	[E2]
5	TcCTR	CLK/TRG Cycle time	(2TcC)	DC	(2TcC)	DC	(2TcC)	DC	ns	[E3]
6	TwCTRh	CLK/TRG Width (Low)	90	DC	90	DC	25	DC	ns	
7	TwCTRl	CLK/TRG Width (High)	90	DC	90	DC	25	DC	ns	
8	TrCTR	CLK/TRG Rise Time		30		30		15	ns	
9	TfCTR	CLK/TRG Fall Time		30		30		15	ns	
10	TdCr(ZCr)	Clock Rise to ZC/TO Rise Delay		80		80		25	ns	
11	TdCf(ZCf)	Clock Fall to ZC/TO Fall Delay		80		80		25	ns	

Notes:
[E1] Timer Mode.
[E2] Counter Mode.
[E3] Counter Mode only; when using a cycle time less than 3TcC, parameter #2 must be met.