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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	Z80
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	6MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z84c1506fec">https://www.e-xfl.com/product-detail/zilog/z84c1506fec</a>



Figure 1. Z84013/015 Version



Figure 2. Z84C13/C15 Version



\* ICT for the Z84013

Figure 3. Z84013/Z84C13 Pin-out Assignments

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**CPU SIGNALS**

Pin Name	Pin Number	Input/Output, 3-State	Function
A0-A15	16-1(x13), 6-1, 100-91(x15)	I/O	16-bit address bus. Specifies I/O and memory addresses to be accessed. During the refresh period, addresses for refreshing are output. The bus is an input when the external master is accessing the on-chip peripherals.
D0-D7	83-76(x13), 89-82(x15)	I/O	8-bit bidirectional data bus. When the on-chip CPU is accessing on-chip peripherals, these lines are set to output and hold the data to/from on-chip peripherals.
/RD	30(x13), 14(x15)	I/O	Read signal. CPU read signal for accepting data from memory or I/O devices. When an external master is accessing the on-chip peripherals, it is an input signal.
/WR	20(x13), 13(x15)	I/O	Write Signal. This signal is output when data, to be stored in a specified memory or peripheral LSI, is on the MPU data bus. When an external master is accessing the on-chip peripherals, it is an input signal.
/MREQ	23(x13), 17(x15)	I/O, 3-State	Memory request signal. When an effective address for memory access is on the address bus, "0" is output. When an external master is accessing the on-chip peripherals, it is a tri-state signal.
/IORQ	21(x13), 15(x15)	I/O	I/O request signal. When addresses for I/O are on the lower 8 bits (A7-A0) of the address bus in the I/O operation, "0" is output. In addition, the /IORQ signal is output with the /M1 signal at the time of interrupt acknowledge cycle to inform peripheral LSI of the state of the interrupt response vector is when put on the data bus. When an external master is accessing the on-chip peripherals, it is an input signal.
/M1	17(x13), 8(x15)	I/O	Machine cycle "1". /MREQ and "0" are output together in the operation code fetch cycle. /M1 is output for every opcode fetch when a two byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with /IORQ. It is 3-stated in EV mode.

## SIO SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, 3-State	Function
/RxCA, /RxCB	35,51(x13), 33,49(x15)	In	Receive clock signal. In the asynchronous mode, the receive clocks can be 1, 16, 32, or 64 times the data transfer rate.
/TxCA, /TxCB	36,50(x13), 34,48(x15)	In	Transmitter clock signal. In the asynchronous mode, the transmitter clocks can be 1, 16, 32, or 64 times the data transfer rate.
TxDA, TxDB	37,49(x13), 35,47(x15)	Out	Serial transmit data signal.
/DTRA, /DTRB	38,48(x13), 36,46(x15)	Out	Data terminal ready signal. When ready, these signals go active to enable the terminal transmitter. When not ready they go inactive to disable the transfer from the terminal.
/RTSA, /RTSB	39,47(x13), 37,45(x15)	Out	Request to send signal. "0" when transmitting serial data. They are active when enabling their receivers to transmit data.
/CTSA, /CTSB	40,46(x13), 38,44(x15)	In	Clear to send signal. When "0", after transmitting these signals the modem is ready to receive serial data. When ready, these signals go active to enable terminal transmitter. When not ready, these signals go inactive to disable transfer from the terminal.
/DCDA, /DCDB	41,45(x13), 39,43(x15)	In	Data carrier detect signal. When "0", serial data can be received. These signals are active to enable receivers to transmit.

## SYSTEM CONTROL SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
IEI	60(x13), 72(x15)	In	Interrupt enable input signal. IEI is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.
IEO	59(x13), 71(x15)	Out	The interrupt enable output signal. In the daisy chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is "1" and the CPU is not servicing an interrupt from the on-chip peripherals.
/CS0 (C13/C15 only)	42(C13), 40(C15)	Out	Chip Select 0. Used to access external memory or I/O devices. This pin has been assigned to "ICT" pin on Z84013/015. This signal is decoded only from A15-A12 without control signals. Refer to "Functional Description" on-chip select signals for further explanation.

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The following pins have different functions between 013/015 and C13/C15

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Pin Name	Pin # X13	Pin # X15	Function
/RESET	28	9	Functionality is different.
/WAIT	19	15	Functionality is different.
EV	58	67	Functionality is different.
/WDTOUT	61	73	Push-pull output on Z84013/015, Open drain on Z84 C13/C15
ICT	40, 42	42, 40	(Test pin) on Z84013/015; /CS0 and /CS1 on Z84C13/15.
TxCA, TxCB, RxCA and RxCB	35, 36, 50, 51	33, 34, 48, 49	On Z84C13/15; these signals have Schmitt-triggered inputs.
/BUSACK	29	12	In EV mode, 3-stated on Z84C13/15; remains active on Z84013/015.

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## FUNCTIONAL DESCRIPTION

Figure 5(a) shows the functional block diagram of the Z84013/015 and Figure 5(b) shows the functional block diagram of the Z84C13/C15. As described earlier, the only difference between the Z84x13 and the Z84x15 is the PIO not being available on the Z84x13.

Functionally, the on-chip SIO, PIO (not available on Z84x13), CTC, and the Z80 CPU are the same as the discrete devices. Therefore, for detailed description of each individual unit, refer to the Product Specification/Technical Manual of each discrete product.

The following subsections describe each individual functional unit of the IPC.

### Z84C00/01 Logic Unit

The CPU provides all the capabilities and pins of the Zilog Z80 CPU. This allows 100% software compatibility with existing Z80 software. In addition, it has the pin called "A7RF" to extend DRAM refresh address to 8-bits. Refer to "Z84C01 Z80 CPU with CGC" Product Specification.

### Z84C20 Parallel Input/Output Logic Unit (Z84x15 Only)

This logic unit provides both TTL- and CMOS- compatible interfaces between peripheral devices and a CPU through the use of two 8-bit parallel ports (Figure 6). The CPU configures the logic to interface to a wide range of peripheral devices with no external logic. Typical devices that are compatible with this interface are keyboards, printers, and EPROM/PAL programmers.

The parallel ports (designated Port A and Port B) are byte wide and completely compatible with the Z84C20 PIO.

These two ports have several modes of operation; input, output, bi-directional, or bit control mode. Each port has two handshake signals (RDY and /STB) which are used to control data transfers. The RDY (ready) indicates that the port is ready for data transfer while /STB (strobe) is an input to the port that indicates when data transfer has occurred. Each of the ports can be programmed to interrupt the CPU upon the occurrence of specified status conditions, and generate unique interrupt vectors when the CPU responds (for more information on the operation of this portion of the logic, please refer to the Z84C20 PIO Product Specification and Technical Manual).

### Z84C30 Counter/Timer Logic Unit

This logic unit provides the user with four individual 8-bit Counter/Timer Channels that are compatible with the Z84C30 CTC (Figure 7). The Counter/Timers can be programmed by the CPU for a broad range of counting and timing applications. Typical applications include event counting, interrupt and interval counting, and serial baud rate clock generation.

Each of the Counter/Timer Channels, designated Channels 0-3, have an 8-bit prescaler (when used in timer mode) and its own 8-bit counter to provide a wide range of count resolution. Each of the channels have their own Clock/Trigger input to quantify the counting process and an output to indicate zero crossing/timeout conditions. With only one interrupt vector programmed into the logic unit, each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.

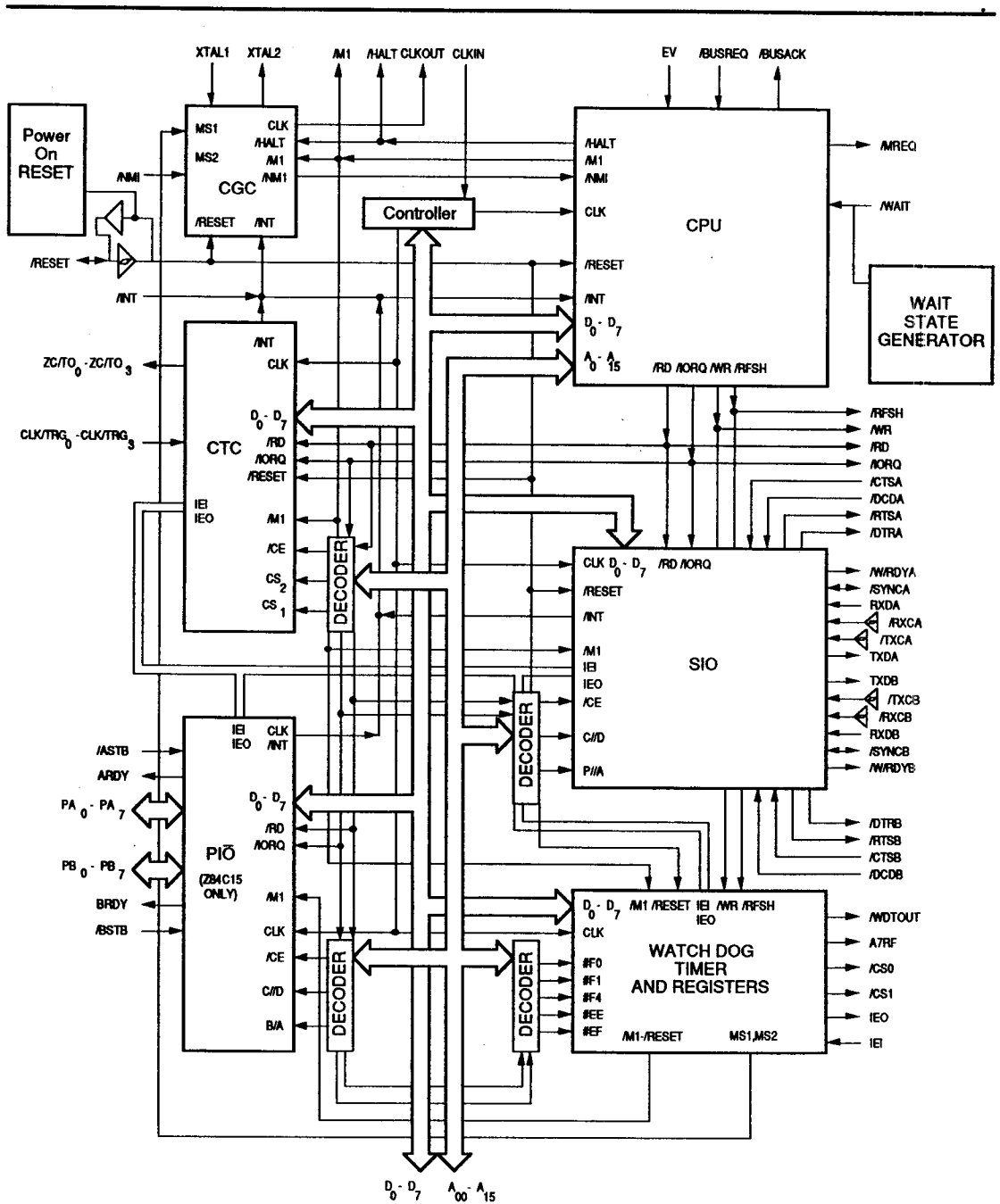


Figure 5(b). Block Diagram for 84C13/C15 IPC

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Recommended characteristics of the crystal and the values for the capacitor are as follows (the values will change with crystal frequency).

- Type of crystal: Fundamental, parallel type crystal (AT cut is recommended).
- Frequency tolerance: Application dependent.
- CL, Load capacitance: Approximately 22pf (acceptable range is 20-30pf).
- Rs, equivalent-series resistance:  $\leq 150$  ohms.
- Drive level: 10mW (for  $\leq 10$ MHz crystal); 5mW (for  $\geq 10$ MHz crystal).
- $C_{IN} = C_{OUT} = 33$ pF.

#### Power-On Reset Logic Unit (Z84C13/C15 Only)

The Z84C13/C15 has the enhanced feature of a Power-on Reset Circuit. During the power-up sequence, the open-drain gate of the on-chip power-on Reset circuit drives /RESET pin to "0" for 25 to 75 msec after the power supply passes through approx. 2.2V. After the termination of the "Power-on Reset" cycle, the open-drain gate of the on-chip Power-on Reset circuit stops to drive the /RESET pin. It is required to have external pull-up register on the /RESET pin.

If it receives /RESET input from outside after the power-on sequence and while the Reset Output Disable bit in Misc Control Register is cleared to "0", it will drive the /RESET pin for 16-processor clock cycles from the falling edge of the external /RESET input. Otherwise, the /RESET pin must be kept in the active state for a period of at least 3 system clock cycles.

If there are power-on reset circuits outside of this device, drive this pin with OPEN-DRAIN type gates with pull-up resistors because /RESET signal is driven low for the period mentioned above during the Power-on sequence. If the external Power-on Reset circuit has push-pull type drivers and they drive the /RESET pin to "1" during that period, it may cause damage. In particular, when using Z84C13/C15 in the Z84013/015 socket, modification may be required on the external reset circuit.

#### Wait State Generator Unit (Z84C13/C15 Only)

The Z84C13/C15 has the enhanced feature of a Wait State Generator circuit. It is capable of generating /WAIT signals to the CPU internally. The status of the External /WAIT input line is sampled after the insertion of software wait states, except for the wait state's insertion of Interrupt Daisy Chain Wait (for this cycle, insertion of a wait state is not simple).

The Wait State Control Register can be programmed to generate multiple Wait states during different CPU cycles listed as follows.

**Memory Wait and Opcode wait.** The Wait State Generator can put 0 to 3 wait states in memory accesses. Additionally, one added wait state can be inserted during an /M1 (Opcode fetch) cycle, because /M1 cycle's timing requirement is tighter than memory Read/Write cycles. It generates wait states to the Memory Access in a specified address range, which is programmed in the Memory Wait Boundary Register.

**I/O Wait.** The Wait State generator can put 0, 2, 4 or 6 wait states in I/O accesses. Regardless of the programming of this field, no I/O wait states are inserted for accesses to on-chip peripherals.

**Interrupt Vector Wait.** During Interrupt acknowledge cycle, the Wait State Generator can insert one wait state after /IORQ goes active, to extend the time between /IORQ fall to vector fetch by CPU. It allows a slow vector response device.

**Interrupt Daisy Chain Wait and RETI sequence extension.** During Interrupt acknowledge cycle, the Wait State Generator can insert 0, 2, 4 or 6 wait states between /M1 falling to /IORQ falling edge, to extend the time required to settle daisy chain. This allows a longer daisy chain. Also, this field controls the number of wait states inserted during RETI (Return From Interrupt) cycle. If specified to insert 4 or 6 wait states during Interrupt Acknowledge cycle, Wait State Generator also inserts wait states during RETI fetch sequence. This sequence is generated with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts 2 or 4 wait states, respectively, if op-code followed by EDh is 4Dh. One wait state if the following op-code is not 4Dh.

#### Chip Select Signals (Z84C13/C15 Only)

The Z84C13/C15 has an enhanced feature of adding two chip select (/CS0, /CS1) pins. Both signals are originally IC test pins (ICT) on the Z84013/015. The boundary value for each Chip Select Signal is 4 bits wide, and compare with A15-A12 of the address. Each Chip Select Signal goes active when:

- /CS0: (D3-D0 of CSBR)  $\geq$  A15-A12  $\geq$  0
- /CS1: (D7-D4 of CSBR)  $\geq$  A15-A12  $>$  (D3-D0 of CSBR)

(Where CSBR is the contents of Chip Select Boundary Register.)

There is also a separate /CS enable bit. /CS0 is enabled on power-up with a boundary value of "F" causing /CS0 to go active for all memory accesses. /CS1 is disabled on

**Table 1. I/O Control Register Address**

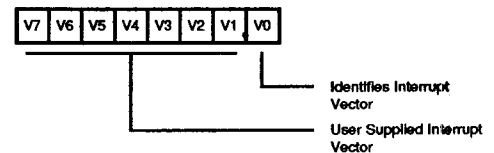
Address	Device	Channel	Register
10h	CTC	Ch 0	Control Register
11h	CTC	Ch 1	Control Register
12h	CTC	Ch 2	Control Register
13h	CTC	Ch 3	Control Register
18h	SIO	Ch. A	Data Register
19h	SIO	Ch. A	Control Register
1Ah	SIO	Ch. B	Data Register
1Bh	SIO	Ch. B	Control Register
1Ch	PIO	Port A	Data Register (Not with Z84x13)
1Dh	PIO	Port A	Command Register (Not with Z84x13)
1Eh	PIO	Port B	Data Register (Not with Z84x13)
1Fh	PIO	Port B	Command Register (Not with Z84x13)
F0h	Watch-Dog Timer		Master Register (WDTMR)
F1h	Watch-Dog Timer		Control Register (WDTCR)
F4h	Interrupt Priority Register		
EEh			System Control Register Pointer (SCRP) (Not with Z84013/015)
EFh			System Control Data Port (SCDP) (Not with Z84013/015)
Through SCR and SCDP			Control Register 00 - Wait State Control register (WCR) Control Register 01 - Memory Wait state Boundary Register (MWBR)
			Control Register 02 - Chip Select Boundary Register (CSBR) Control Register 03 - Misc. Control Register (MCR)

## PIO REGISTERS

For more detailed information, please refer to the PIO Technical Manual. These registers are not in the Z84x13.

### Interrupt Vector Word

The PIO logic unit is designed to work with the Z80 CPU in interrupt Mode 2. The interrupt word must be programmed if interrupts are used. Bit D0 must be a zero (Figure 11).



**Figure 11. PIO Interrupt Vector Word**



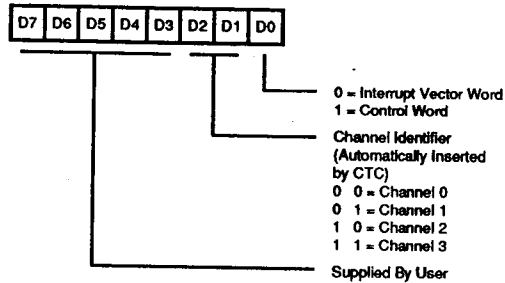
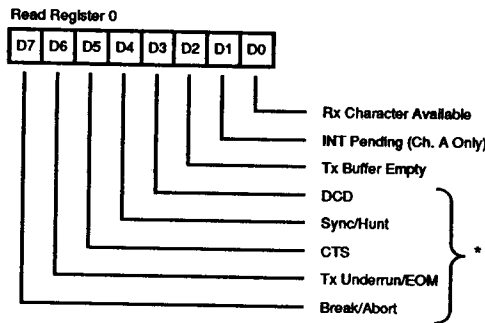


Figure 19. CTC Interrupt Vector Word

### SIO REGISTERS

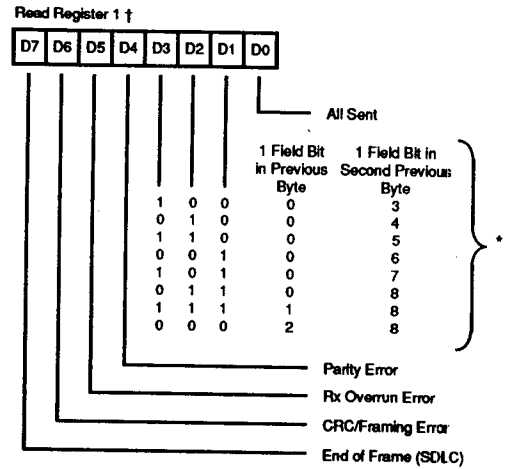
For more detailed information, refer to the SIO Technical Manual.

**Read Registers.** The SIO channel B contains three read registers while channel A contains only two that are read to obtain status information. To read the contents of a register (rather than RR0), the program must first write a pointer to WR0 in exactly the same manner as a write operation. The next I/O read cycle will place the contents of the selected read registers onto the data bus (Figure 20a, b, c).



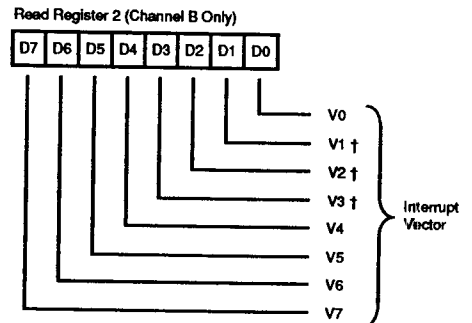
\* Used With "External/Status Interrupt" Modes

Figure 20a. SIO Read Register 0



\* Residue data for eight Rx bits/character programmed  
† Used with special receive condition mode

Figure 20b. SIO Read Register 1



† Variable if "Status Affects Vector" is programmed

Figure 20c. SIO Read Register 2

**Write Registers.** The SIO Channel B contains eight write registers while Channel A contains only seven that are programmed to configure the operating mode characteristics of each channel. With the exception of WR0, programming the write registers is a two step operation. The first operation is a pointer written to WR0 which points to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel (Figure 21).

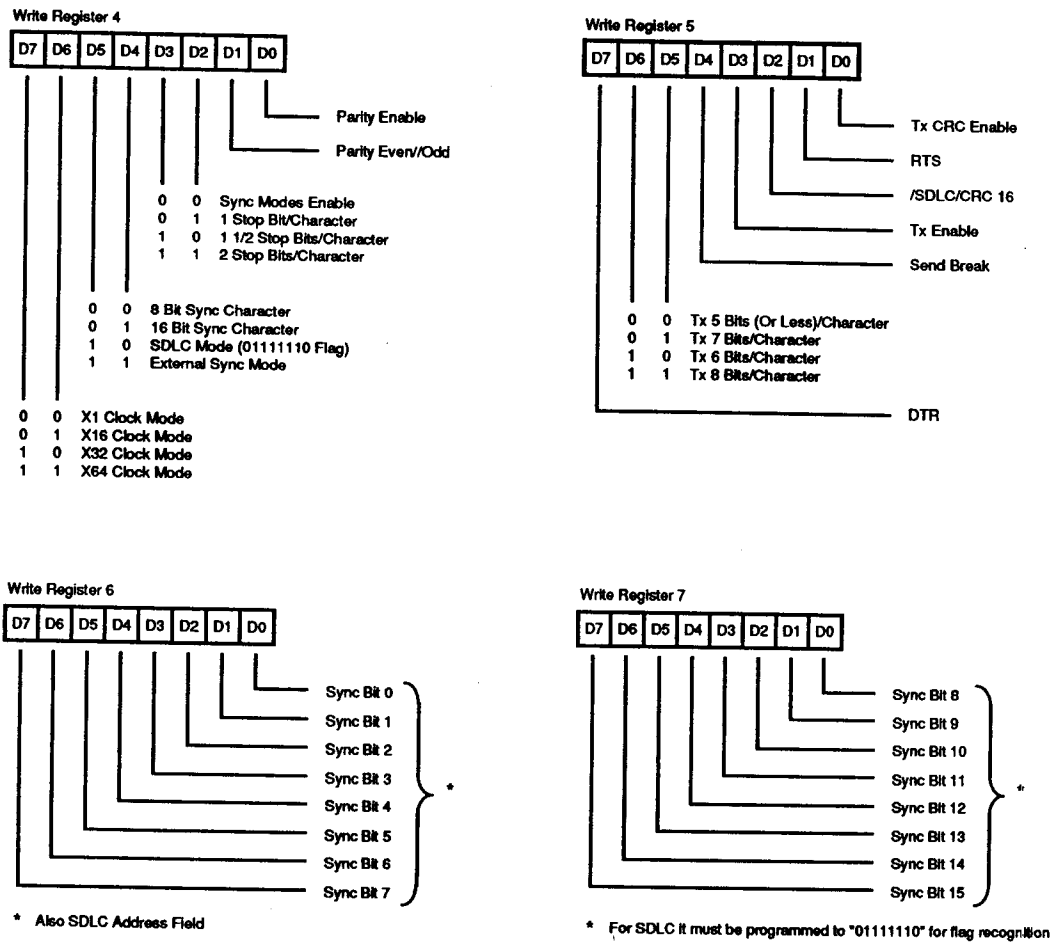


Figure 21. SIO Write Registers (Continued)

## WATCH DOG CONTROL REGISTERS

There are two registers to control Watch Dog Timer operations. These are Watch Dog Timer Master Register (WDTMR; I/O Address F0h) and the WDT Command Register (WDTCR; I/O Address F1h). Watch Dog Timer Logic has a "double key" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop due to program runaway. Programming the WDT follows this procedure. Also, these registers program the power-down mode of operation. The "Second key" is needed when turning off the Watch Dog Timer.

**Enabling the WDT.** The WDT is enabled by setting the WDT Enable Bit (D7:WDTE) to "1" and the WDT Periodic field (D5,D6:WDTP) to the desired time period. These command bits are in the Watch Dog Timer Master Register (WDTMR; I/O Address F0h).

**Disabling the WDT.** The WDT is disabled by clearing WDT Enable bit (WDTE) in the WDTMR to "0" followed by writing "B1h" to the WDT Command Register (WDTCR; I/O Address F1h).

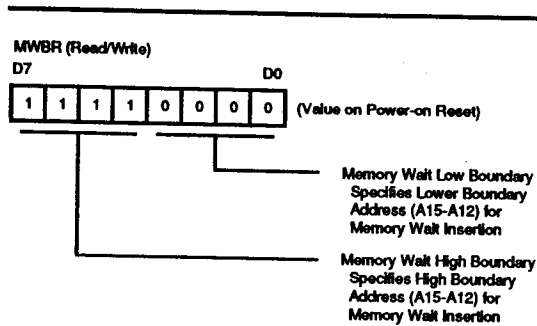


Figure 28. Memory Wait Boundary Register

**Bit D7-D4. Memory Wait High Boundary.** This field specifies A15-A12 of the upper address boundary for Memory Wait.

**Bit D3-D0. Memory Wait Low Boundary.** This field specifies A15-12 of the lower address boundary for Memory Wait.

Memory Wait states are inserted for the address range:

$$(D7-D4 \text{ of MWBR}) \geq A15-A12 \geq (D3-D0 \text{ of MWBR})$$

This register is set to "F0h" on Power-on Reset, which specifies the address range for Memory Wait as "0000h to FFFFh".

**Chip Select Boundary Register (CSBR, Control Register 02h)**

This register specifies the address range for each chip select signal. When accessed memory addresses are within this range, chip select signals are active (Figure 29).

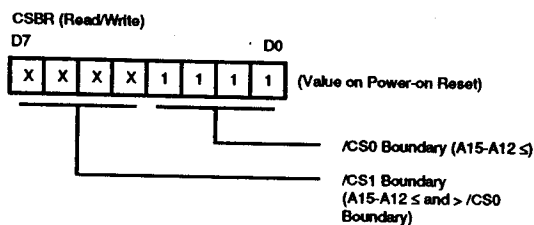


Figure 29. Chip Select Boundary Register

**D7-D4. /CS1 Boundary Address.** These bits specify the boundary address range for /CS1. The bit values are ignored on power-up as the /CS1 enable bit is off. The /CS1 is asserted if the address lines A15-12 have an address value greater than the programmed value for /CS0, and less than or equal to the programmed value in these bits.

**D3-D0. /CS0 Boundary Address.** These bits specify the boundary address range for /CS0. /CS0 is asserted if the address lines A15-12 have an address value less than or equal to the programmed boundary value. The /CS0 enable bit in the MCR must be set to 1. Upon Power-up reset, these bits come up as all 1's so that /CS0 is asserted for all addresses.

Chip Select signals are active for the address range:

$$\begin{aligned} /CS0: (D3-D0 \text{ of CSBR}) &\geq A15-A12 \geq 0 \\ /CS1: (D7-D4 \text{ of CSBR}) &\geq A15-A12 > \\ &(D3-D0 \text{ of CSBR}) \end{aligned}$$

This register is set to "xxxx1111b" on Power-on Reset, which specifies the address range of /CS0 for "0000h to FFFFh" (all Memory location) and /CS1 "undefined."

**Misc Control Register (MCR, Control Register 03h)**

This register specifies miscellaneous options on this device (Figure 30).

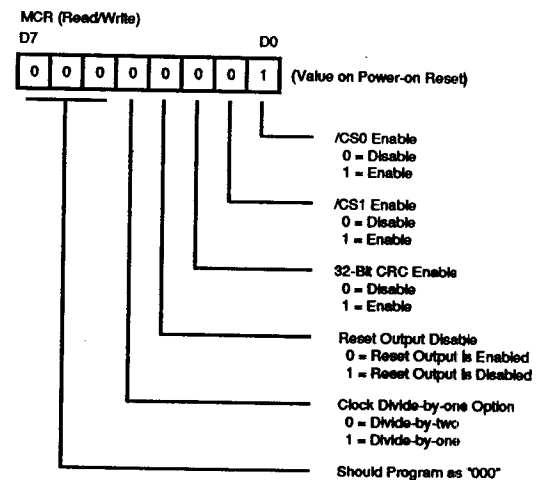


Figure 30. Misc Control Register

**Bit D7-D5. Reserved.** These three bits are reserved and are always programmed as "000".

**Bit D4. Clock Divide-by-one option.** "0"-Disable, "1"-enable. On-chip CGC unit has divide-by-two circuit. By setting this bit to one, this circuit is bypassed and CLKOUT is equal to X'tal oscillator frequency (or external clock input on the XTAL1 pin). This bit has no effect when the on-chip CGC unit is not in use and the external system clock is fed from CLKIN pin. Upon Power-on Reset, this bit is cleared to 0 and the clock is divided by two.

In IDLE2 Mode, the internal oscillator and clock output (CLKOUT) continue to operate. The internal system clock, fed from CLKIN to the components other than CTC is stopped at the T4 Low state of HALT instruction execution.

STOP Mode (HALTM=10). Shown in Figure 34 is the basic timing when the halt instruction is executed in STOP Mode.

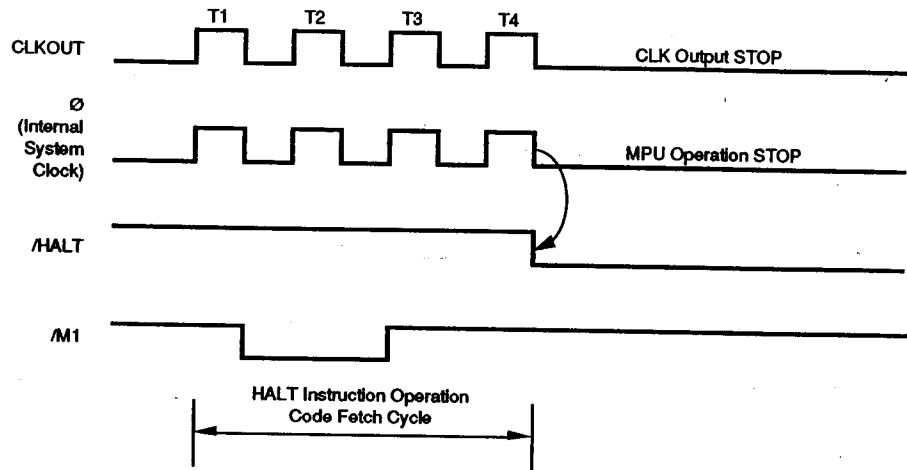


Figure 34. STOP Mode Timing  
(At Halt Instruction Execution)

In STOP Mode, the on-chip CGC unit is stopped at T4 Low state of HALT instruction execution. Therefore, clock output (CLKOUT), operation of Watch Dog Timer, CPU, PIO, CTC, SIO are stopped.

**Release from Halt State.** The halt state of the CPU is released when "0" is input to the /RESET signal and the MPU is reset or an interrupt request is accepted. An interrupt request signal is sampled at the leading edge of the last clock cycle (T4 state) of NOP instruction. In case of the maskable interrupt, interrupt will be accepted by an active /INT signal ("0" level). Also, the interrupt enable flip-

flop is set to "1". The accepted interrupt process is started from the next cycle.

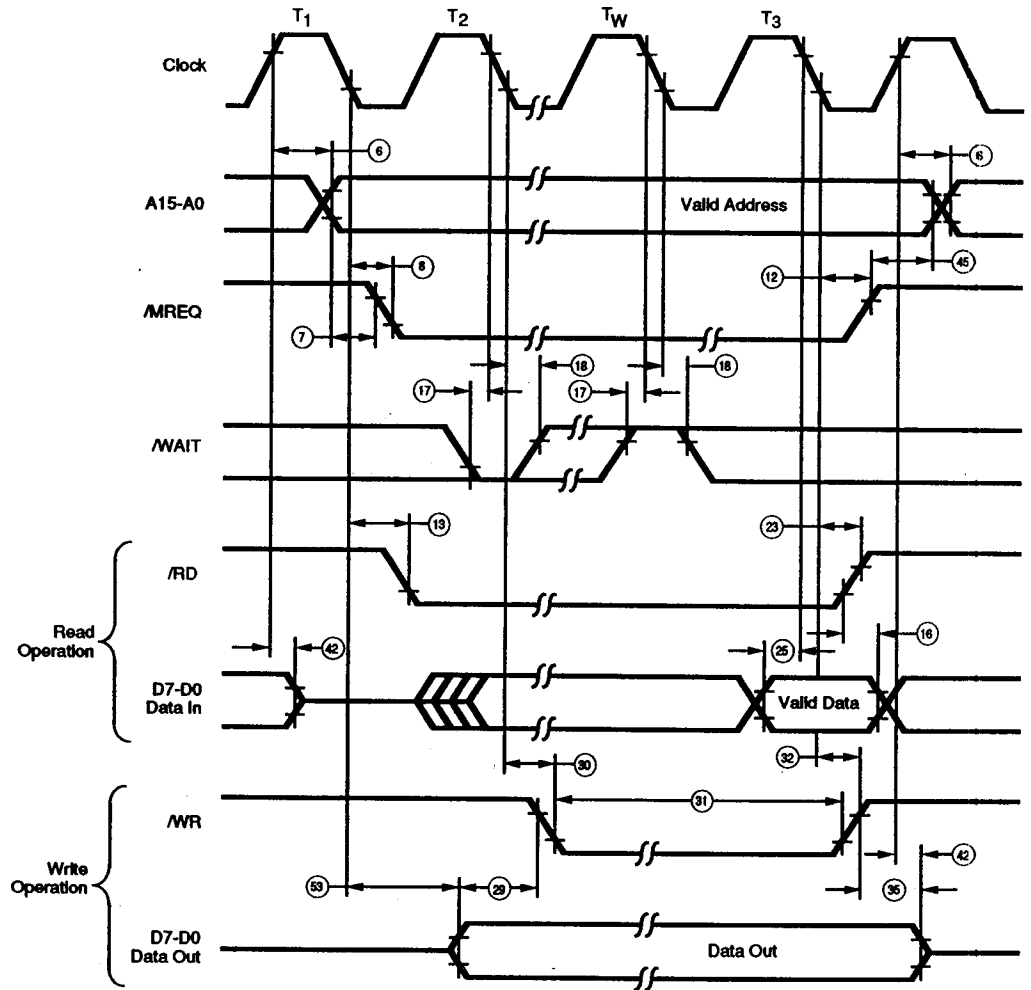
Further, when the internal system clock is stopped (IDLE1/2 Mode, STOP Mode), it is necessary first to restart the internal system clock. The internal system clock is restarted when /RESET or interrupt signal (/NMI or /INT) is asserted.

**RUN Mode (HALTM=11).** The halt release operation is enabled by interrupt request in RUN Mode (Figure 35).

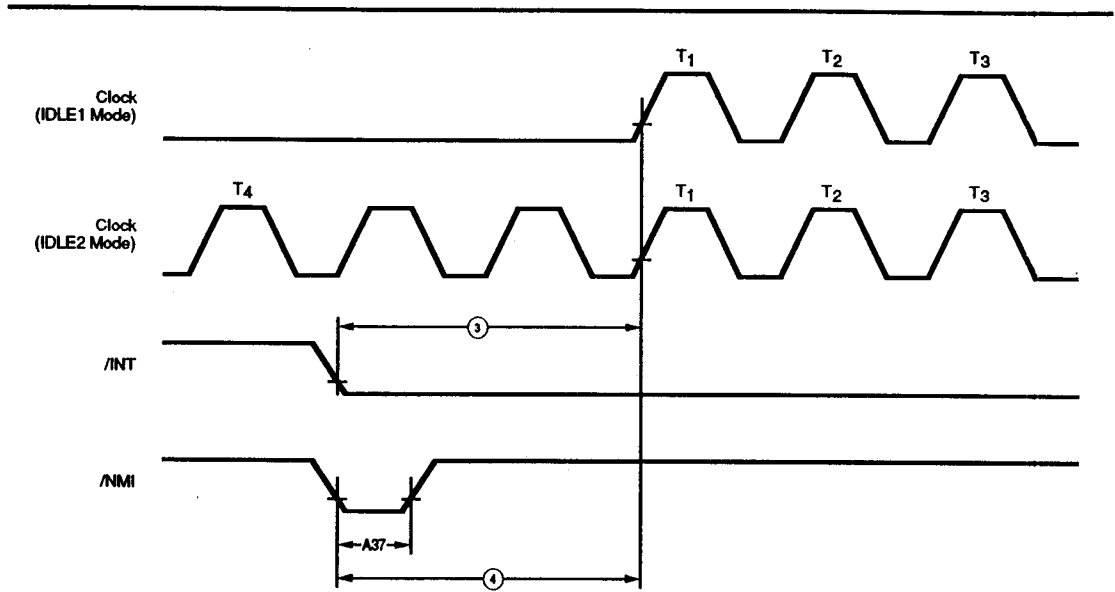


**Memory Read or Write Cycles.** Figure 42 shows the timing of memory read or write cycles other than an Op-code fetch (M1) cycle. The /MREQ and /RD signals function like the Op-code fetch cycle.

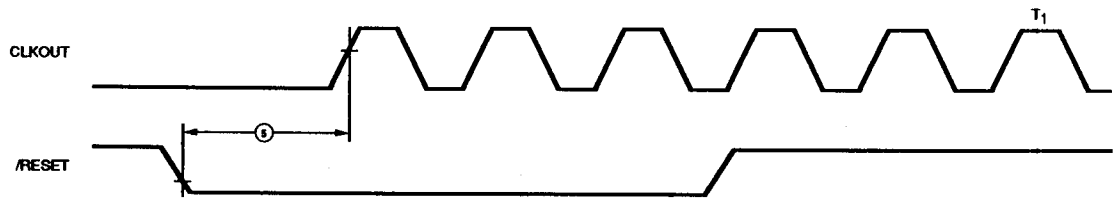
In a memory write cycle, /MREQ also becomes active when the Address Bus is stable. The /WR line is active when the Data Bus is stable, so that it can be used directly as an R/W pulse to most semiconductor memories.



**Figure 42. Memory Read or Write Cycle**  
(See Table A)

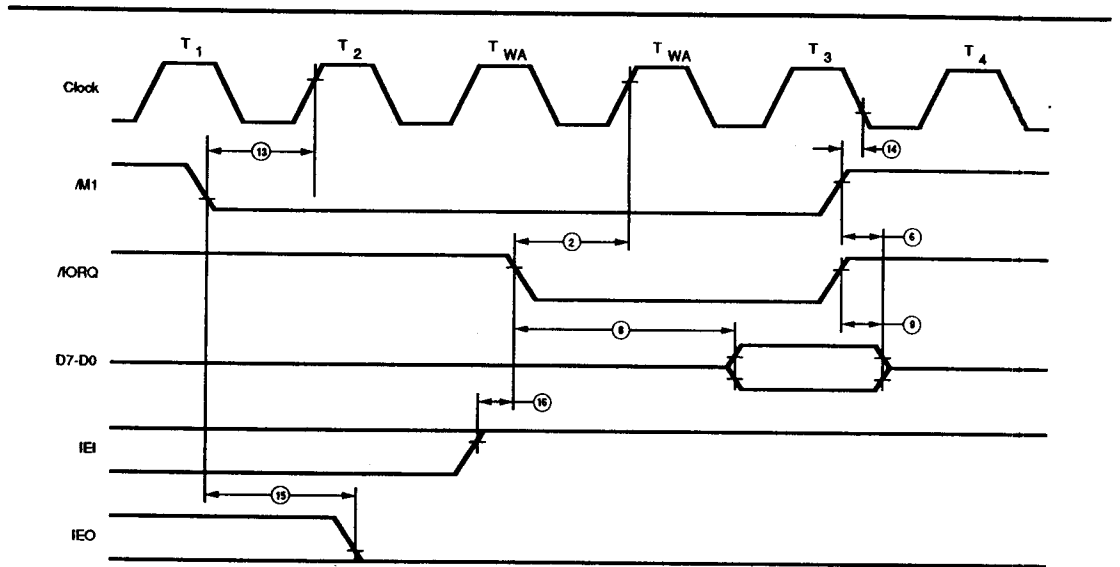


(a) Clock Restart Timing by /INT, /NMI (IDLE1/2 Mode)

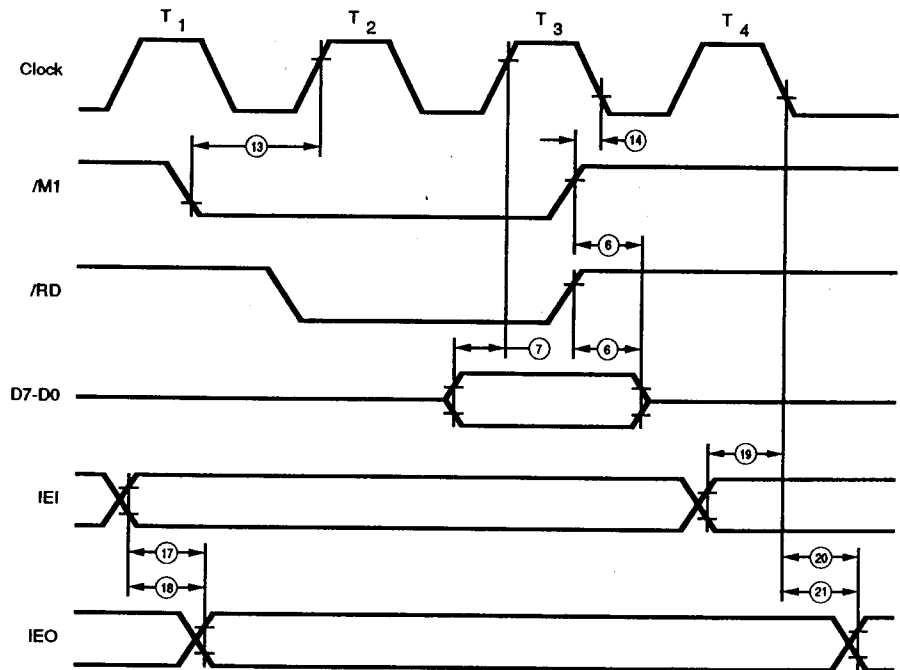


(b) Clock Restart Timing by /RESET (IDLE 1/2 Mode)

Figure 51. Clock Restart Timing (IDLE1/2 Mode)  
(See Table B)



(b) Interrupt Acknowledge Cycle Timing for On-chip peripheral from External Bus master  
(See Table C)



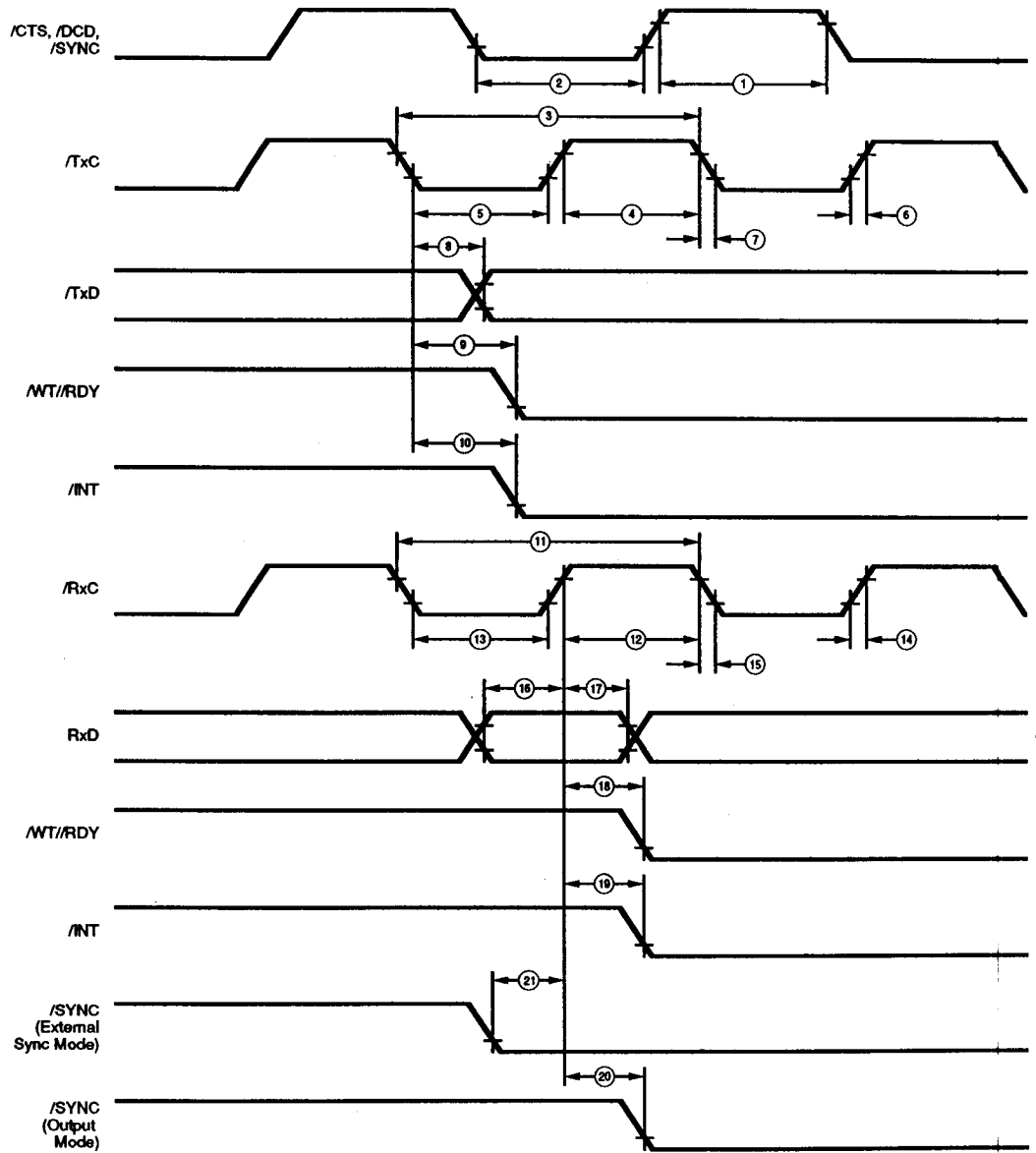
(c) Op-code fetch Cycle Timing for On-chip peripheral from External Bus master  
(See Table C)

Figure 53. On-chip Peripheral Timing from External Bus master (Continued)



### SIO Timing

Figure 56 shows the timing for on-chip SIO.



**Figure 56. SIO Timing**  
(See Table F)

## STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature range is:

E = -40°C to 100°C

Voltage Supply Range:

$+4.50V \leq V_{CC} \leq +5.50V$

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pF.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

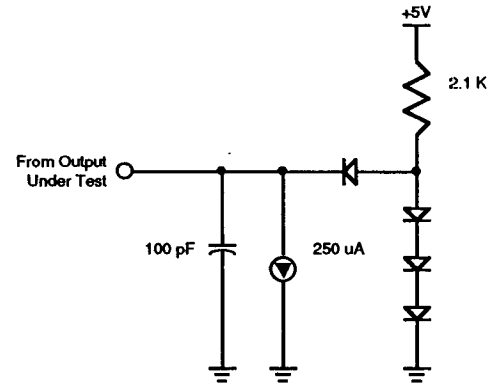


Figure 58. Standard Test Load

## CAPACITANCE

Guaranteed by design and characterization

Symbol	Parameter	Min	Max	Unit
$C_{\text{clock}}$	Clock Capacitance	35	pF	
$C_{\text{IN}}$	Input Capacitance	5	pF	
$C_{\text{OUT}}$	Output Capacitance	15	pF	

## DC CHARACTERISTICS

$V_{CC}=5.0V \pm 10\%$ , unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Condition
$V_{OLC}$	Clock Output High Voltage	$V_{CC}-0.6$		V	-2.0mA
$V_{OHC}$	Clock Output Low Voltage		0.4	V	+2.0mA
$V_{IHC}$	Clock Input High Voltage	$V_{CC}-0.6$		V	
$V_{ILC}$	Clock Input Low Voltage		0.4	V	
$V_{IH}$	Input High Voltage	2.2	$V_{CC}$	V	
$V_{IL}$	Input Low Voltage	-0.3	0.8	V	
$V_{OL}$	Output Low Voltage		0.4 [5]	V	$I_{LO}=2.0mA$
$V_{OH1}$	Output High Voltage	2.4		V	$I_{OH}=-1.6mA$
$V_{OH2}$	Output High Voltage	$V_{CC}-0.8$ [5]		V	$I_{OH}=-250\mu A$
$I_{CC1}$	Power Supply Current XTALIN = 10MHz XTALIN = 6MHz		50 30	mA mA	$V_{CC}=5V$ $V_{IH}=V_{CC}-0.2V$ $V_{IL}=0.2V$
$I_{CC2}$	Power Supply Current (STOP Mode)		50	$\mu A$	$V_{CC}=5V$
$I_{CC3}$	Power Supply Current (IDLE1 Mode) XTALIN = 10MHz XTALIN = 6MHz		6 4	mA mA	$V_{CC}=5V$ $V_{IH}=V_{CC}-0.2V$ $V_{IL}=0.2V$
$I_{CC4}$	Power Supply Current (IDLE2 Mode) XTALIN = 10MHz XTALIN = 6MHz		TBD [1] TBD [1]	mA mA	$V_{CC}=5V$ $V_{IH}=V_{CC}-0.2V$ $V_{IL}=0.2V$
$I_{LI}$	Input Leakage Current	-10	10 [4]	$\mu A$	$V_{IN}=0.4V$ to $V_{CC}$
$I_{L(SY)}$	SYNC pin Leakage Current	-40	10	$\mu A$	$V_{OUT}=0.4V$ to $V_{CC}$
$I_{LO}$	3-state Output Leakage Current in Float	-10	10 [2]	$\mu A$	$V_{OUT}=0.4V$ to $V_{CC}$
$I_{OH0}$	Darlington Drive Current (Port B and CTC ZC/TO)	-1.5		mA	$V_{OH}=1.5V$ REXT = 390 Ohms

### Notes:

[1] Measurements made with outputs floating.

[2] A15-A0, D7-D0, /MREQ, /IORQ, /RD and /WR.

[3]  $I_{CC2}$  Standby Current is guaranteed when the /HALT pin is low in STOP mode.

[4] All Pins except XTALI, where  $I_{LI}=\pm 25\mu A$ .

[5] A15-A0, D7-D0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1 and /BUSACK.

## AC CHARACTERISTICS

Table A. CPU Timing (See Figure 41 to 48)

No	Symbol	Parameter	Z84X1306 Z84X1506		Z84X1310 Z84X1510		Z84C1316* Z84C1516		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	TcC	Clock Cycle time	162**	DC	100**	DC	61	DC	nS	[A1]
2	TwCh	Clock Pulse Width (High)	65	DC	40	DC	20	DC	nS	[A1]
3	TwCl	Clock Pulse Width (Low)	65	DC	40	DC	20	DC	ns	[A1]
4	TfC	Clock Fall time		20		10		6	ns	[A1]
5	TrC	Clock Rise time		20		10		6	ns	[A1]
6	TdCr(A)	Address Valid from Clock Rise		90		65		55	ns	
7	TdA(MREQf)	Address Valid to /MREQ Fall	35**		0**		-15		ns	
8	TdCf(MREQf)	Clock Fall to /MREQ Fall Delay		70		55		40	ns	
9	TdCr(MREQr)	Clock Rise to /MREQ Rise Delay		70		55		40	ns	
10	TwMREQh	/MREQ Pulse Width (High)	65**		30**		10		ns	[A2]
11	TwMREQl	/MREQ Pulse Width (Low)	132**		75**		25		ns	[A2]
12	TdCf(MERQr)	Clock Fall to /MREQ Rise Delay		70		55		40	ns	
13	TdCf(RDf)	Clock Fall to /RD Fall Delay		80		65		40	ns	
14	TdCr(RDr)	Clock Rise to /RD Rise Delay		70		55		40	ns	
15	TsD(Cr)	Data Setup Time to Clock Rise	30		25		10		ns	
16	ThD(RDr)	Data Hold Time After /RD Rise	0		0		0		ns	
17	TsWAIT(Cf)	/WAIT Setup Time to Clock Fall	60		20		75		ns	
18	ThWAIT(Cf)	/WAIT Hold Time After Clock Fall	10		10		10		ns	
19	TdCr(M1f)	Clock Rise to /M1 Fall Delay		80		65		40	ns	
20	TdCr(M1r)	Clock Rise to /M1 Rise Delay		80		65		40	ns	
21	TdCr(RFSHf)	Clock Rise to /RFSH Fall Delay		110		80		60	ns	
22	TdCr(RFSHr)	Clock Rise to /RFSH Rise Delay		100		80		60	ns	
23	TdCf(RDr)	Clock Fall to /RD Rise Delay		70		55		40	ns	
24	TdCr(RDf)	Clock Rise to /RD Fall Delay		70		55		40	ns	
25	TsD(Cf)	Data Setup to Clock Fall During M2, M3, M4 or M5 Cycles	40		25		12		ns	
26	TdA(IORQf)	Address Stable Prior to /IORQ Fall	107**		50**		0		ns	
27	TdCr(IORQf)	Clock Rise to /IORQ Fall Delay		65		50		40	ns	
28	TdCf(IORQr)	Clock Fall to /IORQ Rise Delay		70		55		40	ns	
29	TdD(WRf)	Data Stable Prior to /WR Fall	22**		40**		-10		ns	
30	TdCf(WRf)	Clock Fall to /WR Fall Delay		70		55		40	ns	
31	TwWR	/WR Pulse Width	132**		75**		25		ns	
32	TdCf(WRr)	Clock Fall to /WR Rise Delay		70		55		40	ns	
33	TdD(WRf)IO	Data Stable Prior to /WR Fall	-55**		-10**		-30		ns	
34	TdCr(WRf)	Clock Rise to /WR Fall Delay		60		50		40	ns	
35	TdWRr(D)	Data Stable from /WR Fall	30**		10**		0	0	ns	
36	TdCf(HALT)	Clock Fall to /HALT 0 or 1		260		90		70	ns	
37	TwNMI	/NMI pulse Width	60		60		60		ns	
38	TsBUSREQ(Cr)	/BUSREQ Setup Time to Clock Rise	50		30		15		ns	
39	ThBUSREQ(Cr)	/BUSREQ Hold Time after Clock Rise	10		10		10		ns	
40	TdCr(BUSACKf)	Clock Rise to /BASACK Fall Delay		90		75		40	ns	

## AC CHARACTERISTICS (Continued)

Table B. CGC Timing (See Figure 49 to 52)

No	Symbol	Parameter	Z84C1306 Z84C1506		Z84C1310 Z84C1510		Z84C1316* Z84C1516		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	TRST(INT)S	Clock Restart Time by /INT (STOP Mode)	(Typ)2 <sup>14</sup> +2.5TcC		(Typ)2 <sup>14</sup> +2.5TcC		(Typ)2 <sup>14</sup> +2.5TcC		ns	
2	TRST(MNI)S	Clock Restart Time by /NMI (STOP Mode)	(Typ)2 <sup>14</sup> +2.5TcC		(Typ)2 <sup>14</sup> +2.5TcC		(Typ)2 <sup>14</sup> +2.5TcC		ns	
3	TRST(INT)I	Clock Restart Time by /INT (IDLE Mode)	2.5TcT		2.5TcT		2.5TcT		ns	
4	TRST(Nmi)I	Clock Restart Time by /NMI (IDLE Mode)	2.5TcT		2.5TcT		2.5TcT		ns	
5	TRST(RESET)I	Clock Restart Time by /RESET (IDLE Mode)	1TcC		1TcC		1TcC		ns	
6	TiCLKOUT	CLKOUT Rise Time		15		10		6	ns	
7	TrCLKOUT	CLKOUT Fall time		15		10		6	ns	
8	TcX1	XTAL1 Cycle Time (for External Clock Input on XTAL1)								
		Divide-by-Two Mode	81		50		31		ns	
		Divide-by-One Mode	162		100		61		ns	
9	TwiX1	XTAL1 Low Pulse Width (for External Clock Input on XTAL1)								
		Divide-by-Two Mode	35		15		10		ns	
		Divide-by-One Mode	65		40		25		ns	
10	TwhX1	XTAL1 High Pulse Width (for External Clock input on XTAL1)								
		Divide-by-Two mode	35		15		10		ns	
		Divide-by-One mode	65		40		25		ns	
11	TrX1	XTAL1 Rise Time (for External Clock Input on XTAL1)		25		25		15	ns	[B1]
12	TfX1	XTAL1 Fall Time (for External Clock Input on XTAL1)		25		25		15	ns	[B1]

**Note:**

[B1] If parameters 8 and 9 are not met, adjust parameters 11 and 12 to satisfy parameters 8 and 9.