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Details

Product Status	Obsolete
Core Processor	Z80
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z84c1510fec00tr

CPU SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
A0-A15	16-1(x13), 6-1, 100-91(x15)	I/O	16-bit address bus. Specifies I/O and memory addresses to be accessed. During the refresh period, addresses for refreshing are output. The bus is an input when the external master is accessing the on-chip peripherals.
D0-D7	83-76(x13), 89-82(x15)	I/O	8-bit bidirectional data bus. When the on-chip CPU is accessing on-chip peripherals, these lines are set to output and hold the data to/from on-chip peripherals.
/RD	30(x13), 14(x15)	I/O	Read signal. CPU read signal for accepting data from memory or I/O devices. When an external master is accessing the on-chip peripherals, it is an input signal.
/WR	20(x13), 13(x15)	I/O	Write Signal. This signal is output when data, to be stored in a specified memory or peripheral LSI, is on the MPU data bus. When an external master is accessing the on-chip peripherals, it is an input signal.
/MREQ	23(x13), 17(x15)	I/O, 3-State	Memory request signal. When an effective address for memory access is on the address bus, "0" is output. When an external master is accessing the on-chip peripherals, it is a tri-state signal.
/IORQ	21(x13), 15(x15)	I/O	I/O request signal. When addresses for I/O are on the lower 8 bits (A7-A0) of the address bus in the I/O operation, "0" is output. In addition, the /IORQ signal is output with the /M1 signal at the time of interrupt acknowledge cycle to inform peripheral LSI of the state of the interrupt response vector is when put on the data bus. When an external master is accessing the on-chip peripherals, it is an input signal.
/M1	17(x13), 8(x15)	I/O	Machine cycle "1". /MREQ and "0" are output together in the operation code fetch cycle. /M1 is output for every opcode fetch when a two byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with /IORQ. It is 3-stated in EV mode.

CPU SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, 3-State	Function
A7RF	55(x13), 70(x15)	Out	1-bit auxiliary address bus. Output is the same as bit-7 (A7) of the address bus. However, during a refresh cycle, this pin outputs the address which is the most significant bit of the 8-bit refresh address signal linked to the low order 7 bits of the address bus.

CTC SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
CLK/TRG0 - CLK/TRG3	75-72(x13), 81-78(x15)	In	External clock/trigger input. These four CLK/TRG pins correspond to four Counter/Timer Channels. In the counter mode, each active edge will cause the downcounter to decrement by one. In timer mode, an active edge will start the timer. It is program selectable whether the active edge is rising or falling.
ZC/T00 - ZC/T03	68-71(x13), 74-77(x15)	Out	Zero count/timer out signal. In either timer or counter mode, pulses are output when the down-counter has reached zero.

SIO SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
/W//RDYA, /W//RDYB	32,54(x13), 30,52(x15)	Out	Wait/Ready signal A and Wait/Ready signal B. Used as /WAIT or /READY depending upon SIO programming. When programmed as /WAIT they go active at "0", alerting the CPU that addressed memory or I/O devices are not ready by requesting the CPU to wait. When programmed as /READY, they are active at "0" which determines when a peripheral device associated with a DMA port is for read/write data.
/SYNCA, /SYNCB	33,53(x13), 31,51(x15)	I/O	Synchronous signals. In asynchronous receive mode, they act as /CTS and /CDC. In external sync mode, these signals act as inputs. In internal sync mode, they act as outputs.
RxDA, RxDB	34,52(x13), 32,50(x15)	In	Serial receive data signal.

SIO SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, 3-State	Function
/RxCA, /RxCB	35,51(x13), 33,49(x15)	In	Receive clock signal. In the asynchronous mode, the receive clocks can be 1, 16, 32, or 64 times the data transfer rate.
/TxCA, /TxCB	36,50(x13), 34,48(x15)	In	Transmitter clock signal. In the asynchronous mode, the transmitter clocks can be 1, 16, 32, or 64 times the data transfer rate.
TxDA, TxDB	37,49(x13), 35,47(x15)	Out	Serial transmit data signal.
/DTRA, /DTRB	38,48(x13), 36,46(x15)	Out	Data terminal ready signal. When ready, these signals go active to enable the terminal transmitter. When not ready they go inactive to disable the transfer from the terminal.
/RTSA, /RTSB	39,47(x13), 37,45(x15)	Out	Request to send signal. "0" when transmitting serial data. They are active when enabling their receivers to transmit data.
/CTSA, /CTSB	40,46(x13), 38,44(x15)	In	Clear to send signal. When "0", after transmitting these signals the modem is ready to receive serial data. When ready, these signals go active to enable terminal transmitter. When not ready, these signals go inactive to disable transfer from the terminal.
/DCDA, /DCDB	41,45(x13), 39,43(x15)	In	Data carrier detect signal. When "0", serial data can be received. These signals are active to enable receivers to transmit.

SYSTEM CONTROL SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
IEI	60(x13), 72(x15)	In	Interrupt enable input signal. IEI is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.
IEO	59(x13), 71(x15)	Out	The interrupt enable output signal. In the daisy chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is "1" and the CPU is not servicing an interrupt from the on-chip peripherals.
/CS0 (C13/C15 only)	42(C13), 40(C15)	Out	Chip Select 0. Used to access external memory or I/O devices. This pin has been assigned to "ICT" pin on Z84013/015. This signal is decoded only from A15-A12 without control signals. Refer to "Functional Description" on-chip select signals for further explanation.

Recommended characteristics of the crystal and the values for the capacitor are as follows (the values will change with crystal frequency).

- Type of crystal: Fundamental, parallel type crystal (AT cut is recommended).
- Frequency tolerance: Application dependent.
- CL, Load capacitance: Approximately 22pf (acceptable range is 20-30pf).
- Rs, equivalent-series resistance: ≤ 150 ohms.
- Drive level: 10mW (for ≤ 10 MHz crystal); 5mW (for ≥ 10 MHz crystal).
- $C_{IN} = C_{OUT} = 33$ pF.

Power-On Reset Logic Unit (Z84C13/C15 Only)

The Z84C13/C15 has the enhanced feature of a Power-on Reset Circuit. During the power-up sequence, the open-drain gate of the on-chip power-on Reset circuit drives /RESET pin to "0" for 25 to 75 msec after the power supply passes through approx. 2.2V. After the termination of the "Power-on Reset" cycle, the open-drain gate of the on-chip Power-on Reset circuit stops to drive the /RESET pin. It is required to have external pull-up register on the /RESET pin.

If it receives /RESET input from outside after the power-on sequence and while the Reset Output Disable bit in Misc Control Register is cleared to "0", it will drive the /RESET pin for 16-processor clock cycles from the falling edge of the external /RESET input. Otherwise, the /RESET pin must be kept in the active state for a period of at least 3 system clock cycles.

If there are power-on reset circuits outside of this device, drive this pin with OPEN-DRAIN type gates with pull-up resistors because /RESET signal is driven low for the period mentioned above during the Power-on sequence. If the external Power-on Reset circuit has push-pull type drivers and they drive the /RESET pin to "1" during that period, it may cause damage. In particular, when using Z84C13/C15 in the Z84013/015 socket, modification may be required on the external reset circuit.

Wait State Generator Unit (Z84C13/C15 Only)

The Z84C13/C15 has the enhanced feature of a Wait State Generator circuit. It is capable of generating /WAIT signals to the CPU internally. The status of the External /WAIT input line is sampled after the insertion of software wait states, except for the wait state's insertion of Interrupt Daisy Chain Wait (for this cycle, insertion of a wait state is not simple).

The Wait State Control Register can be programmed to generate multiple Wait states during different CPU cycles listed as follows.

Memory Wait and Opcode wait. The Wait State Generator can put 0 to 3 wait states in memory accesses. Additionally, one added wait state can be inserted during an /M1 (Opcode fetch) cycle, because /M1 cycle's timing requirement is tighter than memory Read/Write cycles. It generates wait states to the Memory Access in a specified address range, which is programmed in the Memory Wait Boundary Register.

I/O Wait. The Wait State generator can put 0, 2, 4 or 6 wait states in I/O accesses. Regardless of the programming of this field, no I/O wait states are inserted for accesses to on-chip peripherals.

Interrupt Vector Wait. During Interrupt acknowledge cycle, the Wait State Generator can insert one wait state after /IORQ goes active, to extend the time between /IORQ fall to vector fetch by CPU. It allows a slow vector response device.

Interrupt Daisy Chain Wait and RETI sequence extension. During Interrupt acknowledge cycle, the Wait State Generator can insert 0, 2, 4 or 6 wait states between /M1 falling to /IORQ falling edge, to extend the time required to settle daisy chain. This allows a longer daisy chain. Also, this field controls the number of wait states inserted during RETI (Return From Interrupt) cycle. If specified to insert 4 or 6 wait states during Interrupt Acknowledge cycle, Wait State Generator also inserts wait states during RETI fetch sequence. This sequence is generated with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts 2 or 4 wait states, respectively, if op-code followed by EDh is 4Dh. One wait state if the following op-code is not 4Dh.

Chip Select Signals (Z84C13/C15 Only)

The Z84C13/C15 has an enhanced feature of adding two chip select (/CS0, /CS1) pins. Both signals are originally IC test pins (ICT) on the Z84013/015. The boundary value for each Chip Select Signal is 4 bits wide, and compare with A15-A12 of the address. Each Chip Select Signal goes active when:

/CS0: (D3-D0 of CSBR) \geq A15-A12 \geq 0

/CS1: (D7-D4 of CSBR) \geq A15-A12 $>$ (D3-D0 of CSBR)

(Where CSBR is the contents of Chip Select Boundary Register.)

There is also a separate /CS enable bit. /CS0 is enabled on power-up with a boundary value of "F" causing /CS0 to go active for all memory accesses. /CS1 is disabled on

Table 1. I/O Control Register Address

Address	Device	Channel	Register
10h	CTC	Ch 0	Control Register
11h	CTC	Ch 1	Control Register
12h	CTC	Ch 2	Control Register
13h	CTC	Ch 3	Control Register
18h	SIO	Ch. A	Data Register
19h	SIO	Ch. A	Control Register
1Ah	SIO	Ch. B	Data Register
1Bh	SIO	Ch. B	Control Register
1Ch	PIO	Port A	Data Register (Not with Z84x13)
1Dh	PIO	Port A	Command Register (Not with Z84x13)
1Eh	PIO	Port B	Data Register (Not with Z84x13)
1Fh	PIO	Port B	Command Register (Not with Z84x13)
F0h	Watch-Dog Timer		Master Register (WDTMR)
F1h	Watch-Dog Timer		Control Register (WDTCR)
F4h	Interrupt Priority Register		
EEh			System Control Register Pointer (SCRP) (Not with Z84013/015)
EFh			System Control Data Port (SCDP) (Not with Z84013/015)
Through SCRП and SCDP			Control Register 00 - Wait State Control register (WCR) Control Register 01 - Memory Wait state Boundary Register (MWBR)
			Control Register 02 - Chip Select Boundary Register (CSBR) Control Register 03 - Misc. Control Register (MCR)

PIO REGISTERS

For more detailed information, please refer to the PIO Technical Manual. These registers are not in the Z84x13.

Interrupt Vector Word

The PIO logic unit is designed to work with the Z80 CPU in interrupt Mode 2. The interrupt word must be programmed if interrupts are used. Bit D0 must be a zero (Figure 11).

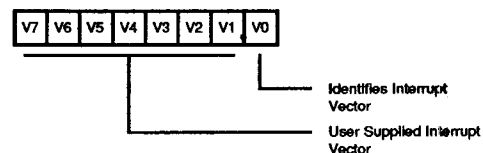


Figure 11. PIO Interrupt Vector Word

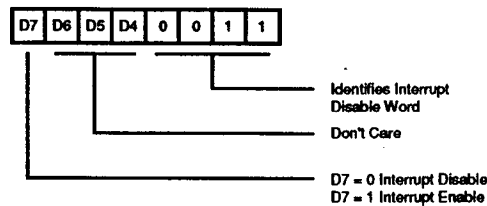


Figure 16. Interrupt Disable Word

CTC CONTROL REGISTERS

For more detailed information, refer to the CTC Technical Manual.

Channel Control Word

This word sets the operating modes and parameters as described below. Bit D0 is a "1" to indicate that this is a Control Word (Figure 17).

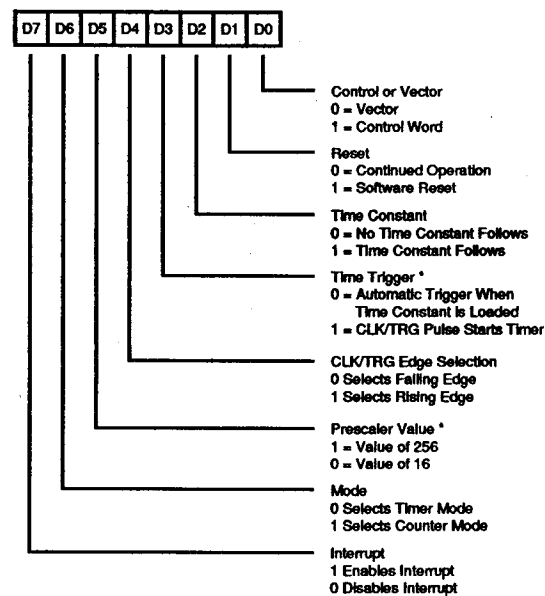


Figure 17. CTC Channel Control Word

Bit D7. Interrupt Enable. This bit enables the interrupt logic so that an internal INT can be generated at zero count. Interrupts are programmed in either mode and may be enabled or disabled at any time.

Bit D6. Mode Bit. This bit selects either Timer Mode or Counter Mode.

Bit D5. Prescaler Factor. This bit selects the prescaler factor for use in the timer mode. Either divide-by-16 or divide-by-256 is available.

Bit D4. Clock/Trigger Edge Selector. This bit selects the active edge of the CLK/TRG input pulses.

Bit D3. Timer Trigger. This bit selects the trigger mode for timer operation. Either automatic or external trigger may be selected.

Bit D2. Time Constant. This bit indicates that the next word programmed is time constant data for the downcounter.

Bit D1. Software Reset. Writing 1 to this bit indicates a software reset operation, which stops counting activities until another time constant word is written.

Time Constant Word

Before a channel starts counting, it must receive a time constant word. The time constant value is anywhere between 1 and 256, with "0" being accepted as a count of 256 (Figure 18).

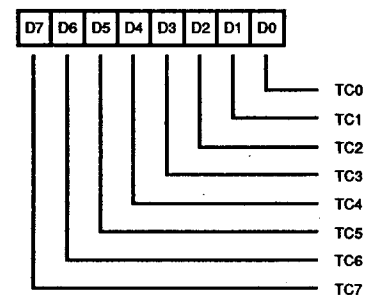


Figure 18. CTC Time Constant Word

Interrupt Vector Word

If one or more of the CTC channels have interrupt enabled, then the Interrupt Vector Word must be programmed. Only the five most significant bits of this word are programmed, and bit D0 must be "0". Bits D2-D1 are automatically modified by the CTC channels when it responds with an interrupt vector (Figure 19).

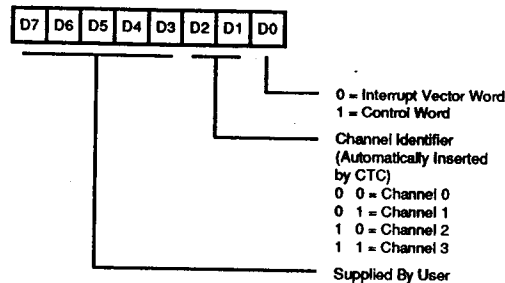
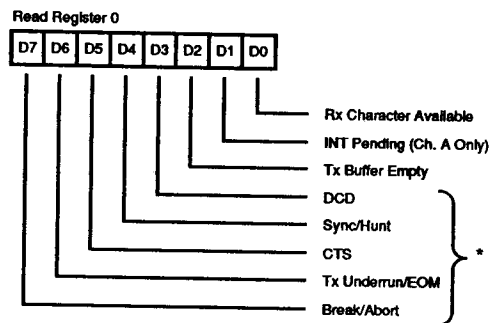


Figure 19. CTC Interrupt Vector Word

SIO REGISTERS

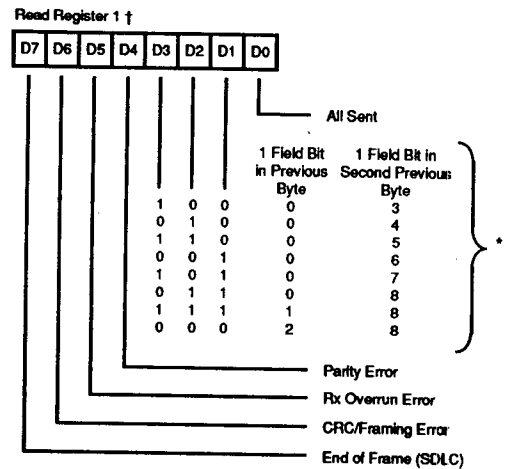
For more detailed information, refer to the SIO Technical Manual.

Read Registers. The SIO channel B contains three read registers while channel A contains only two that are read to obtain status information. To read the contents of a register (rather than RR0), the program must first write a pointer to WR0 in exactly the same manner as a write operation. The next I/O read cycle will place the contents of the selected read registers onto the data bus (Figure 20a, b, c).



* Used With "External/Status Interrupt" Modes

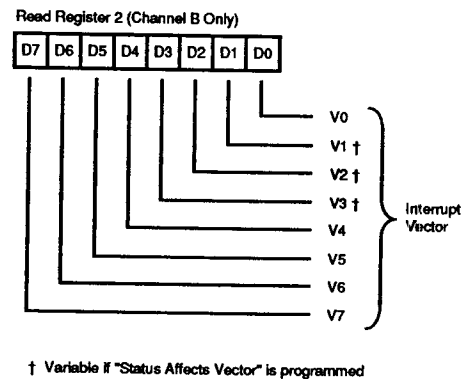
Figure 20a. SIO Read Register 0



* Residue data for eight Rx bits/character programmed

† Used with special receive condition mode

Figure 20b. SIO Read Register 1



† Variable if "Status Affects Vector" is programmed

Figure 20c. SIO Read Register 2

Write Registers. The SIO Channel B contains eight write registers while Channel A contains only seven that are programmed to configure the operating mode characteristics of each channel. With the exception of WR0, programming the write registers is a two step operation. The first operation is a pointer written to WR0 which points to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel (Figure 21).

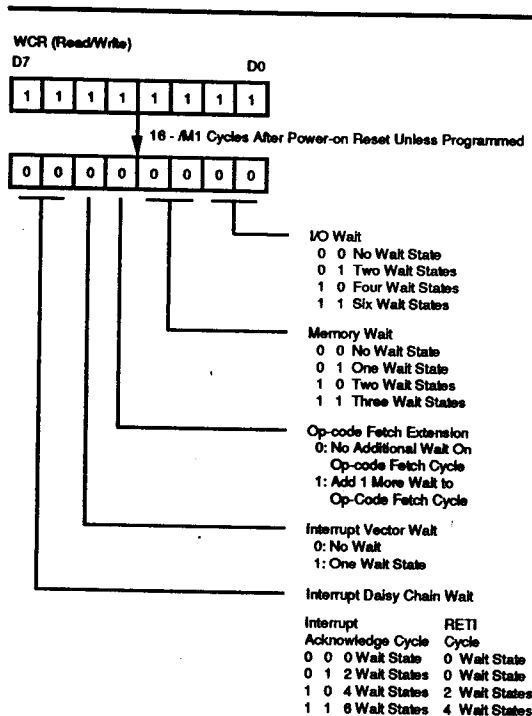


Figure 27. Wait State Control Register

This register has the following fields:

Bit 7-6. Interrupt Daisy Chain Wait. This 2-bit field specifies the number of wait states to be inserted during an Interrupt Daisy Chain settle period of the Interrupt Acknowledge cycle, which is /IORQ falls after the settling period from /M1 going active "0". Also, this field controls the number of wait states inserted during the RETI (Return From Interrupt) cycle. If specified to insert 4 or 6 wait states during Interrupt Acknowledge cycle, the Wait state generator also inserts wait states during RETI fetch sequence. This sequence is formed with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts 1 wait state if op-code followed by EDh is NOT 4Dh, and inserts 2 or 4 wait states, respectively, if the following op-code is 4Dh.

Interrupt Acknowledge	RETI cycle
00 - No Wait states	No Wait states
01 - 2 Wait states	No Wait states
10 - 4 Wait states	2 Wait states
11 - 6 Wait states	4 Wait states

For fifteen /M1 cycles from Power-on Reset, bits 7-6 are set to "11". They clear to "00" on the trailing edge of the 16th /M1 signal unless programmed.

Bit 5. Interrupt Vector Wait. While this bit is set to one, the wait state generator inserts one wait state after the /IORQ signal goes active during the Interrupt acknowledge cycle. This gives more time for the vector read cycle. While this bit is cleared to zero, no wait state is inserted (standard timing). For fifteen /M1 cycles from Power-on Reset, this bit is set to "1", then cleared to "0" on the trailing edge of the 16th /M1 signal, unless programmed.

Bit 4. Opcode Fetch Extension. If this bit is set to "1", one additional wait state is inserted during the Op-code fetch cycle in addition to the number of wait states programmed in the Memory Wait field. For fifteen /M1 cycles from Power-on Reset, this bit is set to "1", then cleared to "0" on the trailing edge of the 16th /M1 signal, unless programmed.

Bit 3-2. Memory Wait States. This 2-bit field specifies the number of wait states to be inserted during memory Read/Write transactions.

- 00 - No Wait states
- 01 - 1 Wait states
- 10 - 2 Wait states
- 11 - 3 Wait states

For fifteen /M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the 16th /M1 signal, unless programmed.

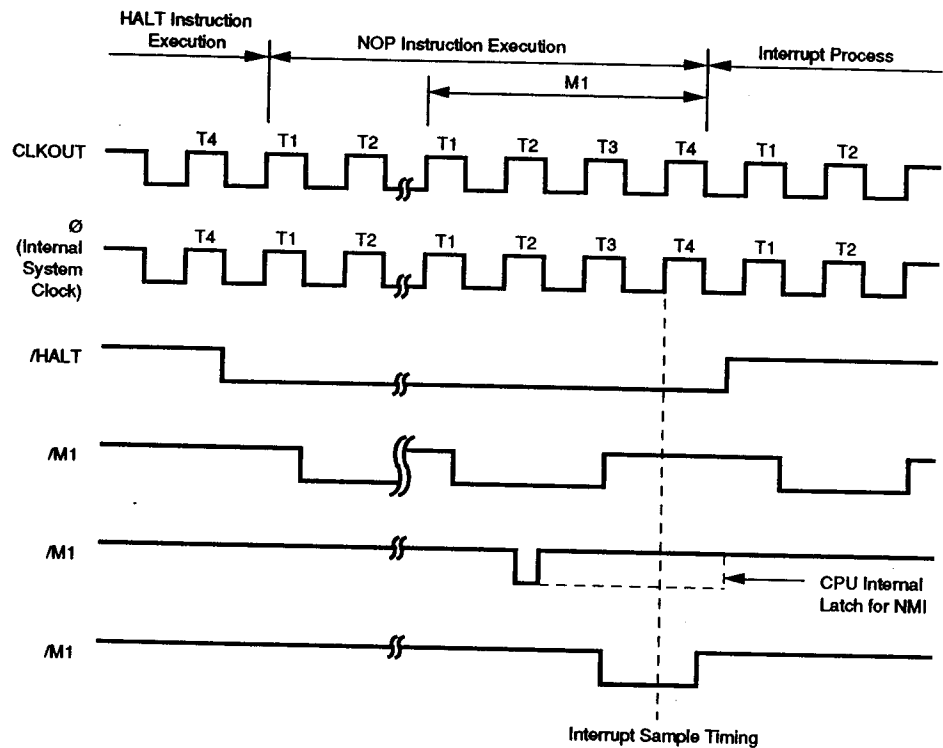
Bit 1-0. I/O Wait states. This 2-bit field specifies the number of wait states to be inserted during I/O transactions.

- 00 - No Wait states
- 01 - 2 Wait states
- 10 - 4 Wait states
- 11 - 6 Wait states

For fifteen /M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the 16th /M1 signal, unless programmed. For the accesses to the on-chip I/O registers, no Wait states are inserted regardless of the programming of this field.

Memory Wait Boundary Register (MWBR, Control Register 01h)

This register specifies the address range to insert memory wait states. When accessed memory addresses are within this range, the Memory Wait State generator inserts Memory Wait States specified in the Memory Wait field of WCR (Figure 28).



**Figure 35. Halt Release Operation Timing
By Interrupt Request Signal In RUN Mode**

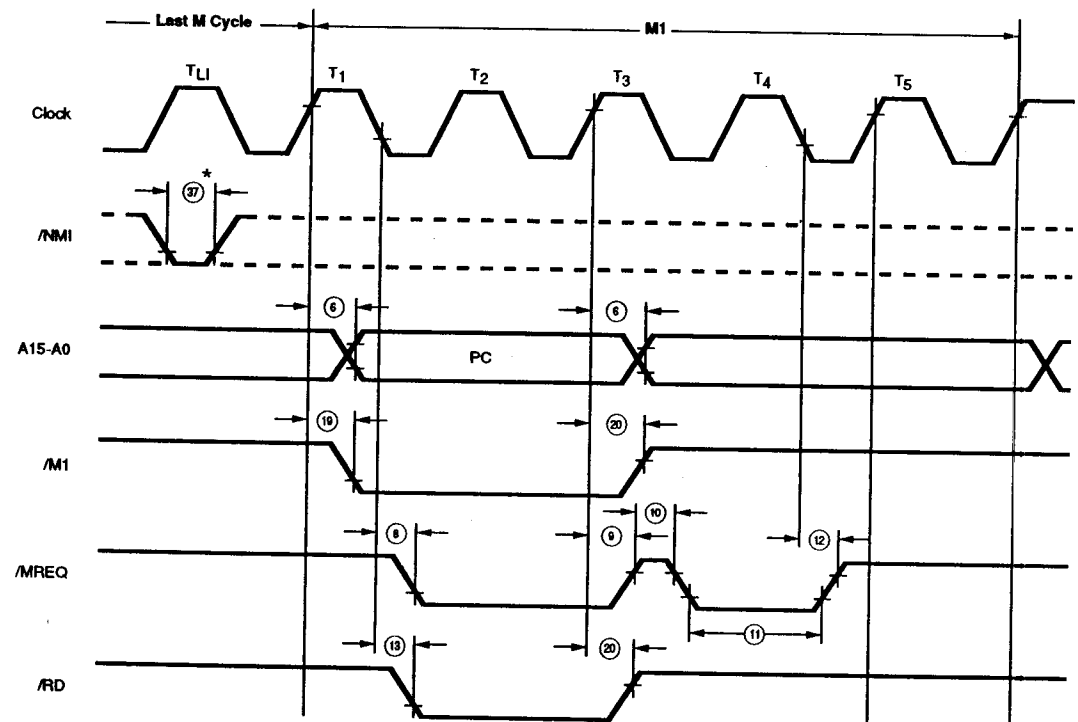
In RUN Mode the internal system clock is not stopped. If the interrupt signal is recognized on the rising clock edge of T4 of the continued NOP instruction, CPU will execute the interrupt process from the next cycle.

The halt release resets CPU in RUN Mode (Figure 36). After reset, CPU will execute an instruction starting from address 0000H. However, in order to reset the CPU it is

necessary to keep /RESET signal at "0" for at least 3 system clock cycles. (For Z84C13/C15: 3 clock cycles if Reset output is disabled.) In addition, if /RESET signal becomes "1", after the dummy cycle for at least two T states, CPU executes an instruction from address 0000H.

Non-Maskable Interrupt Request Cycle. /NMI is sampled at the same time as the maskable interrupt input /INT, but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal

memory read operation except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the /NMI service routine located at the address 0066H (Figure 45).

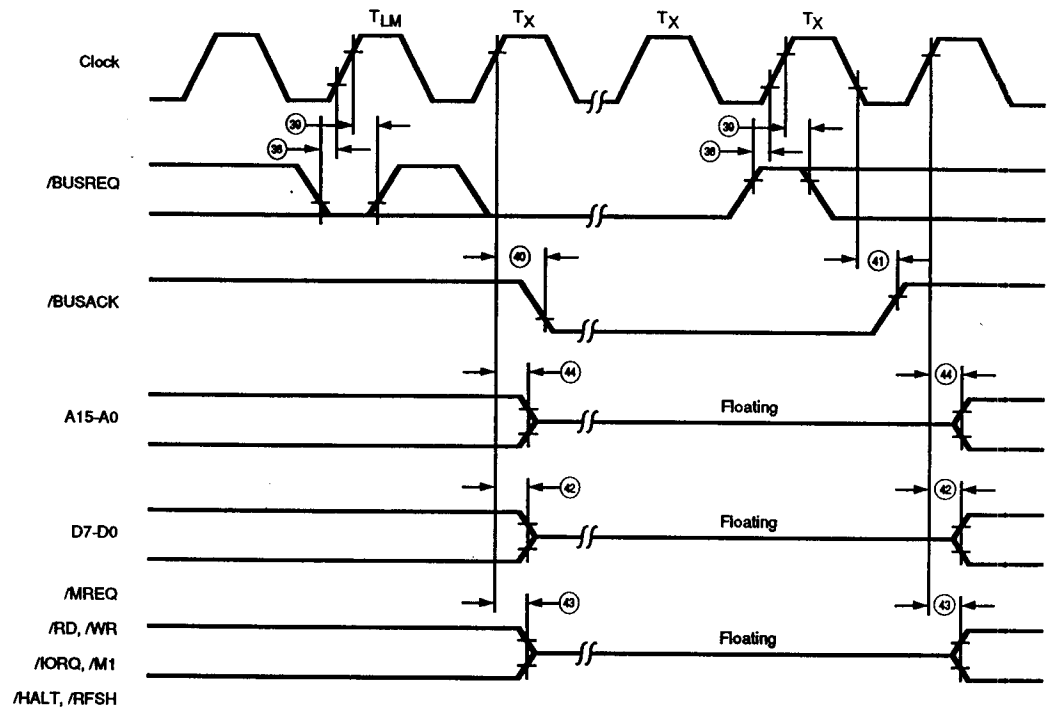


* Although /NMI is an asynchronous input, to guarantee its being recognized on the following machine cycle, /NMI's falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{LI}).

Figure 45. Non-Maskable Interrupt Request Operation
(See Table A)

Bus Request/Acknowledge Cycle. The CPU samples $\overline{\text{BUSREQ}}$ with the rising edge of the last clock period of any machine cycle (Figure 46). If $\overline{\text{BUSREQ}}$ is active, the CPU sets its address, data, and $\overline{\text{MREQ}}$ to Inputs, and $\overline{\text{IORQ}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ lines set to an input for on-chip

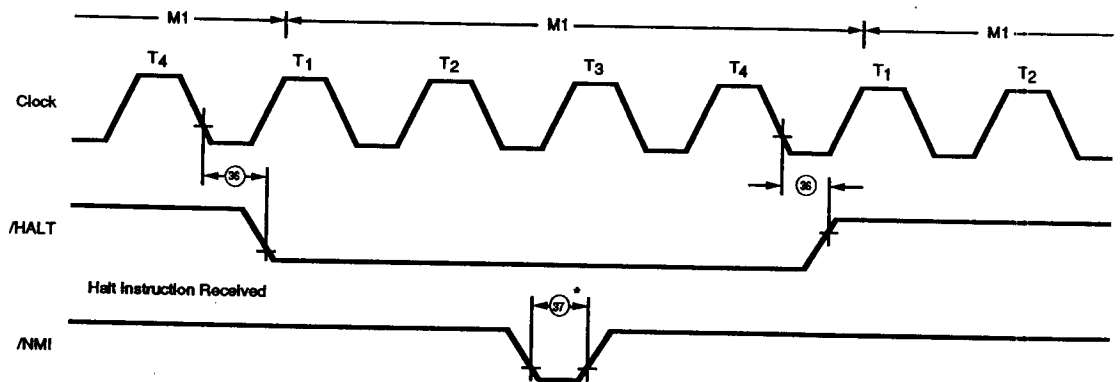
peripheral access from an external bus master with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.



- Notes:
- 1) T_{LM} = Last state of any M cycle
 - 2) T_X = An arbitrary clock cycle used by requesting device

Figure 46. BUS Request/Acknowledge Cycle
(See Table A)

Halt acknowledge cycle. Figure 47 shows the timing for Halt acknowledge cycle.



* Although /NMI is an asynchronous input, to guarantee its being recognized on the following machine cycle, /NMI's falling edge must occur no later than the rising edge of the clock preceding the last state of any instruction cycle (T_{L1}).

Figure 47. Halt Acknowledge
(See Table A)

Reset Cycle. /RESET must be active for at least three clock cycles for the CPU to properly accept it. As long as /RESET remains active, the address and data buses float, and the control outputs are inactive.

Once /RESET goes inactive, two internal T cycles are consumed before the CPU resumes normal processing operation. /RESET clears the PC register, so the first op-code fetch location is 0000H (Figure 48).

Z84C13/C15 Only. If Reset output is disabled, /RESET must be active for at least three clock cycles for the CPU to properly accept it. Otherwise, /RESET must be active for at least two clock cycles and the on-chip reset circuit extends /RESET signal to at least a minimum of 16-clock cycles.

CGC TIMING

Figure 49 to Figure 52 shows the timing related CGC and Power-On Reset circuit.

Parameters referenced in Figure 49 thru Figure 52 appear in Table B.

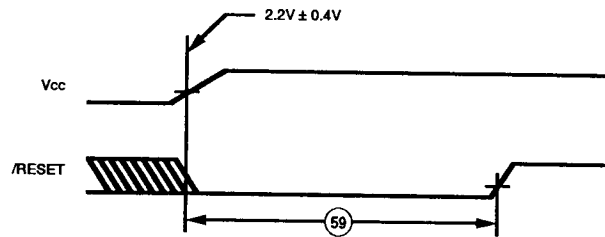


Figure 49. Reset on Power-up (Applies only for Z84C13/C15)
(See Table B)

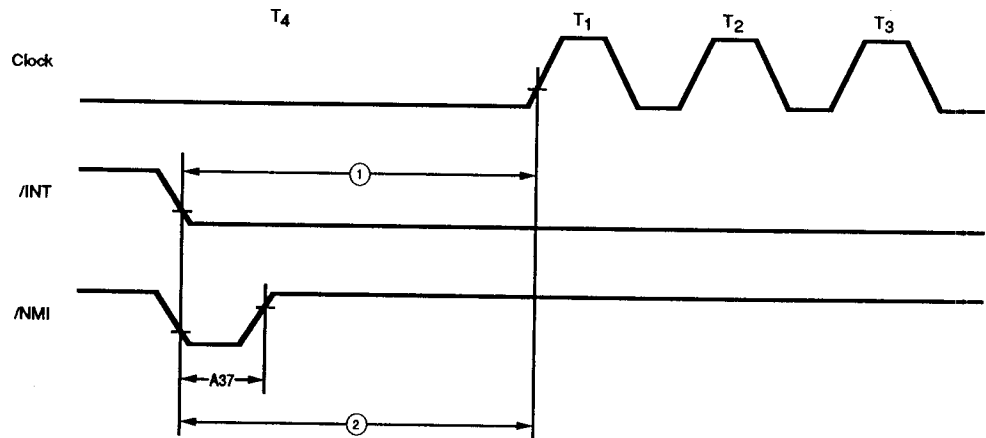
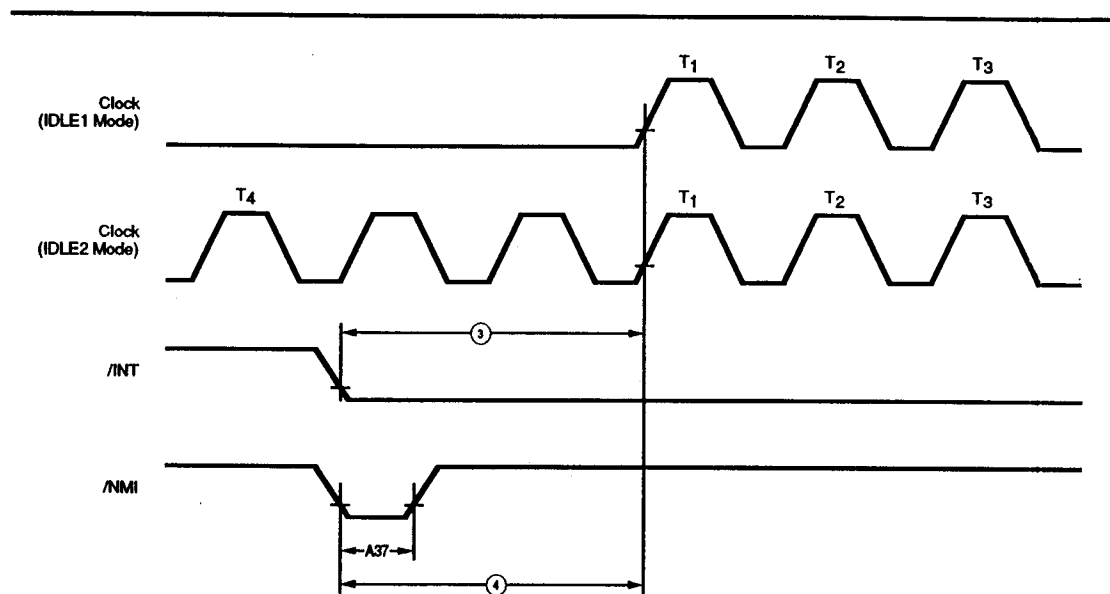
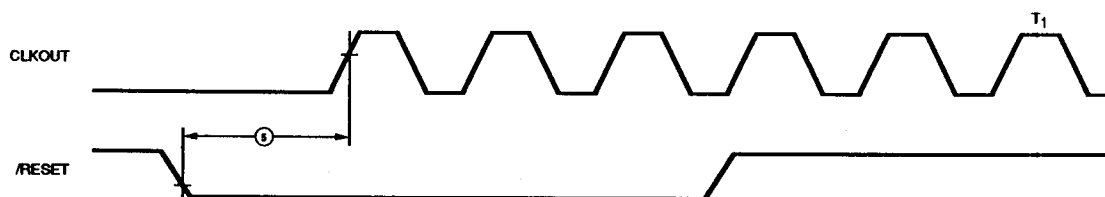


Figure 50. Clock Restart Timing by $\overline{\text{INT}}$, $\overline{\text{NMI}}$ (STOP Mode)
(See Table B)

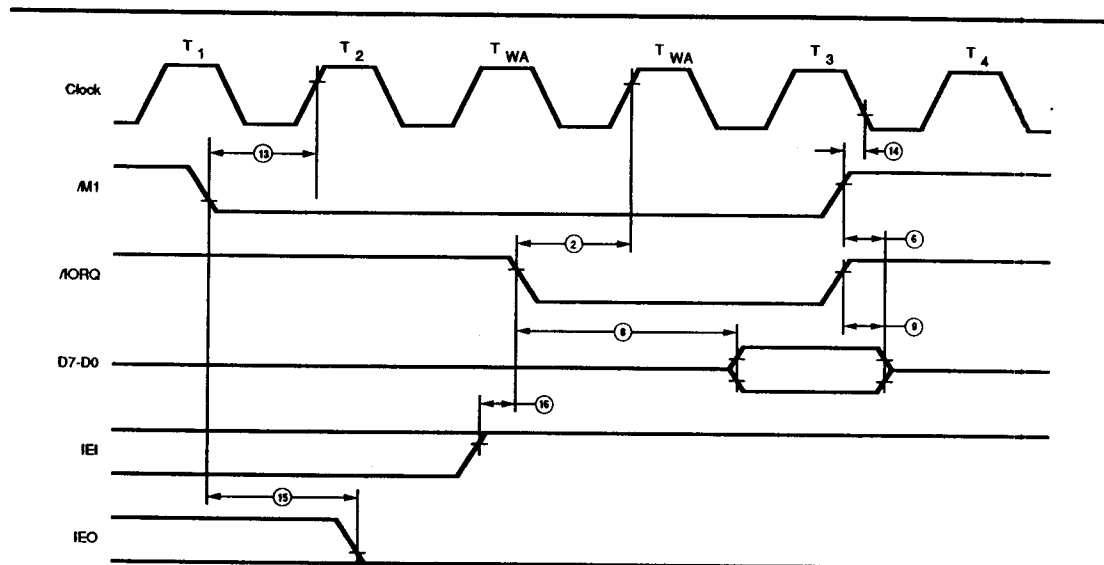


(a) Clock Restart Timing by $\overline{\text{INT}}$, $\overline{\text{NMI}}$ (IDLE1/2 Mode)

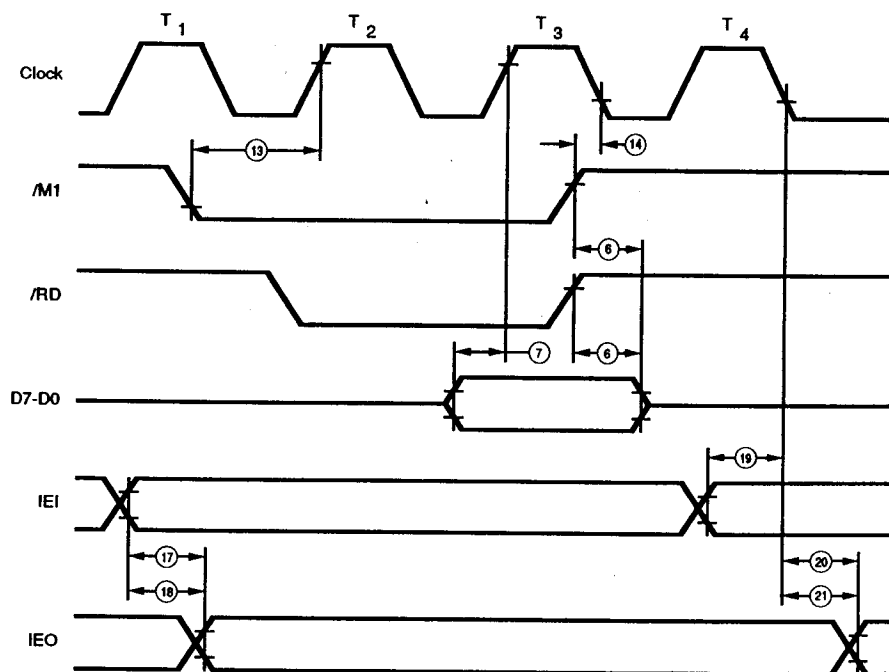


(b) Clock Restart Timing by $\overline{\text{RESET}}$ (IDLE 1/2 Mode)

Figure 51. Clock Restart Timing (IDLE1/2 Mode)
(See Table B)



(b) Interrupt Acknowledge Cycle Timing for On-chip peripheral from External Bus master
(See Table C)



(c) Op-code fetch Cycle Timing for On-chip peripheral from External Bus master
(See Table C)

Figure 53. On-chip Peripheral Timing from External Bus master (Continued)

PIO timing

(Not applicable on Z84x13) Figure 54 shows the timing for on-chip PIO.

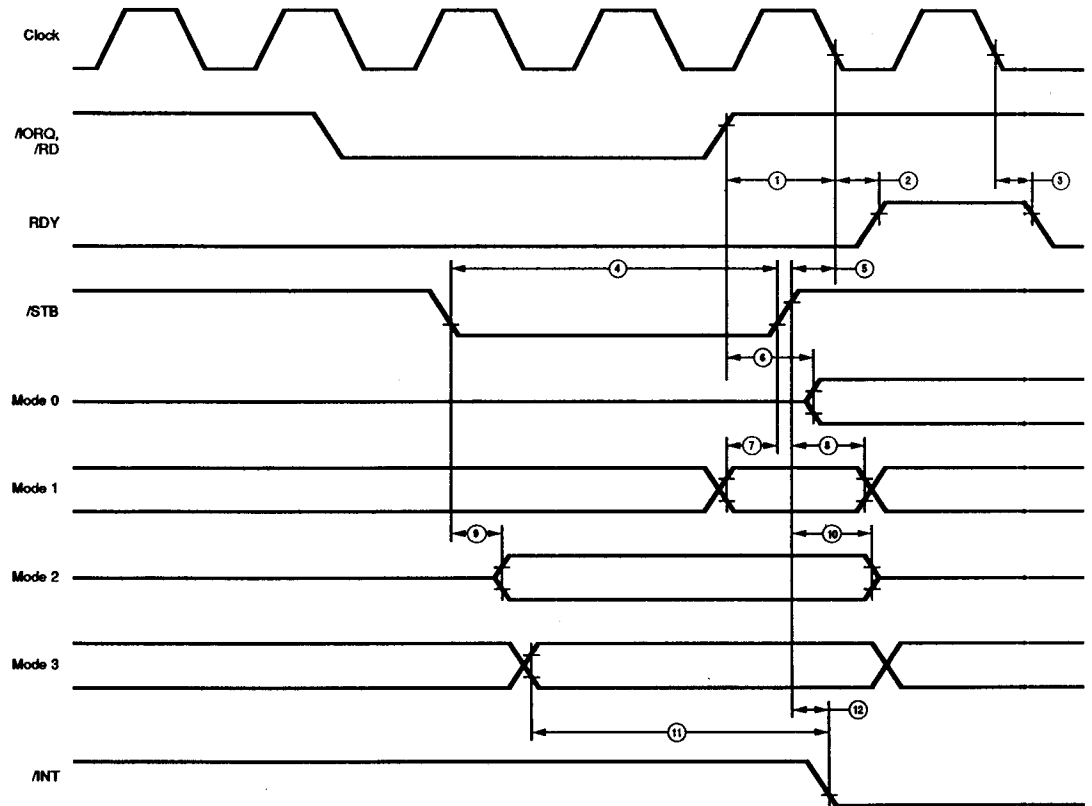


Figure 54. PIO Timing
(See Table D)

CTC Timing

Figure 55 shows the timing for on-chip CTC.

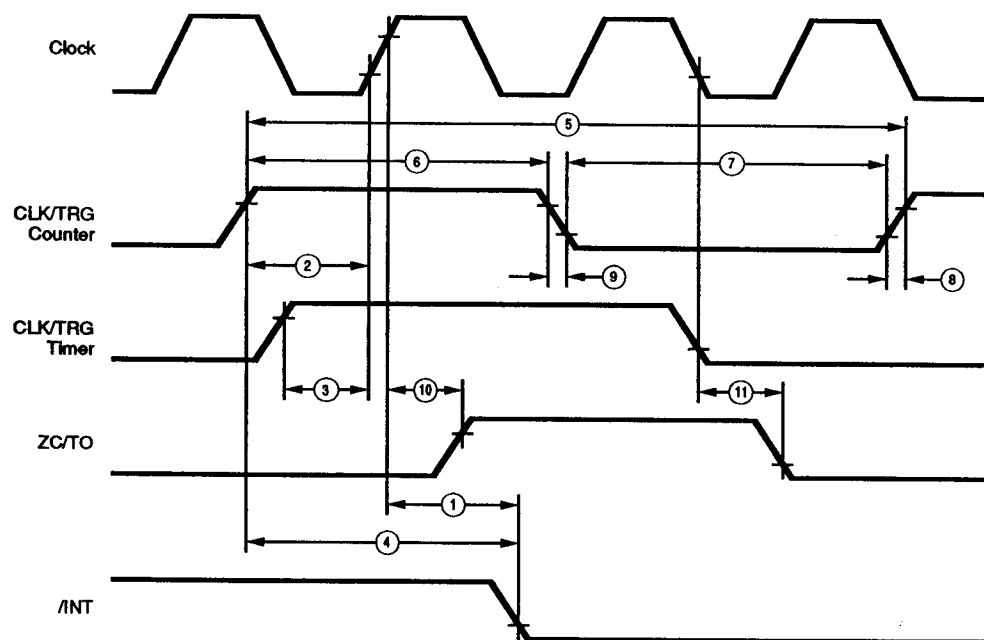


Figure 55. Counter/Timer Timing
(See Table E)

SIO Timing

Figure 56 shows the timing for on-chip SIO.

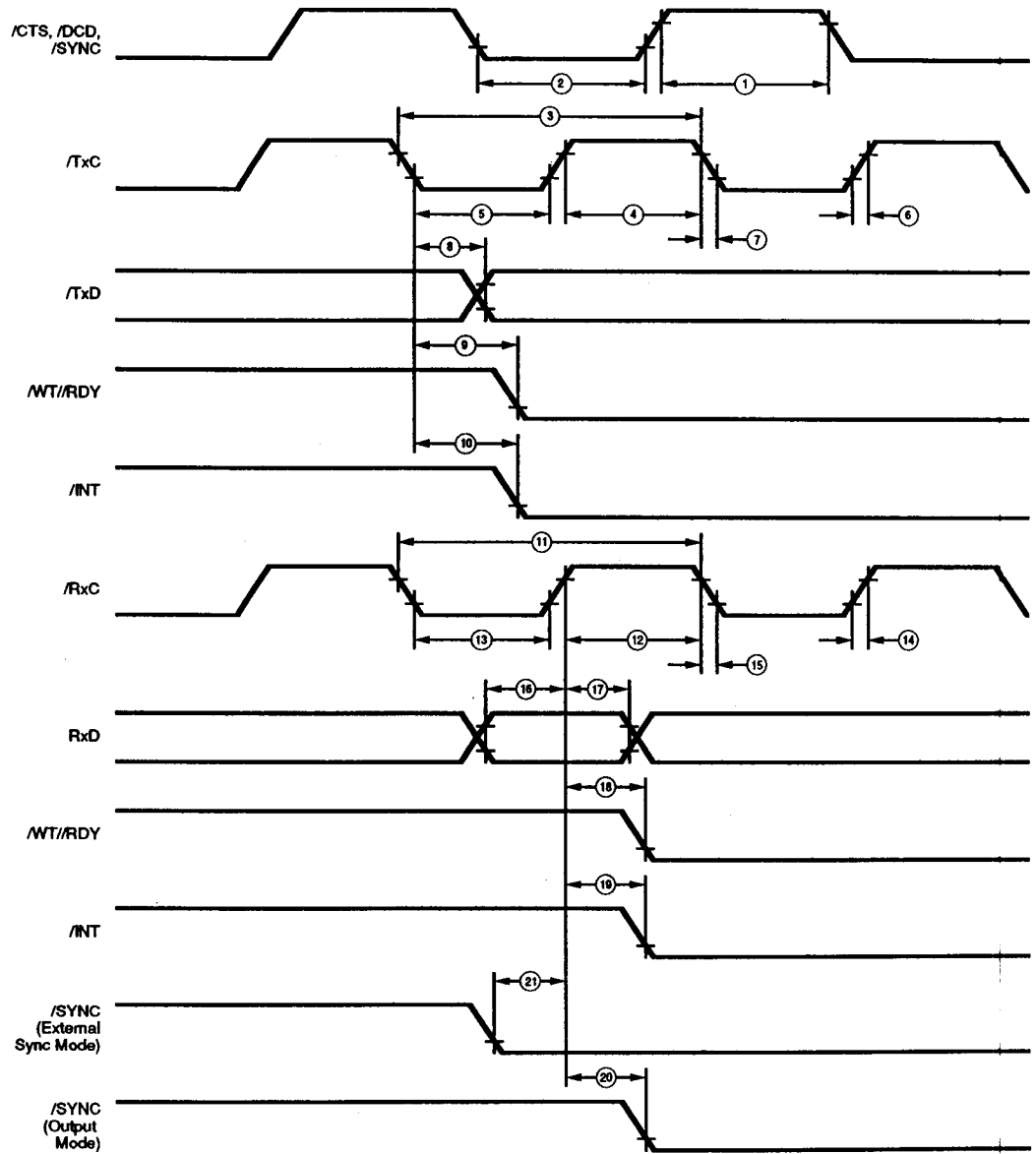


Figure 56. SIO Timing
(See Table F)

AC CHARACTERISTICS

Table A. CPU Timing (See Figure 41 to 48)

No	Symbol	Parameter	Z84X1306 Z84X1506		Z84X1310 Z84X1510		Z84C1316* Z84C1516		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	TcC	Clock Cycle time	162**	DC	100**	DC	61	DC	nS	[A1]
2	TwCh	Clock Pulse Width (High)	65	DC	40	DC	20	DC	nS	[A1]
3	TwCl	Clock Pulse Width (Low)	65	DC	40	DC	20	DC	ns	[A1]
4	TfC	Clock Fall time		20		10		6	ns	[A1]
5	TrC	Clock Rise time		20		10		6	ns	[A1]
6	TdCr(A)	Address Valid from Clock Rise		90		65		55	ns	
7	TdA(MREQf)	Address Valid to /MREQ Fall	35**		0**		-15		ns	
8	TdCf(MREQf)	Clock Fall to /MREQ Fall Delay		70		55		40	ns	
9	TdCr(MREQr)	Clock Rise to /MREQ Rise Delay		70		55		40	ns	
10	TwMREQh	/MREQ Pulse Width (High)	65**		30**		10		ns	[A2]
11	TwMREQl	/MREQ Pulse Width (Low)	132**		75**		25		ns	[A2]
12	TdCf(MERQr)	Clock Fall to /MREQ Rise Delay		70		55		40	ns	
13	TdCf(RDf)	Clock Fall to /RD Fall Delay		80		65		40	ns	
14	TdCr(RDr)	Clock Rise to /RD Rise Delay		70		55		40	ns	
15	TsD(Cr)	Data Setup Time to Clock Rise	30		25		10		ns	
16	ThD(RDr)	Data Hold Time After /RD Rise	0		0		0		ns	
17	TsWAIT(Cf)	/WAIT Setup Time to Clock Fall	60		20		75		ns	
18	ThWAIT(Cf)	/WAIT Hold Time After Clock Fall	10		10		10		ns	
19	TdCr(M1f)	Clock Rise to /M1 Fall Delay		80		65		40	ns	
20	TdCr(M1r)	Clock Rise to /M1 Rise Delay		80		65		40	ns	
21	TdCr(RFSHf)	Clock Rise to /RFSH Fall Delay		110		80		60	ns	
22	TdCr(RFSHr)	Clock Rise to /RFSH Rise Delay		100		80		60	ns	
23	TdCf(RDr)	Clock Fall to /RD Rise Delay		70		55		40	ns	
24	TdCr(RDf)	Clock Rise to /RD Fall Delay		70		55		40	ns	
25	TsD(Cf)	Data Setup to Clock Fall During M2, M3, M4 or M5 Cycles	40		25		12		ns	
26	TdA(IORQf)	Address Stable Prior to /IORQ Fall	107**		50**		0		ns	
27	TdCr(IORQf)	Clock Rise to /IORQ Fall Delay		65		50		40	ns	
28	TdCf(IORQr)	Clock Fall to /IORQ Rise Delay		70		55		40	ns	
29	TdD(WRf)	Data Stable Prior to /WR Fall	22**		40**		-10		ns	
30	TdCf(WRf)	Clock Fall to /WR Fall Delay		70		55		40	ns	
31	TwWR	/WR Pulse Width	132**		75**		25		ns	
32	TdCf(WRr)	Clock Fall to /WR Rise Delay		70		55		40	ns	
33	TdD(WRf)IO	Data Stable Prior to /WR Fall	-55**		-10**		-30		ns	
34	TdCr(WRf)	Clock Rise to /WR Fall Delay		60		50		40	ns	
35	TdWRr(D)	Data Stable from /WR Fall	30**		10**		0	0	ns	
36	TdCf(HALT)	Clock Fall to /HALT 0 or 1		260		90		70	ns	
37	TwNMI	/MNI pulse Width	60		60		60		ns	
38	TsBUSREQ(Cr)	/BUSREQ Setup Time to Clock Rise	50		30		15		ns	
39	ThBUSREQ(Cr)	/BUSREQ Hold Time after Clock Rise	10		10		10		ns	
40	TdCr(BUSACKf)	Clock Rise to /BASACK Fall Delay		90		75		40	ns	

Table H. Footnote to Table A.					
No	Symbol	Parameter	Z84X1306 Z84X1506	Z84X1310 Z84X1510	Z84C1316* Z84C1516
1	TcC	TwCh + TwCl + TrC + TfC			
7	TdA(MREQf)	TwCh + TfC	-50	-50	-45
10	TwMREQh	TwCh + TfC	-20	-20	-20
11	TwMREQl	TcC	-30	-25	-25
26	TdA(IORQf)	TcC	-55	-50	-50
29	TdD(WRf)	TcC	-140	-60	-60
31	TwWR	TcC	-30	-25	-25
33	TdD(WRf)	TwCl + TrC	-140	-60	-60
35	TdWRr(D)	TwCl + TrC	-55	-40	-25
45	TdCTr(A)	TwCl + TrC	-50	-30	-30
50	TdM1f(IORQf)	2TcC + TwCh + TfC	-50	-30	-30