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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	Z80
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z84c1510feg

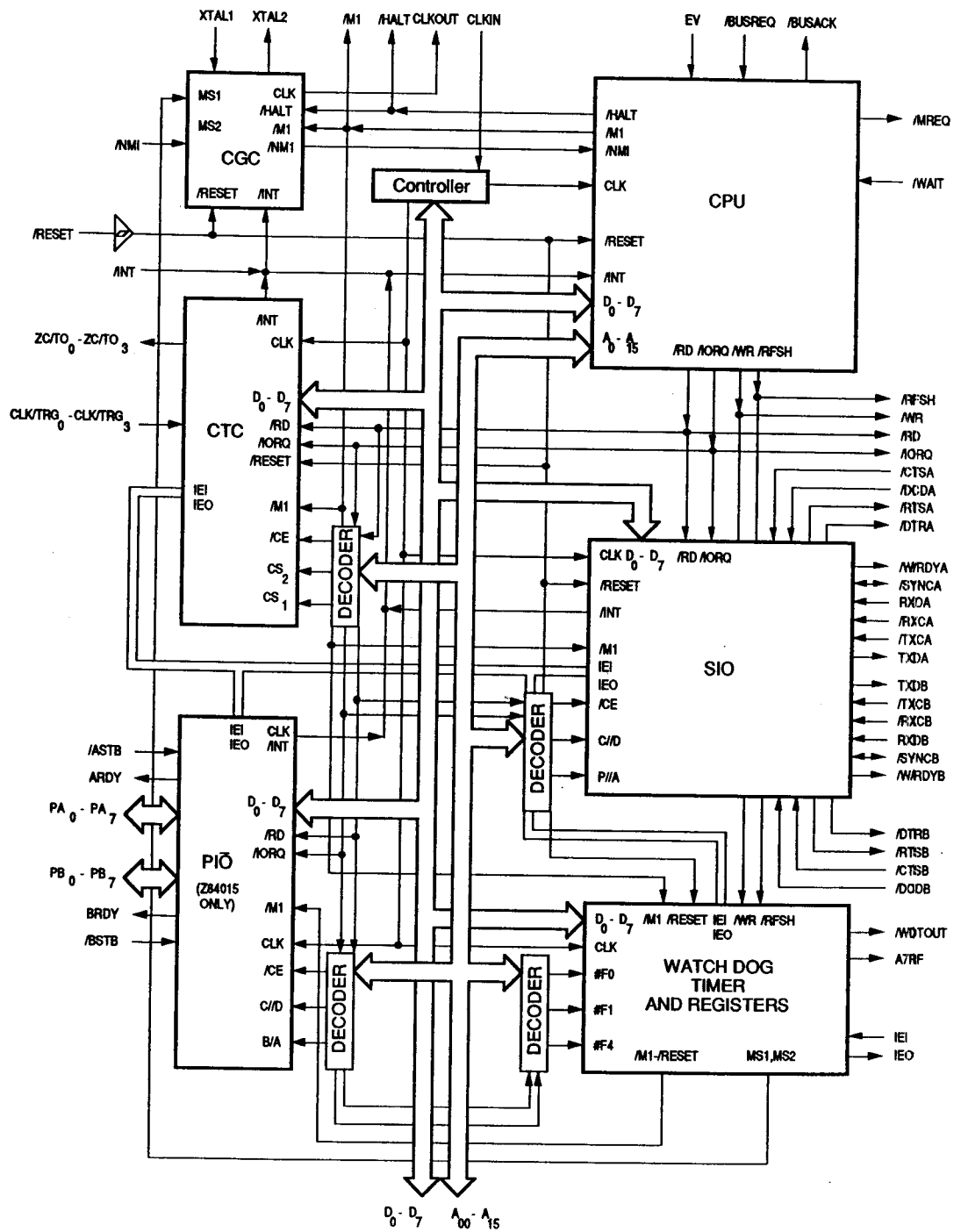


Figure 5(a). Block Diagram for 84013/015 IPC

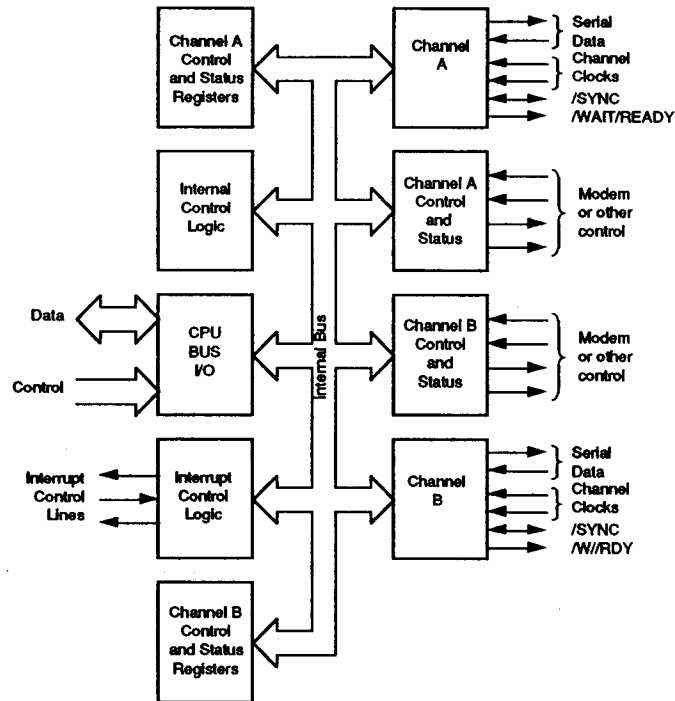


Figure 8. SIO Block Diagram

Watch Dog Timer (WDT) Logic Unit

This logic unit has been superintegrated into the IPC. It detects an operation error, caused by the program run-away, and returns to normal operation. Figure 9, shows the block diagram of the WDT. Upon Power-On Reset, this unit is enabled. If WDT is not required, but /WDTOUT is connected to /RESET or any other circuit, it has to be disabled. During the power-down mode of operation (either IDLE1/2 or Stop), the Watch Dog Timer is halted.

WDT Output (/WDTOUT pin). When the WDT is used, the "0" level signal is output from the /WDTOUT pin after a duration of time specified in the WDTP or in the WDTMR. The output pulse width is one of the following, depending on the /WDTOUT pin connection.

- The /WDTOUT is connected to the /RESET pin: The "0" level is pulsed for 5T_{cC} (System clock cycles).
- The /WDTOUT is connected to a pin other than the /RESET pin: The "0" level is kept until the Watch Dog timer is cleared by software, or reset by /RESET pin.

CGC Logic Unit. The IPC has CGC (Clock Generator/Controller) unit. This unit is identical to the one with the Z84C01 and the Z84C50, and supports power-down modes of operation. The output from this unit is on the pin called CLKOUT, and is not connected to the system clock internally. The CLKIN pin is the system clock input. The user can connect CLKOUT to CLKIN to utilize this CGC unit, or supply external clock from CLKIN pin.

The CGC unit allows crystal input (XTAL1, XTAL2) or External Clock input on the XTAL1 pin. It has clock divide-by-two circuits and generates a half-speed clock to the input.

Z84C13/C15. The power-down modes of the IPC vary depending upon whether the system clock is fed from the CGC unit (tie CLKOUT to CLKIN) or the external clock source on the CLKIN pin. They also have divide-by-one Mode. If the clock is supplied by this CGC unit, all of the modes in "halt" state are available. When external clock is provided on the CLKIN pin, XTAL1 is not left open (tied to "0" or "1") to avoid meta-stable conditions to minimize power consumption.

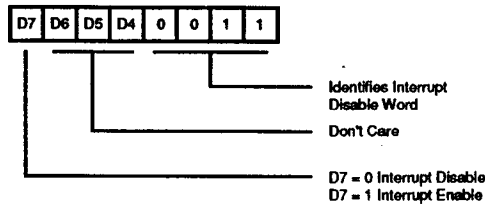


Figure 16. Interrupt Disable Word

CTC CONTROL REGISTERS

For more detailed information, refer to the CTC Technical Manual.

Channel Control Word

This word sets the operating modes and parameters as described below. Bit D0 is a "1" to indicate that this is a Control Word (Figure 17).

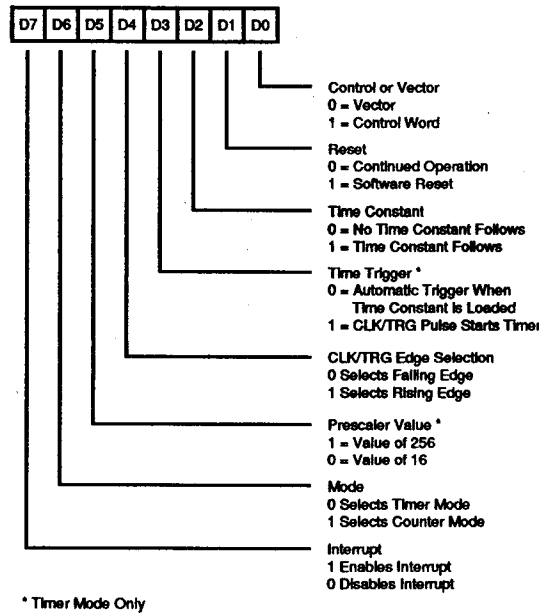


Figure 17. CTC Channel Control Word

Bit D7. Interrupt Enable. This bit enables the interrupt logic so that an internal INT can be generated at zero count. Interrupts are programmed in either mode and may be enabled or disabled at any time.

Bit D6. Mode Bit. This bit selects either Timer Mode or Counter Mode.

Bit D5. Prescaler Factor. This bit selects the prescaler factor for use in the timer mode. Either divide-by-16 or divide-by-256 is available.

Bit D4. Clock/Trigger Edge Selector. This bit selects the active edge of the CLK/TRG input pulses.

Bit D3. Timer Trigger. This bit selects the trigger mode for timer operation. Either automatic or external trigger may be selected.

Bit D2. Time Constant. This bit indicates that the next word programmed is time constant data for the downcounter.

Bit D1. Software Reset. Writing 1 to this bit indicates a software reset operation, which stops counting activities until another time constant word is written.

Time Constant Word

Before a channel starts counting, it must receive a time constant word. The time constant value is anywhere between 1 and 256, with "0" being accepted as a count of 256 (Figure 18).

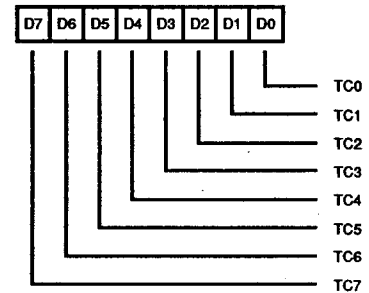


Figure 18. CTC Time Constant Word

Interrupt Vector Word

If one or more of the CTC channels have interrupt enabled, then the Interrupt Vector Word must be programmed. Only the five most significant bits of this word are programmed, and bit D0 must be "0". Bits D2-D1 are automatically modified by the CTC channels when it responds with an interrupt vector (Figure 19).

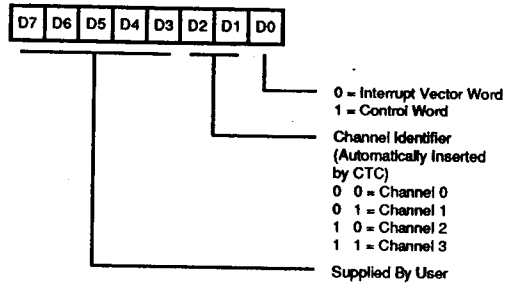
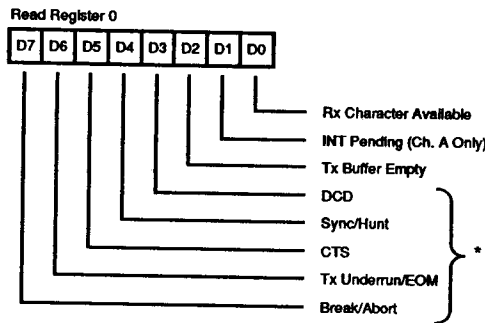


Figure 19. CTC Interrupt Vector Word

SIO REGISTERS

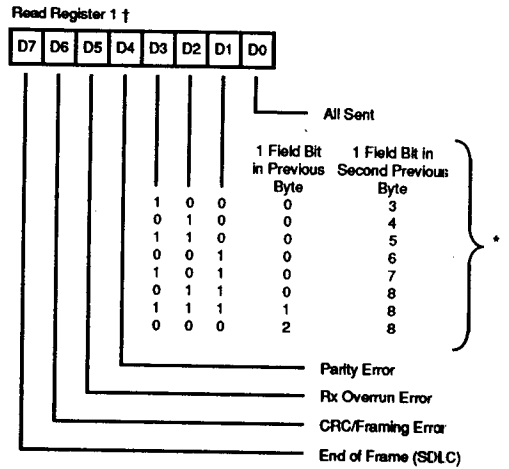
For more detailed information, refer to the SIO Technical Manual.

Read Registers. The SIO channel B contains three read registers while channel A contains only two that are read to obtain status information. To read the contents of a register (rather than RR0), the program must first write a pointer to WR0 in exactly the same manner as a write operation. The next I/O read cycle will place the contents of the selected read registers onto the data bus (Figure 20a, b, c).



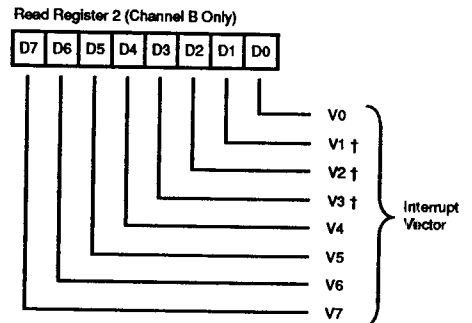
* Used With "External/Status Interrupt" Modes

Figure 20a. SIO Read Register 0



* Residue data for eight Rx bits/character programmed
† Used with special receive condition mode

Figure 20b. SIO Read Register 1



† Variable if "Status Affects Vector" is programmed

Figure 20c. SIO Read Register 2

Write Registers. The SIO Channel B contains eight write registers while Channel A contains only seven that are programmed to configure the operating mode characteristics of each channel. With the exception of WR0, programming the write registers is a two step operation. The first operation is a pointer written to WR0 which points to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel (Figure 21).

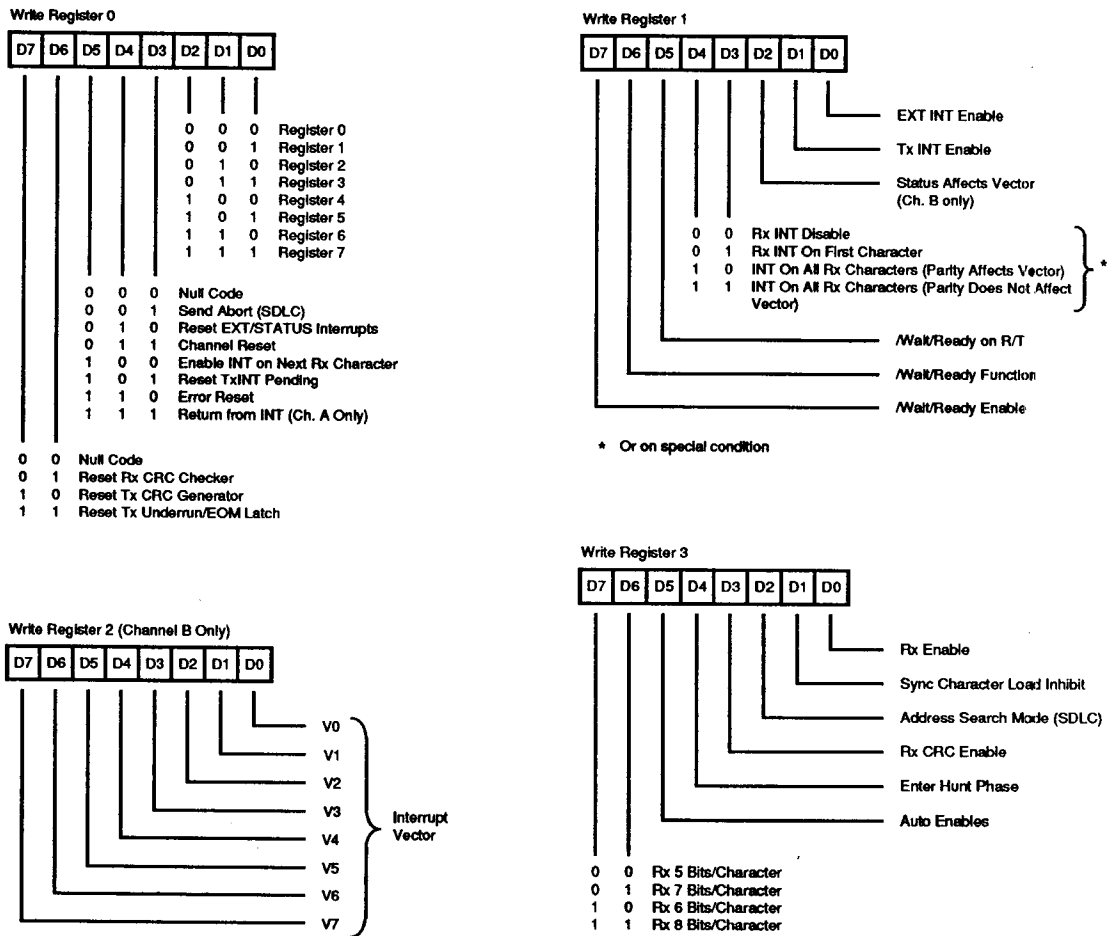


Figure 21. SIO Write Registers

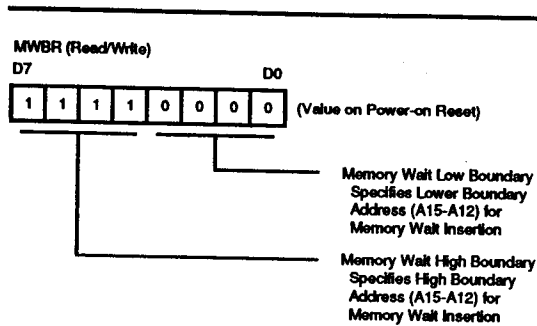


Figure 28. Memory Wait Boundary Register

Bit D7-D4. Memory Wait High Boundary. This field specifies A15-A12 of the upper address boundary for Memory Wait.

Bit D3-D0. Memory Wait Low Boundary. This field specifies A15-12 of the lower address boundary for Memory Wait.

Memory Wait states are inserted for the address range:

$$(D7-D4 \text{ of MWBR}) \geq A15-A12 \geq (D3-D0 \text{ of MWBR})$$

This register is set to "F0h" on Power-on Reset, which specifies the address range for Memory Wait as "0000h to FFFFh".

Chip Select Boundary Register (CSBR, Control Register 02h)

This register specifies the address range for each chip select signal. When accessed memory addresses are within this range, chip select signals are active (Figure 29).

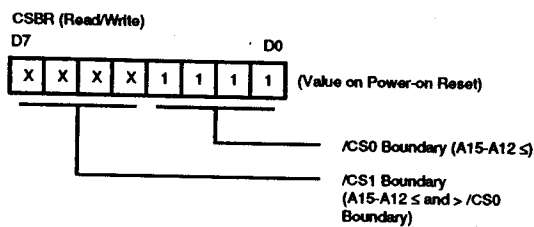


Figure 29. Chip Select Boundary Register

D7-D4. /CS1 Boundary Address. These bits specify the boundary address range for /CS1. The bit values are ignored on power-up as the /CS1 enable bit is off. The /CS1 is asserted if the address lines A15-12 have an address value greater than the programmed value for /CS0, and less than or equal to the programmed value in these bits.

D3-D0. /CS0 Boundary Address. These bits specify the boundary address range for /CS0. /CS0 is asserted if the address lines A15-12 have an address value less than or equal to the programmed boundary value. The /CS0 enable bit in the MCR must be set to 1. Upon Power-up reset, these bits come up as all 1's so that /CS0 is asserted for all addresses.

Chip Select signals are active for the address range:

$$\begin{aligned} /CS0: (D3-D0 \text{ of CSBR}) \geq A15-A12 \geq 0 \\ /CS1: (D7-D4 \text{ of CSBR}) \geq A15-A12 > (D3-D0 \text{ of CSBR}) \end{aligned}$$

This register is set to "xxxx1111b" on Power-on Reset, which specifies the address range of /CS0 for "0000h to FFFFh" (all Memory location) and /CS1 "undefined."

Misc Control Register (MCR, Control Register 03h)

This register specifies miscellaneous options on this device (Figure 30).

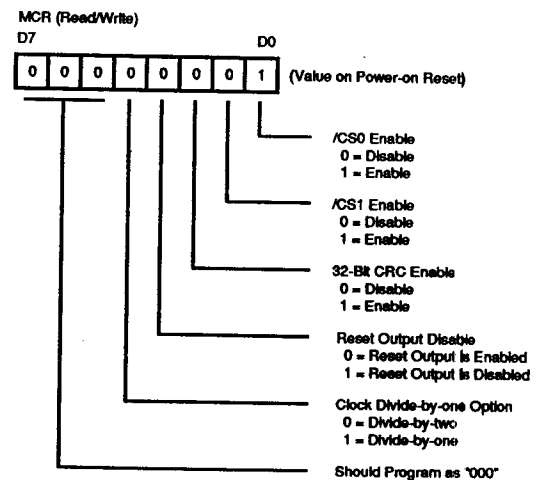


Figure 30. Misc Control Register

Bit D7-D5. Reserved. These three bits are reserved and are always programmed as "000".

Bit D4. Clock Divide-by-one option. "0"-Disable, "1"-enable. On-chip CGC unit has divide-by-two circuit. By setting this bit to one, this circuit is bypassed and CLKOUT is equal to X'tal oscillator frequency (or external clock input on the XTAL1 pin). This bit has no effect when the on-chip CGC unit is not in use and the external system clock is fed from CLKIN pin. Upon Power-on Reset, this bit is cleared to 0 and the clock is divided by two.

Table 3. Device status in Halt state
(When using on-chip CGC unit; CLKOUT and CLKIN are tied together)

Mode	CGC	CPU	CTC	PIO	SIO	WDT	CLKOUT
IDLE1	O	X	X	X	X	X	X
IDLE2	O	X	O	X	X	X	O
STOP	X	X	X	X	X	X	X
RUN	O	O	O	O	O	O	O

O: Operating
X: Stop

All of the operating modes listed here are valid with crystal input (Crystal connected between XTAL1/2 or external clock input on XTAL1). For the external clock on the CLKIN pin, only the IDLE2 and RUN modes are applicable.

TIMING

Basic Timing

The basic timing is explained here with emphasis placed on the halt function relative to the clock generator. The following items are identical to those for the Z84C00. Refer to the data sheet for the Z84C00.

- Operation code fetch cycle
- Memory Read/Write operation
- Input/Output operation
- Bus request/acknowledge operation
- Maskable interrupt request operation
- Non-Maskable interrupt request operation
- Reset Operation

Operation When HALT Instruction is Executed. When the CPU fetches a halt instruction in the operation code fetch cycle, /HALT goes active (Low) in synch with the falling edge of T4 state before the peripheral LSI and CPU stops the operation. After this, the system clock generation differs depending upon the operation mode (RUN Mode, IDLE1/2 Mode or STOP Mode). If the internal system clock is running, the CPU continues to execute NOP instruction even in the halt state.

RUN Mode (HALTM = 11). Shown in Figure 31 is the basic timing when the halt instruction is executed in RUN Mode.

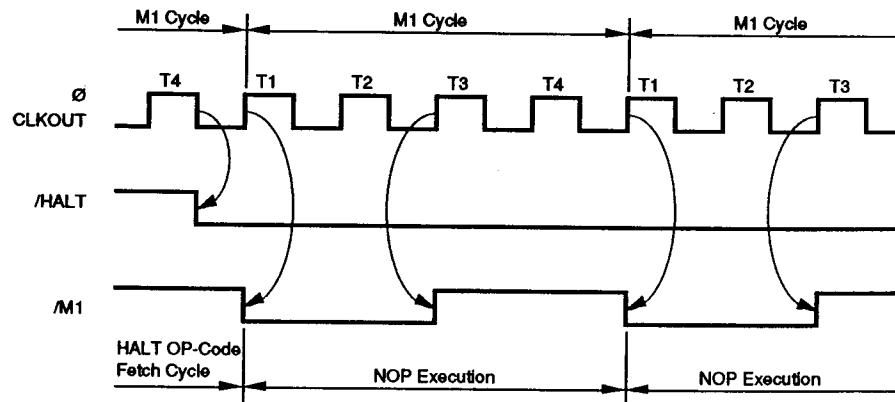


Figure 31. Timing of RUN Mode
(at Halt Instruction Command Execution)

In RUN Mode, output from the CGC unit (CLKOUT) is not stopped and the internal system clock (\emptyset) continues even after the halt instruction is executed. Therefore, until the halt state is released by the interrupt signal (/NMI or /INT)

or /RESET signal, MPU continues to execute HALT instructions (internally executing NOP instructions).

IDLE1 Mode (HALTM=00). Shown in Figure 32 is the basic timing when the halt instruction is executed in IDLE1 Mode.

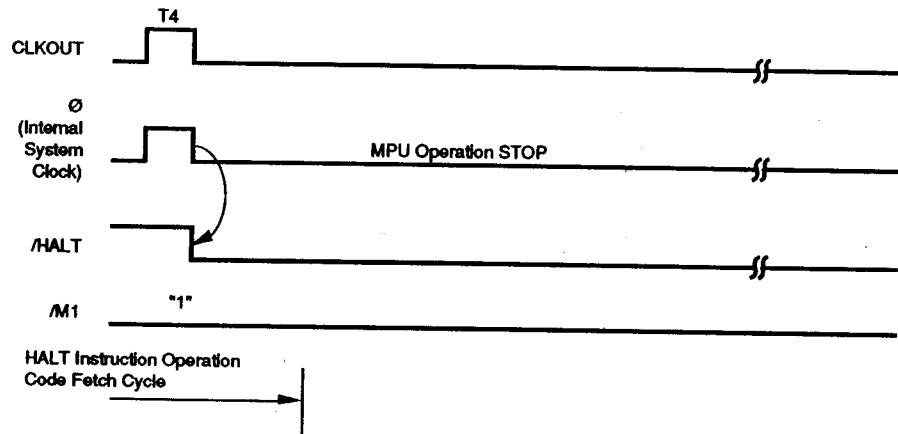


Figure 32. IDLE1 Mode Timing
(At Halt Instruction Execution)

In IDLE1 Mode, the internal oscillator continues to operate, but clock output (CLKOUT) is stopped at T4 Low state of HALT instruction execution. Then all components in the MPU stop their operation. This mode is not supported

when the CGC unit is inactive and the external clock is fed from CLKIN pin; CLKOUT should be connected to CLKIN.

IDLE2 Mode (HALTM=01). Shown in Figure 33 is the basic timing when the halt instruction is executed in IDLE2 Mode.

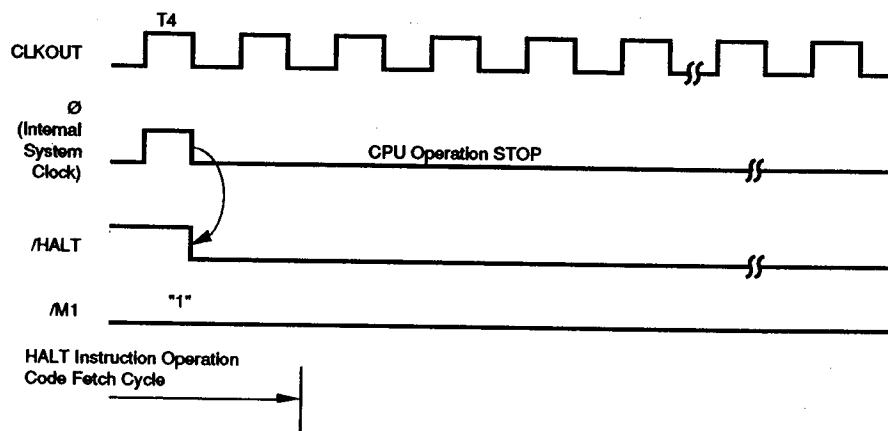


Figure 33. IDLE2 Mode Timing
(At Halt Instruction Execution)

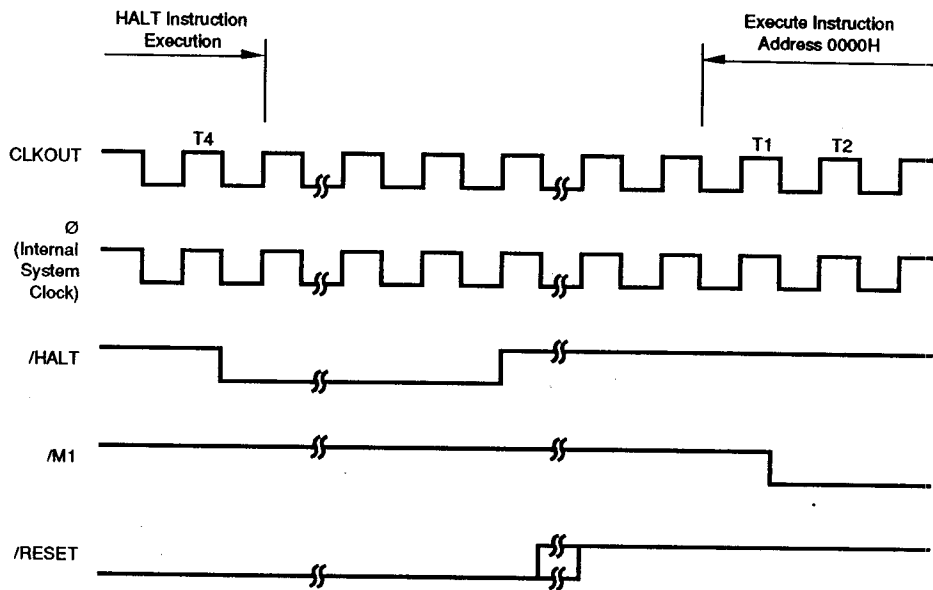


Figure 36. Halt Release Operation Timing By Reset in RUN Mode

IDLE1 Mode (HALTM=00), IDLE2 Mode (HALTM=01). The halt release operation by interrupt signal in IDLE1 Mode is shown in Figure 37 (a) and in IDLE2 Mode in Figure 37 (b).

When /RESET signal at "0" level is input into the IPC, the internal system clock is restarted and the IPC will execute an instruction stored in address 0000H.

Halt release in STOP Mode (HALTM=10) by interrupt. The halt release operation by interrupt signal in STOP Mode is shown in Figure 39.

At time of /RESET signal input, it is necessary to take the same care as that in resetting the IPC in RUN Mode.

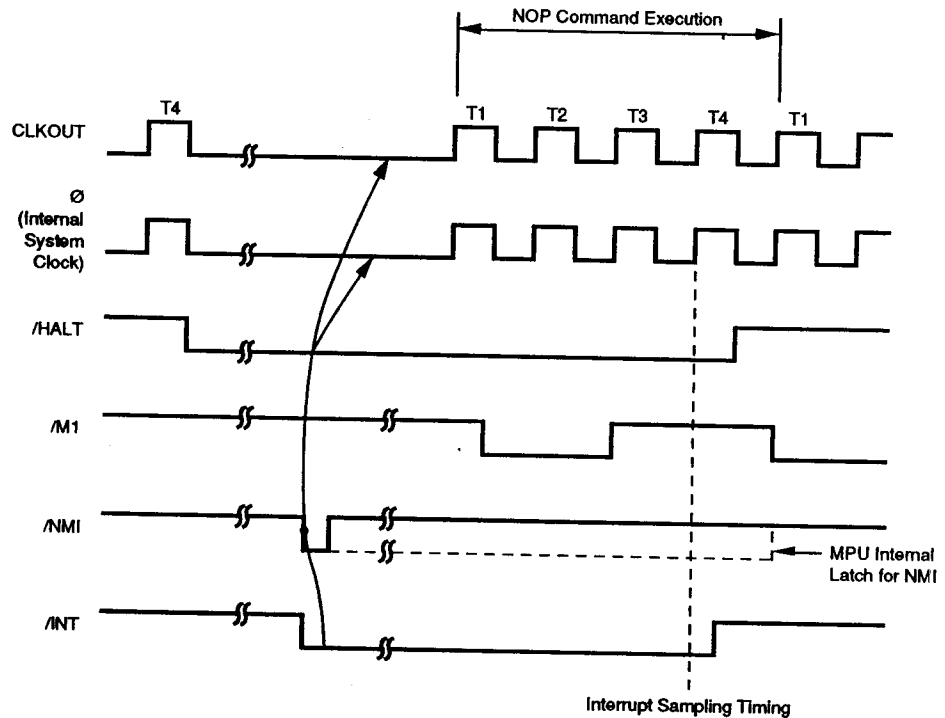


Figure 39. Halt Release Operation Timing By Interrupt Request Signal in STOP Mode

When the IPC receives an interrupt signal, the internal oscillator is restarted. To obtain stabilized oscillation, CLKOUT (and the internal system clock) are started after a start-up time of $(2^{14}+2.5)$ TcC (TcC: Clock Cycle) by the internal counter.

CPU executes one NOP instruction after the internal system clock is restarted. At the same time, it samples an interrupt signal at the rise of T4 state during the execution of this NOP instruction. If the interrupt signal is accepted, CPU executes the interrupt process operation from the next cycle.

During interrupt signal input, it is necessary to take the same care as the interrupt signal input in IDLE1/2 Mode.

Halt release in STOP Mode (HALTM=10) by /RESET. When /RESET at "0" level is input into the IPC, the internal oscillator is restarted. However, the internal clock counter for warm-up does not operate. Therefore, the operation is not carried out properly due to unstable clock oscillation. It is necessary to hold /RESET at "0" level for sufficient time. The halt release operation by the IPC resetting in STOP Mode is shown in Figure 40.

Z84C13/C15 Only. The /RESET pulse is stretched to a minimum of 16 cycles and driven out of the Z84C13/C15 on the /RESET pin if Reset output is enabled (bit D3 of MCR is cleared to "0"). Setting bit D3 disables the driving out of

/RESET. The values in the control registers (WDTMR, SCRIP, WCR, MWBR, CSBR and MCR) are initialized to the default value on /RESET.

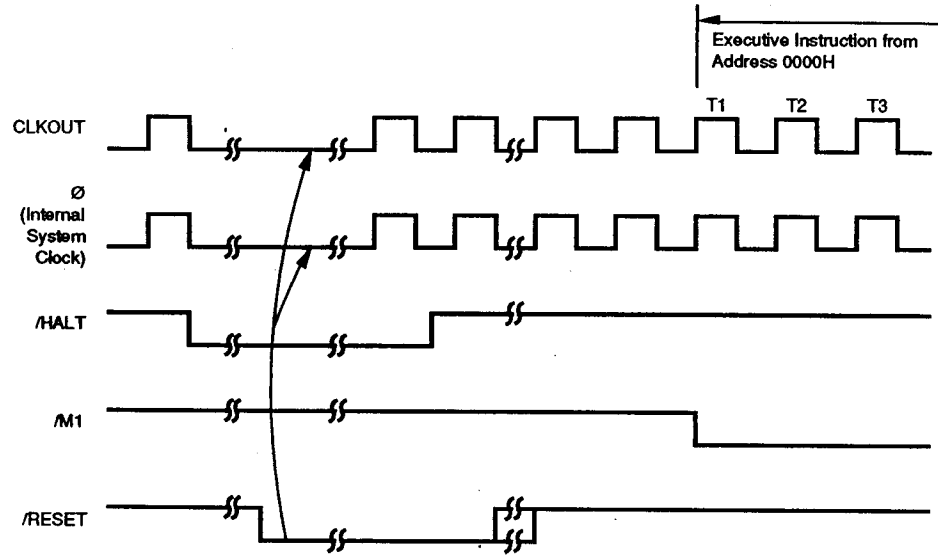


Figure 40. Halt Release Operation Timing By Reset in STOP Mode

Start-up Time at Time of Restart (STOP Mode). When the MPU is released from the halt state by accepting an interrupt request, it executes an interrupt service routine. Therefore, when an interrupt request is accepted, it starts generating clock on the CLKOUT pin, after a start-up time, by the internal counter $[(2^{14} + 2.5) T_{CC}]$ (T_{CC} : Clock Cycle). This obtains a stabilized oscillation for operation.

Further, in case of restart by the /RESET signal, the internal counter does not operate.

Evaluation operation. Each of the CPU signals (A15-0, D7-0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1, /RFSH) can be 3-stated by activating the EV pin. The Z84C13/C15 enhances the counter part by eliminating the requirement of /BUSREQ to go active.

Instruction set. The instruction set of the IPC is the same for the Z84C00. For details, refer to the data sheet of the Z84C00 Technical Manual.

AC TIMING

The following section describes the timing of the IPC. The numbers appearing in the figures refer to the parameters on Table A - F.

CPU Timing

Parameters referenced in Figure 41 through Figure 48 appear in Table A.

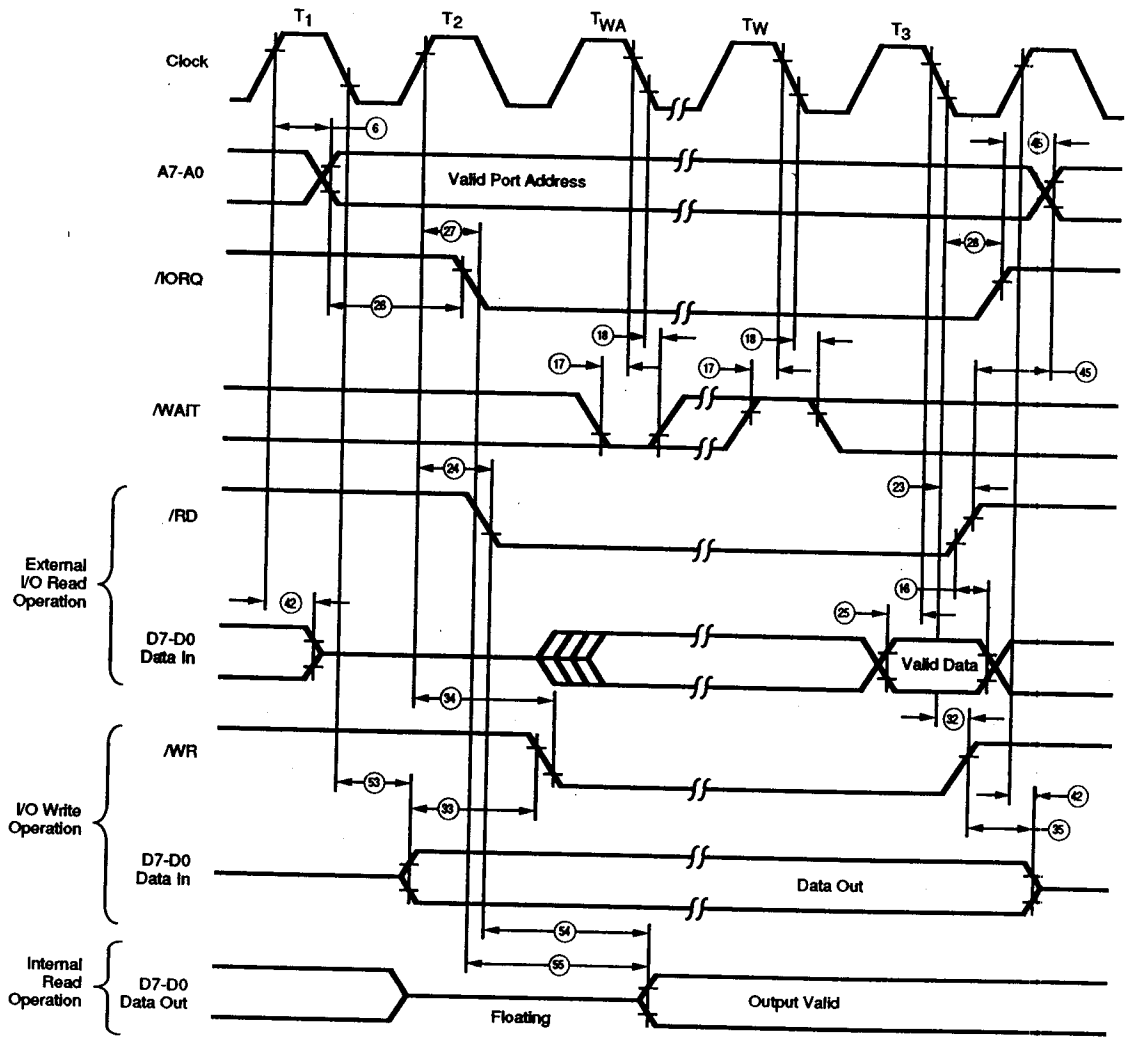
The IPC's CPU executes instructions by proceeding through the following specific sequence of operations:

Memory read or write
I/O device read or write
Interrupt acknowledge

The basic clock period is referred to as a Time or Cycle and three or more T cycles make up a machine cycle (e.g., M1, M2 or M3). Machine cycles are extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

Input or Output Cycles. Figure 43 shows the timing for an I/O read or I/O write operation. During I/O operations, the CPU automatically inserts a single Wait state (T_{WA}). This extra Wait state allows sufficient time for an I/O port to decode the address from the port address lines.

When the CPU is accessing the on-chip I/O registers (PIO, CTC, SIO and system control registers), the data from/to these registers also appears on the data bus, or data bus is output during I/O cycle.

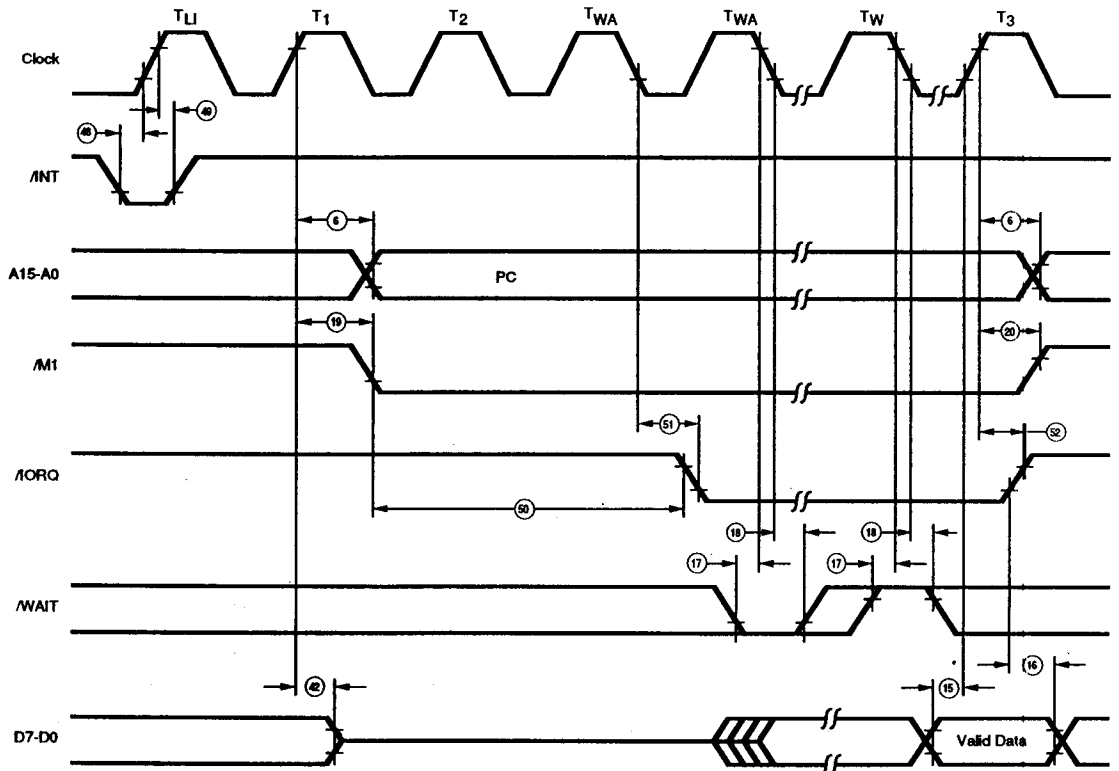


Note: T_{WA} = One wait cycle automatically inserted by CPU

Figure 43. Input or Output Cycle
(See Table A)

Interrupt Request/Acknowledge Cycle. The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 44). When an interrupt is accepted, a special /M1 cycle is generated.

During this /M1 cycle, /IORQ becomes active (instead of /MREQ) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.

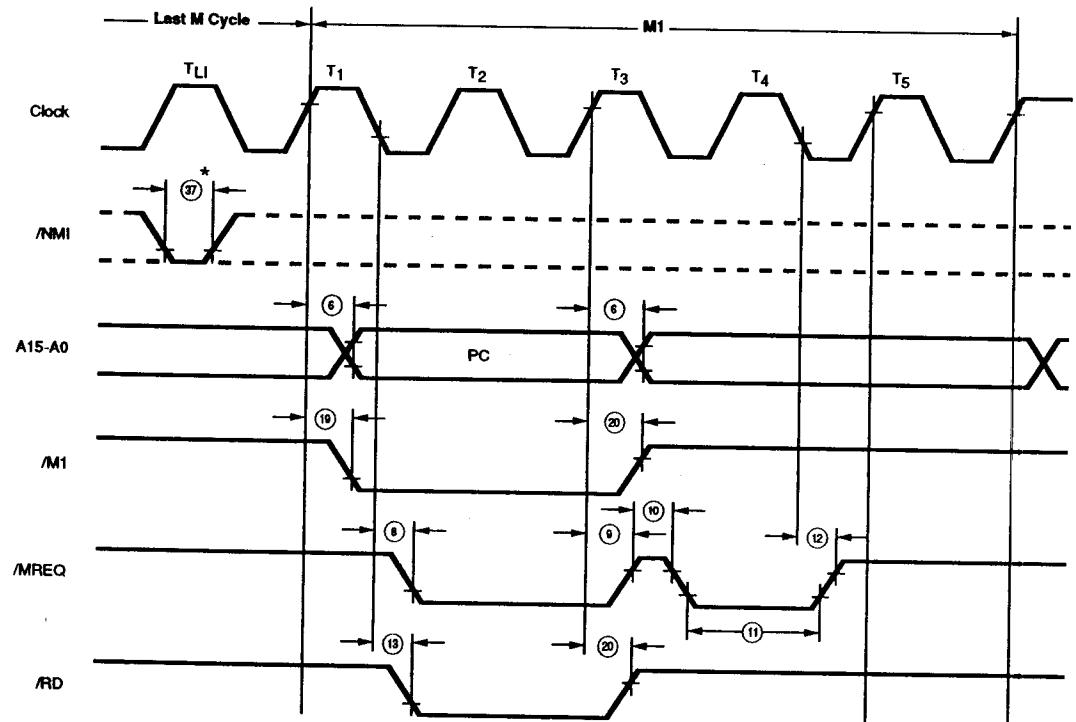


NOTE: 1) T_{LI} = Last state of any instruction cycle
 2) T_{WA} = Wait cycle automatically inserted by CPU

Figure 44. Interrupt Request/Acknowledge Cycle
 (See Table A)

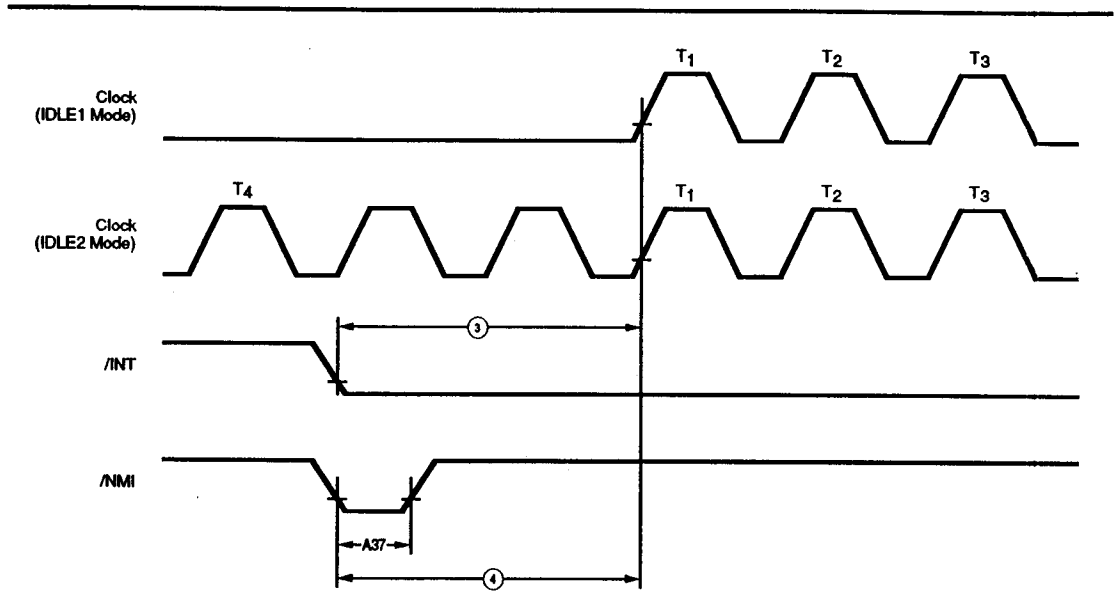
Non-Maskable Interrupt Request Cycle. /NMI is sampled at the same time as the maskable interrupt input /INT, but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal

memory read operation except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the /NMI service routine located at the address 0066H (Figure 45).

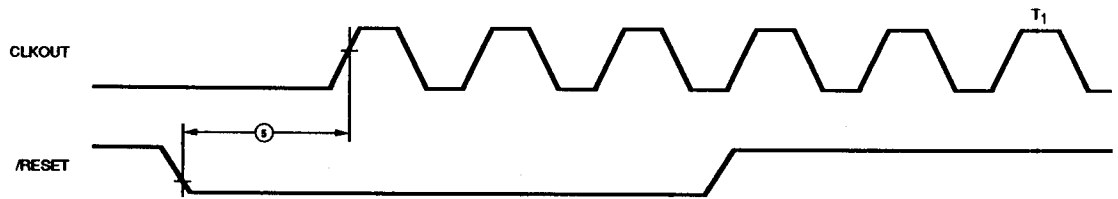


* Although /NMI is an asynchronous input, to guarantee its being recognized on the following machine cycle, /NMI's falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{LI}).

Figure 45. Non-Maskable Interrupt Request Operation
(See Table A)

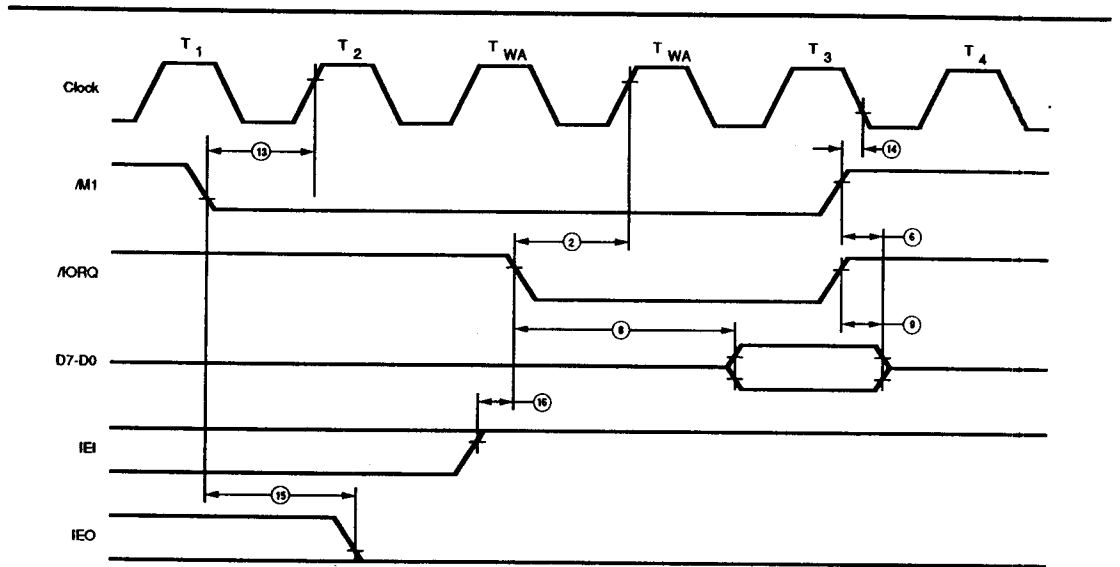


(a) Clock Restart Timing by /INT, /NMI (IDLE1/2 Mode)

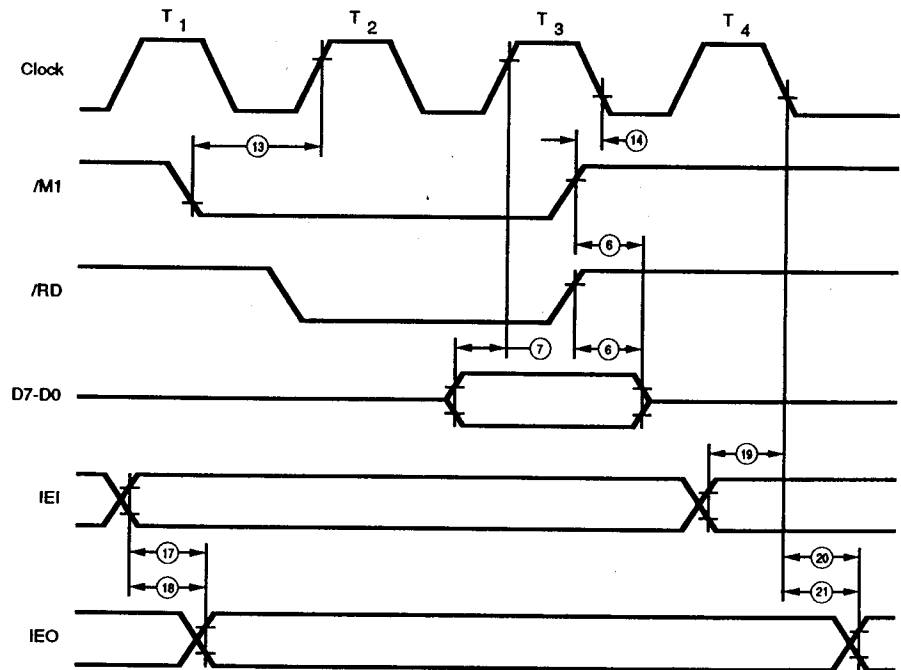


(b) Clock Restart Timing by /RESET (IDLE 1/2 Mode)

Figure 51. Clock Restart Timing (IDLE1/2 Mode)
(See Table B)



(b) Interrupt Acknowledge Cycle Timing for On-chip peripheral from External Bus master
(See Table C)



(c) Op-code fetch Cycle Timing for On-chip peripheral from External Bus master
(See Table C)

Figure 53. On-chip Peripheral Timing from External Bus master (Continued)

SIO Timing

Figure 56 shows the timing for on-chip SIO.

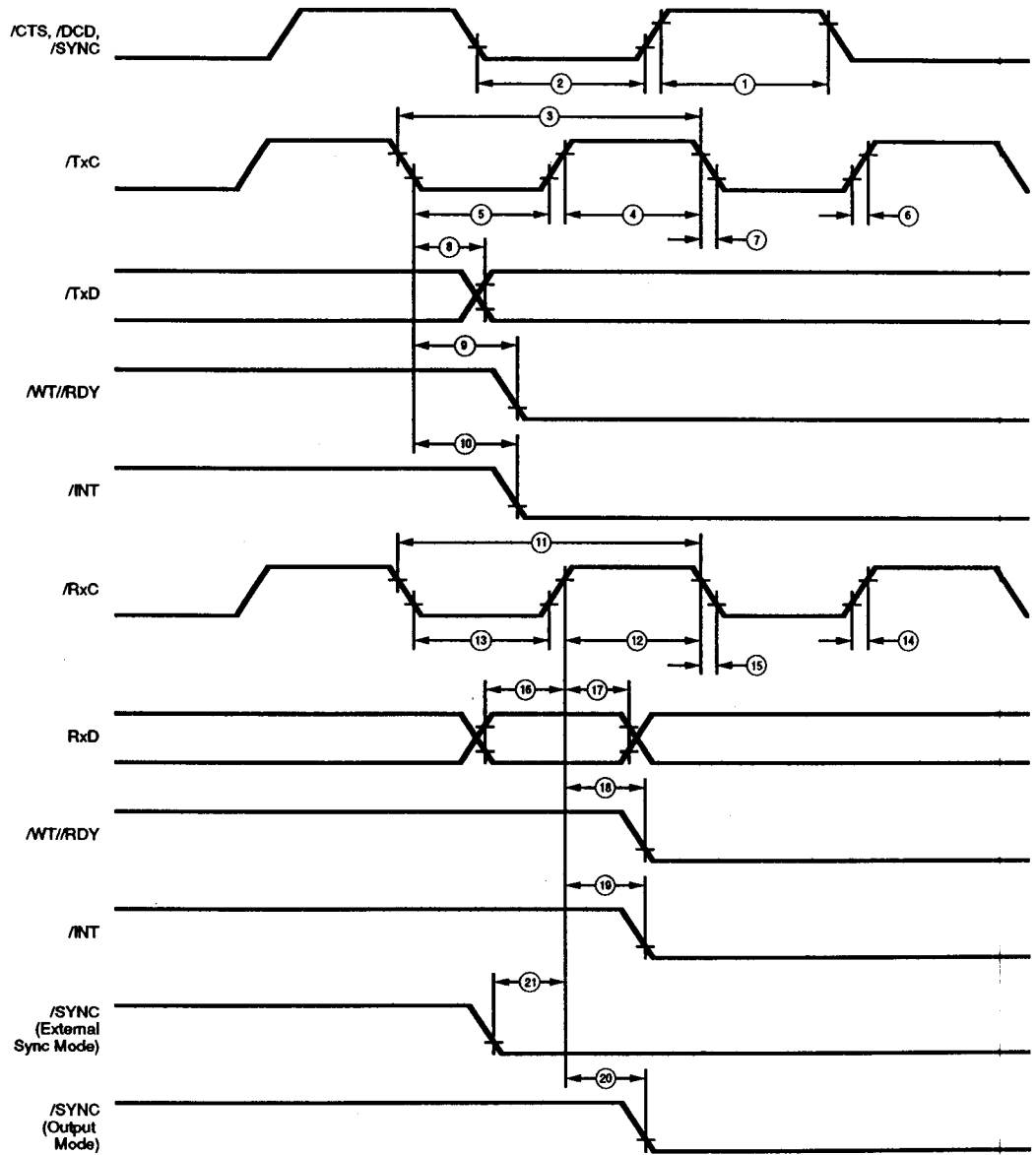


Figure 56. SIO Timing
(See Table F)

AC CHARACTERISTICS (Continued)

Table B. CGC Timing (See Figure 49 to 52)

No	Symbol	Parameter	Z84C1306 Z84C1506		Z84C1310 Z84C1510		Z84C1316* Z84C1516		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	TRST(INT)S	Clock Restart Time by /INT (STOP Mode)	(Typ)2 ¹⁴ +2.5TcC		(Typ)2 ¹⁴ +2.5TcC		(Typ)2 ¹⁴ +2.5TcC		ns	
2	TRST(MNI)S	Clock Restart Time by /NMI (STOP Mode)	(Typ)2 ¹⁴ +2.5TcC		(Typ)2 ¹⁴ +2.5TcC		(Typ)2 ¹⁴ +2.5TcC		ns	
3	TRST(INT)I	Clock Restart Time by /INT (IDLE Mode)	2.5TcT		2.5TcT		2.5TcT		ns	
4	TRST(Nmi)I	Clock Restart Time by /NMI (IDLE Mode)	2.5TcT		2.5TcT		2.5TcT		ns	
5	TRST(RESET)I	Clock Restart Time by /RESET (IDLE Mode)	1TcC		1TcC		1TcC		ns	
6	TiCLKOUT	CLKOUT Rise Time		15		10		6	ns	
7	TrCLKOUT	CLKOUT Fall time		15		10		6	ns	
8	TcX1	XTAL1 Cycle Time (for External Clock Input on XTAL1) Divide-by-Two Mode Divide-by-One Mode	81 162		50 100		31 61		ns ns	
9	TwIX1	XTAL1 Low Pulse Width (for External Clock Input on XTAL1) Divide-by-Two Mode Divide-by-One Mode	35 65		15 40		10 25		ns ns	
10	TwHX1	XTAL1 High Pulse Width (for External Clock input on XTAL1) Divide-by-Two mode Divide-by-One mode	35 65		15 40		10 25		ns ns	
11	TrX1	XTAL1 Rise Time (for External Clock Input on XTAL1)		25		25		15	ns	[B1]
12	TfX1	XTAL1 Fall Time (for External Clock Input on XTAL1)		25		25		15	ns	[B1]

Note:

[B1] If parameters 8 and 9 are not met, adjust parameters 11 and 12 to satisfy parameters 8 and 9.

Table F. SIO Timing (See Figures 53(a) and 56)

No	Symbol	Parameter	Z84C1306 Z84C1506		Z84C1310 Z84C1510		Z84C1316* Z84C1516		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	TwPh	Pulse Width (High)	150		120		80		ns	
2	TwPl	Pulse Width (Low)	150		120		80		ns	
3	TcTxC	/TxC Cycle Time	250		200		120		ns	[F1]
4	TwTxCH	/TxC Width (High)	85		80		55		ns	
5	TwTxCL	/TxC Width (Low)	85		80		55		ns	
6	TrTxC	/TxC Rise Time		60		60		60	ns	
7	TfTxC	/TxC Fall Time		60		60		60	ns	
8	TdTxCl(TxD)	/TxC Fall to TxD Delay		160		120		40	ns	
9	TdTxCl(W/RRf) (Ready Mode)	/TxC Fall to /W//RDY Fall Delay	5	9	5	9	5	8	TcC	
10	TdTxCl(INTf)	/TxC Fall to /INT Fall Delay	5	9	5	9	5	9	TcC	
11	TcRxC	/RxC Cycle Time	250		200		120		ns	[F1]
12	TwRxCh	/RxC Width (High)	85		80		55		ns	
13	TwRxCl	/RxC Width (Low)	85		80		55		ns	
14	TrRxC	/RxC Rise Time		60		60		60	ns	
15	TfRxC	/RxC Fall Time		60		60		60	ns	
16	TsRxD(RxCr)	RxD to /RxC Rise Setup Time (X1 Mode)	0		0		0		ns	
17	ThRxCr(RxD)	/RxC Rise to RxD Hold Time (X1 Mode)	80		60		40		ns	
18	TdRxCr(W/RRf)	/RxC Rise to /W//RDY Fall Delay (Ready Mode)	10	13	10	13	10	13	TcC	
19	TdRxCr(INTf)	/RxC Rise to /INT Fall Delay	10	13	10	13	10	13	TcC	
20	TdRxCr(SYNCf)	/RxC Rise to /SYNC Fall Delay (Output Modes)	4	7	4	7	4	7	TcC	
21	TsSYNCf(RxCr)	/SYNC Fall to /RxC Rise Setup (External Sync Modes)	-100		-100		-100		ns	[F2]
22	TdIOf(W/RRf)	/IORQ Fall or Valid Address to /W//RDY Delay (Wait Mode)		130		110		40	ns	[F2]
23	TdCr(W/RRf)	Clock Rise to /W//RDY Delay (Ready Mode)		85		85		40	ns	[F2]
24	TdCl(W/Rz)	Clock Fall to /W//RDY Float Delay (Wait Mode)		90		80		40	ns	[F2]

Notes:

[F1] In all modes, the System Clock rate must be at least five times the maximum data rate.

[F2] Parameters 22 to 24 are on Figure 53a.