# Zilog - Z84C1516FSC Datasheet

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z80 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 16MHz |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Security Features | - |
| Package / Case | 100-QFP |
| Supplier Device Package | 100-QFP |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z84c1516fsc |

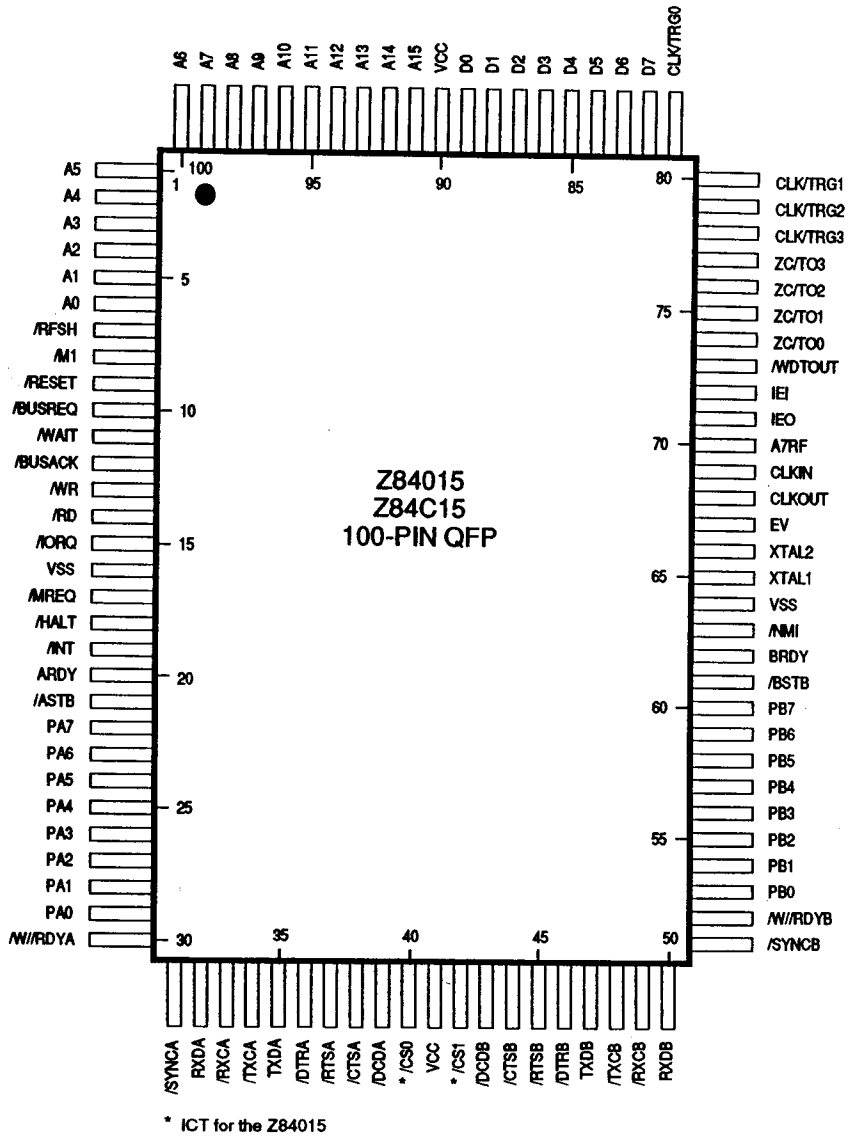



**Figure 4. Z84015/Z84C15 Pin-out Assignments**

## PIN DEFINITIONS

The pin assignment for each device is shown in Figures 3 and 4. Following is the description on each pin. For the description and the pin number, if stated as "x13" or "x15", that applies to both Z84C13/Z84013 or Z84C15/Z84015. Otherwise, C13 for Z84C13, C15 for Z84C15, 013 for Z84013 and 015 for Z84015.

## SYSTEM CONTROL SIGNALS (Continued)

**Note:** For the Z84C13/C15, to access on-chip resources from the CPU (e.g., ICE CPU), the CPU is electrically disconnected; A15-A0, /MREQ, /IORQ, /RD and /WR are changed to input; D7-D0 changes its direction; /M1, /HALT and /RFSH are put into the high impedance state when the EV pin is set to "1". Also, /BUSACK is 3-stated. For details, please refer to "Functional Description" on EV mode.

| Pin Name | Pin Number | Input/Output, 3-State | Function |
|---|---|---|---|
| ICT | 42,44(013), 40,42(015), Not with C13/C15 | Out | Test pins. Used in the open state. |
| NC | 24,27,57,65(x13), Not with x15 | | Not connected. |
| VCC | 43,84(x13), 41,90(x15) | Power Supply | +5 Volts |
| VSS | 22, 62(x13), 16,64(x15) | Power Supply | 0 Volts |

## PIO SIGNALS (for the Z84x15 only)

| Pin Name | Pin Number | Input/Output, 3-State | Function |
|---|---|---|---|
| /ASTB | 21(x15) | In | Port A strobe pulse from a peripheral device. The signal is used as the handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see "PIO Basic Timing"). |
| /BSTB | 61(x15) | In | Port B strobe pulse from a peripheral device. This signal is used as the handshake between Port B and external circuits. The meaning of this signal is the same as /ASTB, except when Port A is in mode 2 (see "PIO Basic Timing"). |
| ARDY | 20(x15) | Out | Register A ready signal. Used as the handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see "PIO Basic Timing"). |
| BRDY | 62(x15) | Out | Register B ready signal. Used as the handshake between Port B and external circuits. The meaning of this signal is the same as ARDY except when Port A is in mode 2 (see "PIO Basic Timing"). |
| PA7-PA0 | 22-29(x15) | I/O, 3-State | Port A data signals. Used for data transfer between Port A and external circuits. |
| PB7-PB0 | 53-60(x15) | I/O, 3-State | Port B data signals. Used for transfer between Port B and external circuits. |

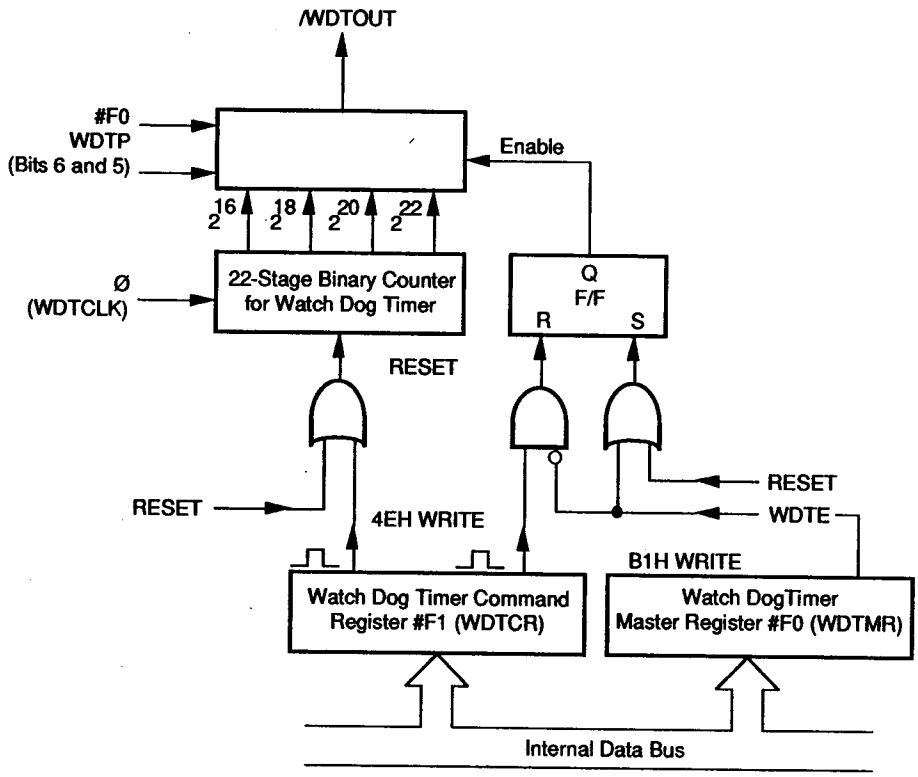



**Figure 9. Block Diagram of Watch Dog Timer**

**Z84013/015 Only.** If the system clock is provided on the CLKIN pin, none of the power-down mode (except RUN mode) is supported.

**Z84C13/C15 Only.** If the system clock is provided on the CLKIN pin, only the IDLE2 mode is applicable. In this mode, if the HALT instruction is executed, internal clock to the CTC is kept on "Continue", but the clock to the other components (CPU, PIO, SIO and Watch Dog Timer) are stopped. The divide-by-two circuit of the CGC unit can be skipped by programming bit D4 of the WDTMR (see "Programming" section). Upon Power-on Reset, it comes up in divide by two mode.

**System Clock Generation**

The IPC has a built-in oscillator circuit and the required clock can be easily generated by connecting a crystal to the external terminals (XTAL1, XTAL2). Clock output is the same frequency as half the speed of the crystal frequency. Example of oscillator connections are shown in Figure 10.

**Z84C13/C15.** Clock output is the same, or half, of the external frequency.

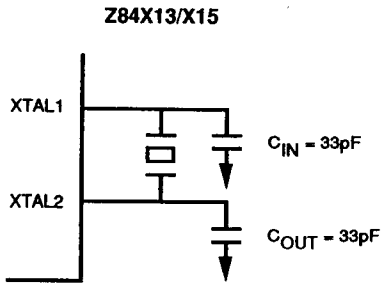



**Figure 10. Circuit Configuration For Crystal**

Recommended characteristics of the crystal and the values for the capacitor are as follows (the values will change with crystal frequency).

- Type of crystal: Fundamental, parallel type crystal (AT cut is recommended).
- Frequency tolerance: Application dependent.
- CL, Load capacitance: Approximately 22pf (acceptable range is 20-30pf).
- Rs, equivalent-series resistance: ≤ 150 ohms.
- Drive level: 10mW (for ≤ 10MHz crystal); 5mW (for ≥ 10MHz crystal).
- $C_{IN} = C_{OUT} = 33pF$.

**Power-On Reset Logic Unit (Z84C13/C15 Only)**
The Z84C13/C15 has the enhanced feature of a Power-on Reset Circuit. During the power-up sequence, the open-drain gate of the on-chip power-on Reset circuit drives /RESET pin to "0" for 25 to 75 msec after the power supply passes through approx. 2.2V. After the termination of the "Power-on Reset" cycle, the open-drain gate of the on-chip Power-on Reset circuit stops to drive the /RESET pin. It is required to have external pull-up register on the /RESET pin.

If it receives /RESET input from outside after the power-on sequence and while the Reset Output Disable bit in Misc Control Register is cleared to "0", it will drive the /RESET pin for 16-processor clock cycles from the falling edge of the external /RESET input. Otherwise, the /RESET pin must be kept in the active state for a period of at least 3 system clock cycles.

If there are power-on reset circuits outside of this device, drive this pin with OPEN-DRAIN type gates with pull-up resisters because /RESET signal is driven low for the period mentioned above during the Power-on sequence. If the external Power-on Reset circuit has push-pull type drivers and they drive the /RESET pin to "1" during that period, it may cause damage. In particular, when using Z84C13/C15 in the Z84013/015 socket, modification may be required on the external reset circuit.

**Wait State Generator Unit (Z84C13/C15 Only)**
The Z84C13/C15 has the enhanced feature of a Wait State Generator circuit. It is capable of generating /WAIT signals to the CPU internally. The status of the External /WAIT input line is sampled after the insertion of software wait states, except for the wait state's insertion of Interrupt Daisy Chain Wait (for this cycle, insertion of a wait state is not simple).

The Wait State Control Register can be programmed to generate multiple Wait states during different CPU cycles listed as follows.

**Memory Wait and Opcode wait.** The Wait State Generator can put 0 to 3 wait states in memory accesses. Additionally, one added wait state can be inserted during an /M1 (Opcode fetch) cycle, because /M1 cycle's timing requirement is tighter than memory Read/Write cycles. It generates wait states to the Memory Access in a specified address range, which is programmed in the Memory Wait Boundary Register.

**I/O Wait.** The Wait State generator can put 0, 2, 4 or 6 wait states in I/O accesses. Regardless of the programming of this field, no I/O wait states are inserted for accesses to on-chip peripherals.

**Interrupt Vector Wait.** During Interrupt acknowledge cycle, the Wait State Generator can insert one wait state after /IORQ goes active, to extend the time between /IORQ fall to vector fetch by CPU. It allows a slow vector response device.

**Interrupt Daisy Chain Wait and RETI sequence extension.** During Interrupt acknowledge cycle, the Wait State Generator can insert 0, 2, 4 or 6 wait states between /M1 falling to /IORQ falling edge, to extend the time required to settle daisy chain. This allows a longer daisy chain. Also, this field controls the number of wait states inserted during RETI (Return From Interrupt) cycle. If specified to insert 4 or 6 wait states during Interrupt Acknowledge cycle, Wait State Generator also inserts wait states during RETI fetch sequence. This sequence is generated with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts 2 or 4 wait states, respectively, if op-code followed by EDh is 4Dh. One wait state if the following op-code is not 4Dh.

**Chip Select Signals (Z84C13/C15 Only)**
The Z84C13/C15 has an enhanced feature of adding two chip select (/CS0, /CS1) pins. Both signals are originally IC test pins (ICT) on the Z84013/015. The boundary value for each Chip Select Signal is 4 bits wide, and compare with A15-A12 of the address. Each Chip Select Signal goes active when:

/CS0: (D3-D0 of CSBR) ≥ A15-A12 ≥ 0
/CS1: (D7-D4 of CSBR) ≥ A15-A12 > (D3-D0 of CSBR)

(Where CSBR is the contents of Chip Select Boundary Register.)

There is also a separate /CS enable bit. /CS0 is enabled on power-up with a boundary value of "F" causing /CS0 to go active for all memory accesses. /CS1 is disabled on

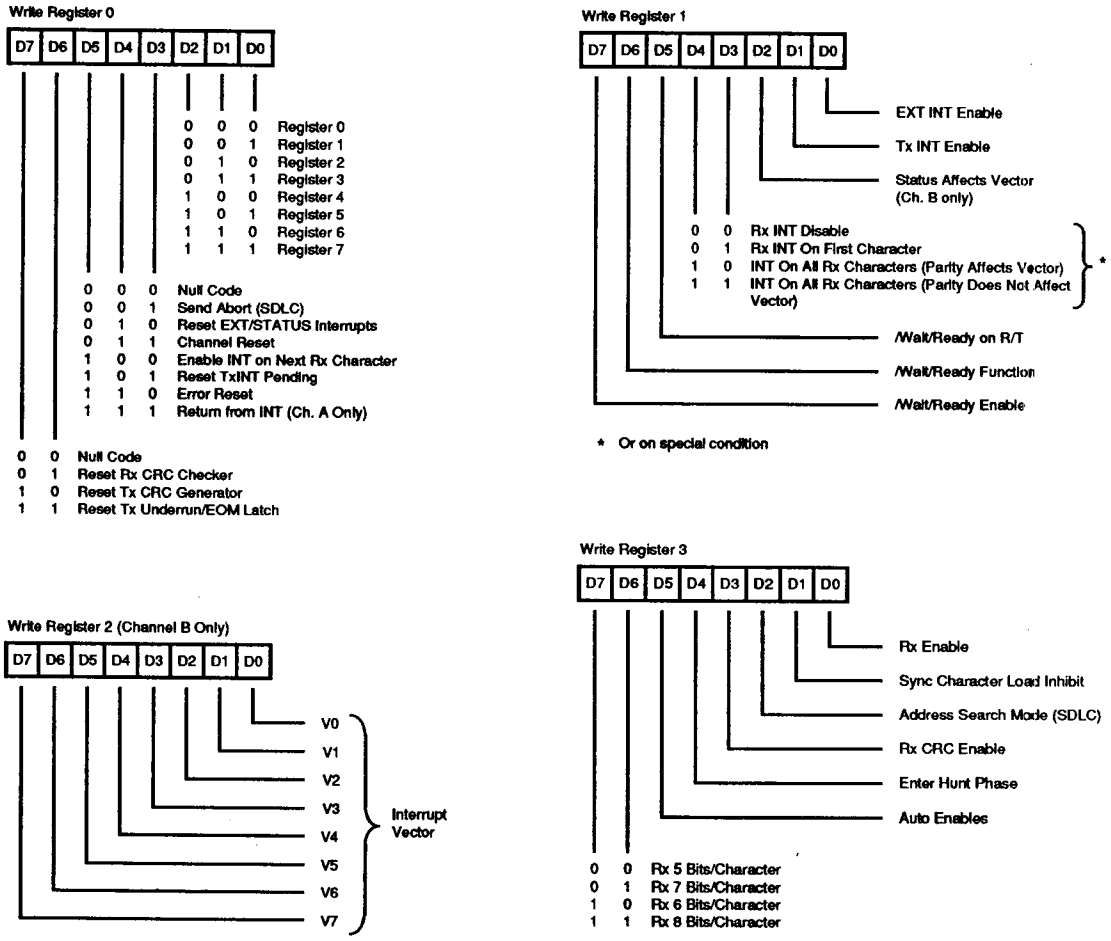



**Figure 21. SIO Write Registers**

**Clearing the WDT.** The WDT can be cleared by writing "4Eh" into the WDTCR.

**Watch Dog Timer Master Register (WDTMR;I/O address F0h).** This register controls the activities of the Watch Dog Timer and selects power-down mode of operation (Figure 22).

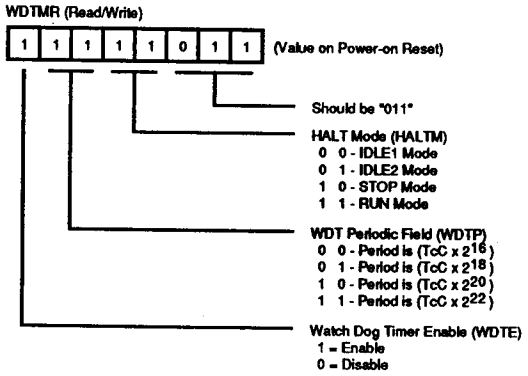



**Figure 22. Watch Dog Timer Master Register**

**Bit D7.** *Watch Dog Timer Enable* (WDTE). This bit controls the activities of Watch Dog Timer. The WDT can be enabled by setting this bit to "1". To disable WDT, write "0" to this bit followed by writing "B1h" in the WDT Command Register. Watch Dog Timer Logic has a "double key" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop, due to program run-away. Upon Power-on reset, this bit is set to "1" and the WDT is enabled.

**Bit D6-D5.** *WDT Periodic field* (WDTP). This two bit field determines the desired time period. Upon Power-on reset, this field sets to "11".

00 - Period is (TcC * $2^{16}$)
01 - Period is (TcC * $2^{18}$)
10 - Period is (TcC * $2^{20}$)
11 - Period is (TcC * $2^{22}$)

**Bit D4-D3.** *HALT mode* (HALTM). This two bit field specifies one of four power-down modes. To change this field, write "DBh" to the WDT command register, followed by a write to this register. For detailed descriptions of this field, please refer to the section "Mode of operations." Upon Power-on Reset, this field is set to 11, which specifies "RUN mode."

00 - IDLE 1 Mode
01 - IDLE 2 Mode
10 - STOP Mode
11 - RUN Mode

**Bit D2-D0.** *Reserved.* These three bits are reserved and should always be programmed as "011". A read to these bit returns "011".

**Watch Dog Timer Command Register (WDTCR; I/O address F1h).** In conjunction with the WDTMR, this register works as a "Second key" for the Watch Dog Timer. This register is write only (Figure 23).

Write B1h after clearing WDTE to "0" - Disable WDT.
Write 4Eh - Clear WDT.
Write DBh followed by a write to HALTM - Change Power-down mode.

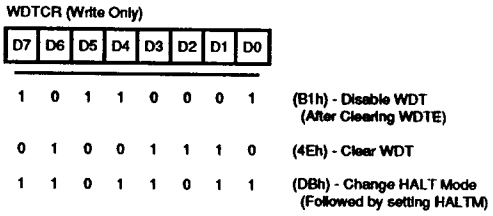



**Figure 23. Watch Dog Timer Command Register**

## INTERRUPT PRIORITY REGISTER
(INTPR; I/O address F4h)

This register (write only) is provided to determine the interrupt priority for the CTC, SIO and the PIO (Figure 24).

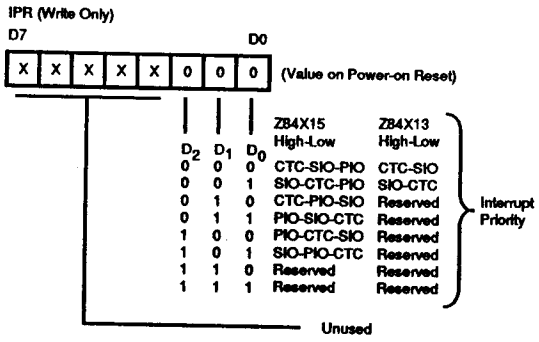



**Figure 24. Interrupt Priority Register**

**Bit D7-D3.** Unused

**Bit D2-D0.** This field specifies the order of the interrupt daisy chain. Upon Power-on Reset, this field is set to "000".

| | Z84C15 High - Low | Z84C13 High - Low |
|---|---|---|
| 000 | CTC-SIO-PIO | CTC-SIO |
| 001 | SIO-CTC-PIO | SIO-CTC |
| 010 | CTC-PIO-SIO | Reserved |
| 011 | PIO-SIO-CTC | Reserved |
| 100 | PIO-CTC-SIO | Reserved |
| 101 | SIO-PIO-CTC | Reserved |
| 110 | Reserved | Reserved |
| 111 | Reserved | Reserved |

## REGISTERS FOR SYSTEM CONFIGURATION

(The following registers are not available on Z84013/015.) There are four indirectly accessible registers to determine System configuration with the Z84C13/C15. These indirectly accessible registers are: Wait State Control Register (WCR, Control Register 00h), Memory Wait Boundary Register (MWBR, Control Register 01h), Chip Select Boundary Register (CSBR, Control Register 02h) and Misc. Control Register (MCR, Control Register 03h). To access these registers, Z84C13/C15 writes "register number to be accessed" to the System Control Register Pointer (SCRP, I/O address EEh), and then accesses the target register through the System Control Data Port (SCDP, I/O address EFh). The pointer which writes into SCRP is kept until modified.

**System Control Register Pointer (SCRP, I/O address EEh)**
This register stores the pointer to access System Control Registers (WCR, MWBR, CSBR and MCR). This register is Read/Write and it holds the pointer value until modified. Upon Power-on Reset, all bits are cleared to zero. The pointer value, other than 00h to 03h is reserved and is not written. Upon Power-on Reset, this register is set to "00h" (Figure 25).

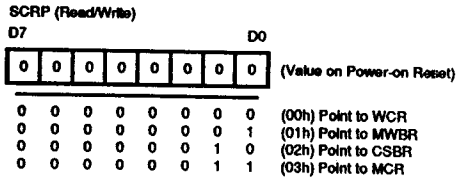



**Figure 25. System Control Register Pointer**

**System Control Data Port (SCDP, I/O address EFh)**
This register is to access WCR, MWBR, CSBR and MCR (Figure 26).

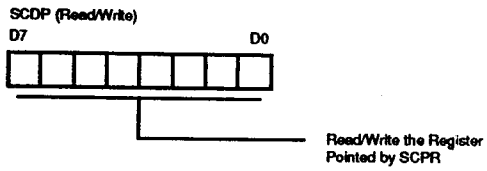



**Figure 26. System Control Data Port**

**Wait State Control Register (WCR, Control Register 00h)**
This register can be accessed through SCDP with the pointer value 00h in SCRP (Figure 27). To maintain compatibility with the Z84013/015, the Z84C13/C15 inserts the maximum number of wait states (set all bits of this register to one) for fifteen /M1 cycles after Power-on Reset. It automatically clears the contents of this register (move to no-wait state insertion) on the trailing edge of the 16th /M1 signal unless software has programmed a value. If automatic wait state insertion is needed, the wait state is programmed within this time period. A read to WCR during this period will return FFh, unless programmed.

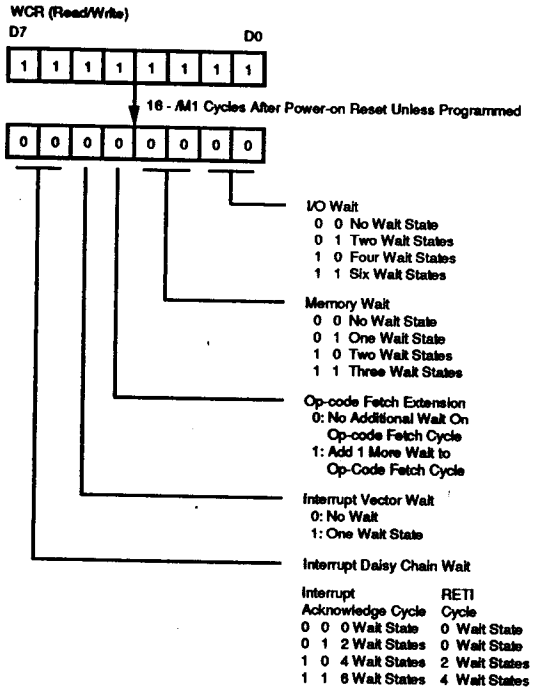



**Figure 27. Wait State Control Register**

This register has the following fields:

**Bit 7-6.** *Interrupt Daisy Chain Wait.* This 2-bit field specifies the number of wait states to be inserted during an Interrupt Daisy Chain settle period of the Interrupt Acknowledge cycle, which is/IORQ falls after the settling period from /M1 going active "0". Also, this field controls the number of wait states inserted during the RETI (Return From Interrupt) cycle. If specified to insert 4 or 6 wait states during Interrupt Acknowledge cycle, the Wait state generator also inserts wait states during RETI fetch sequence. This sequence is formed with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts 1 wait state if op-code followed by EDh is NOT 4Dh, and inserts 2 or 4 wait states, respectively, if the following op-code is 4Dh.

| Interrupt Acknowledge | RETI cycle |
|---|---|
| 00 - No Wait states | No Wait states |
| 01 - 2 Wait states | No Wait states |
| 10 - 4 Wait states | 2 Wait states |
| 11 - 6 Wait states | 4 Wait states |

For fifteen /M1 cycles from Power-on Reset, bits 7-6 are set to "11" . They clear to "00" on the trailing edge of the 16th /M1 signal unless programmed.

**Bit 5.** *Interrupt Vector Wait.* While this bit is set to one, the wait state generator inserts one wait state after the /IORQ signal goes active during the Interrupt acknowledge cycle. This gives more time for the vector read cycle. While this bit is cleared to zero, no wait state is inserted (standard timing). For fifteen /M1 cycles from Power-on Reset, this bit is set to "1", then cleared to "0" on the trailing edge of the 16th /M1 signal, unless programmed.

**Bit 4.** *Opcode Fetch Extension.* If this bit is set to "1", one additional wait state is inserted during the Op-code fetch cycle in addition to the number of wait states programmed in the Memory Wait field. For fifteen /M1 cycles from Power-on Reset, this bit is set to "1", then cleared to "0" on the trailing edge of the 16th /M1 signal, unless programmed.

**Bit 3-2.** *Memory Wait States.* This 2-bit field specifies the number of wait states to be inserted during memory Read/ Write transactions.

00 - No Wait states
01 - 1 Wait states
10 - 2 Wait states
11 - 3 Wait states

For fifteen /M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the16th /M1 signal, unless programmed.

**Bit 1-0.** *I/O Wait states.* This 2-bit field specifies the number of wait states to be inserted during I/O transactions.

00 - No Wait states
01 - 2 Wait states
10 - 4 Wait states
11 - 6 Wait states

For fifteen /M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the16th /M1 signal, unless programmed. For the accesses to the on-chip I/O registers, no Wait states are inserted regardless of the programming of this field.

**Memory Wait Boundary Register (MWBR, Control Register 01h)**

This register specifies the address range to insert memory wait states. When accessed memory addresses are within this range, the Memory Wait State generator inserts Memory Wait States specified in the Memory Wait field of WCR (Figure 28).

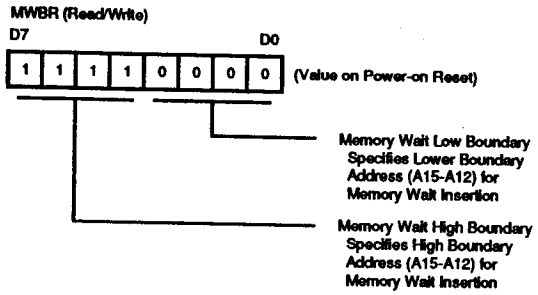



**Figure 28. Memory Wait Boundary Register**

**Bit D7-D4.** *Memory Wait High Boundary.* This field specifies A15-A12 of the upper address boundary for Memory Wait.

**Bit D3-D0.** *Memory Wait Low Boundary.* This field specifies A15-12 of the lower address boundary for Memory Wait.

Memory Wait states are inserted for the address range:

(D7-D4 of MWBR) ≥ A15-A12 ≥ (D3-D0 of MWBR)

This register is set to "F0h" on Power-on Reset, which specifies the address range for Memory Wait as "0000h to FFFFh".

**Chip Select Boundary Register (CSBR, Control Register 02h)**

This register specifies the address range for each chip select signal. When accessed memory addresses are within this range, chip select signals are active (Figure 29).

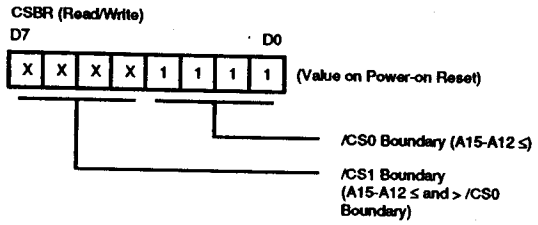



**Figure 29. Chip Select Boundary Register**

**D7-D4.** */CS1 Boundary Address.* These bits specify the boundary address range for /CS1. The bit values are ignored on power-up as the /CS1 enable bit is off. The /CS1 is asserted if the address lines A15-12 have an address value greater than the programmed value for /CS0, and less than or equal to the programmed value in these bits.

**D3-D0.** */CS0 Boundary Address.* These bits specify the boundary address range for /CS0. /CS0 is asserted if the address lines A15-12 have an address value less than or equal to the programmed boundary value. The /CS0 enable bit in the MCR must be set to 1. Upon Power-up reset, these bits come up as all 1's so that /CS0 is asserted for all addresses.

Chip Select signals are active for the address range:

/CS0: (D3-D0 of CSBR) ≥ A15-A12 ≥ 0
/CS1: (D7-D4 of CSBR) ≥ A15-A12 > (D3-D0 of CSBR)

This register is set to "xxxx1111b" on Power-on Reset, which specifies the address range of /CS0 for "0000h to FFFFh" (all Memory location) and /CS1 "undefined."

**Misc Control Register (MCR, Control Register 03h)**

This register specifies miscellaneous options on this device (Figure 30).

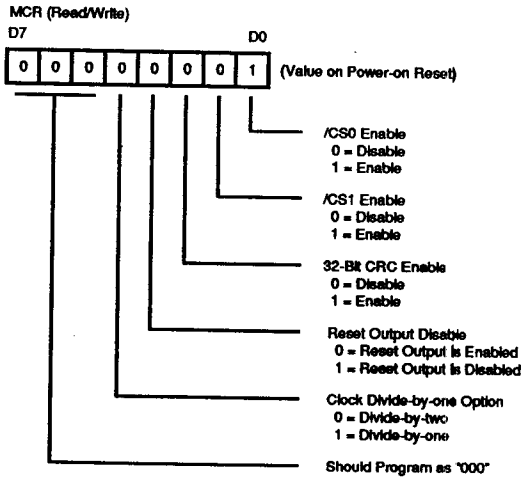



**Figure 30. Misc Control Register**

**Bit D7-D5.** *Reserved.* These three bits are reserved and are always programmed as "000".

**Bit D4.** *Clock Divide-by-one option.* "0"-Disable, "1"-enable. On-chip CGC unit has divide-by-two circuit. By setting this bit to one, this circuit is bypassed and CLKOUT is equal to X'tal oscillator frequency (or external clock input on the XTAL1 pin). This bit has no effect when the on-chip CGC unit is not in use and the external system clock is fed from CLKIN pin. Upon Power-on Reset, this bit is cleared to 0 and the clock is divided by two.

In IDLE2 Mode, the internal oscillator and clock output (CLKOUT) continue to operate. The internal system clock, fed from CLKIN to the components other than CTC is stopped at the T4 Low state of HALT instruction execution.

**STOP Mode (HALTM=10).** Shown in Figure 34 is the basic timing when the halt instruction is executed in STOP Mode.

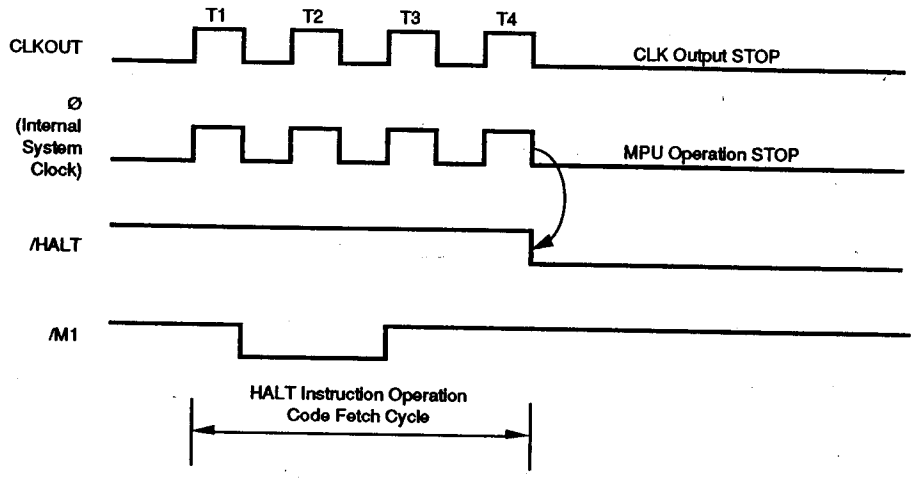



**Figure 34. STOP Mode Timing**
(At Halt Instruction Execution)

In STOP Mode, the on-chip CGC unit is stopped at T4 Low state of HALT instruction execution. Therefore, clock output (CLKOUT), operation of Watch Dog Timer, CPU, PIO, CTC, SIO are stopped.

**Release from Halt State.** The halt state of the CPU is released when "0" is input to the /RESET signal and the MPU is reset or an interrupt request is accepted. An interrupt request signal is sampled at the leading edge of the last clock cycle (T4 state) of NOP instruction. In case of the maskable interrupt, interrupt will be accepted by an active /INT signal ("0" level). Also, the interrupt enable flip-flop is set to "1". The accepted interrupt process is started from the next cycle.

Further, when the internal system clock is stopped (IDLE1/2 Mode, STOP Mode), it is necessary first to restart the internal system clock. The internal system clock is restarted when /RESET or interrupt signal (/NMI or /INT) is asserted.

**RUN Mode (HALTM=11).** The halt release operation is enabled by interrupt request in RUN Mode (Figure 35).

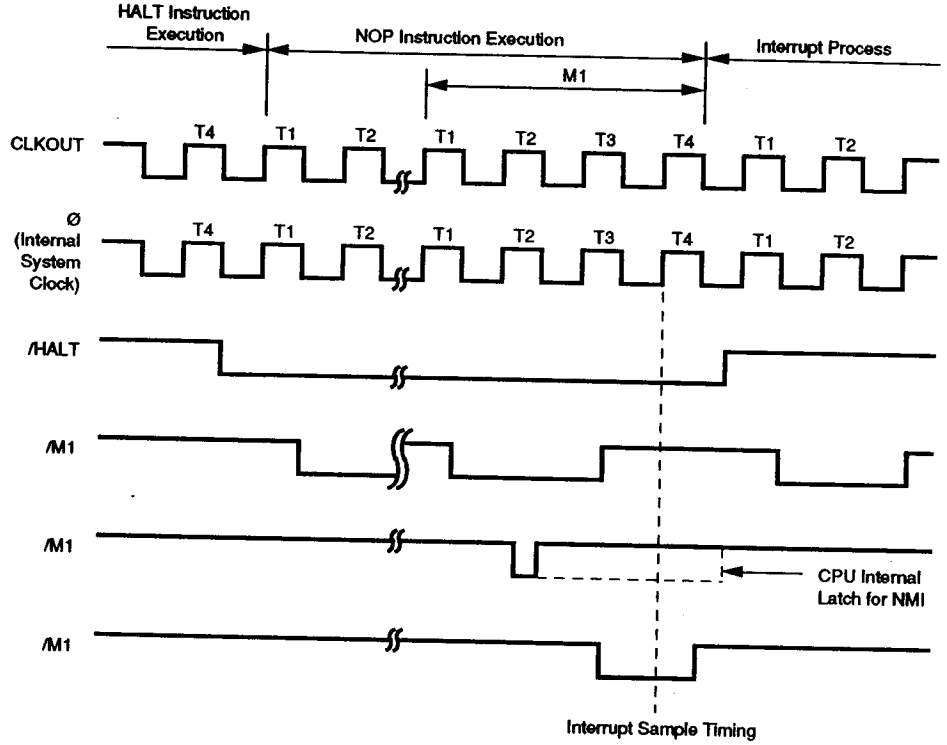



**Figure 35. Halt Release Operation Timing By Interrupt Request Signal in RUN Mode**

In RUN Mode the internal system clock is not stopped. If the interrupt signal is recognized on the rising clock edge of T4 of the continued NOP instruction, CPU will execute the interrupt process from the next cycle.

The halt release resets CPU in RUN Mode (Figure 36). After reset, CPU will execute an instruction starting from address 0000H. However, in order to reset the CPU it is necessary to keep /RESET signal at "0" for at least 3 system clock cycles. (For Z84C13/C15: 3 clock cycles if Reset output is disabled.) In addition, if /RESET signal becomes "1", after the dummy cycle for at least two T states, CPU executes an instruction from address 0000H.

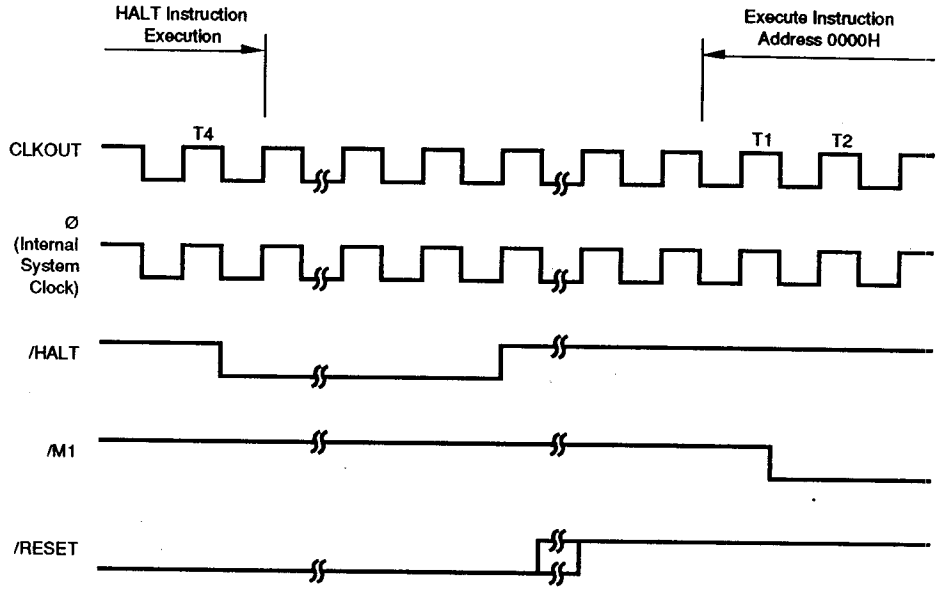



**Figure 36. Halt Release Operation Timing By Reset in RUN Mode**

**IDLE1 Mode (HALTM=00), IDLE2 Mode (HALTM=01).** The halt release operation by interrupt signal in IDLE1 Mode is shown in Figure 37 (a) and in IDLE2 Mode in Figure 37 (b).

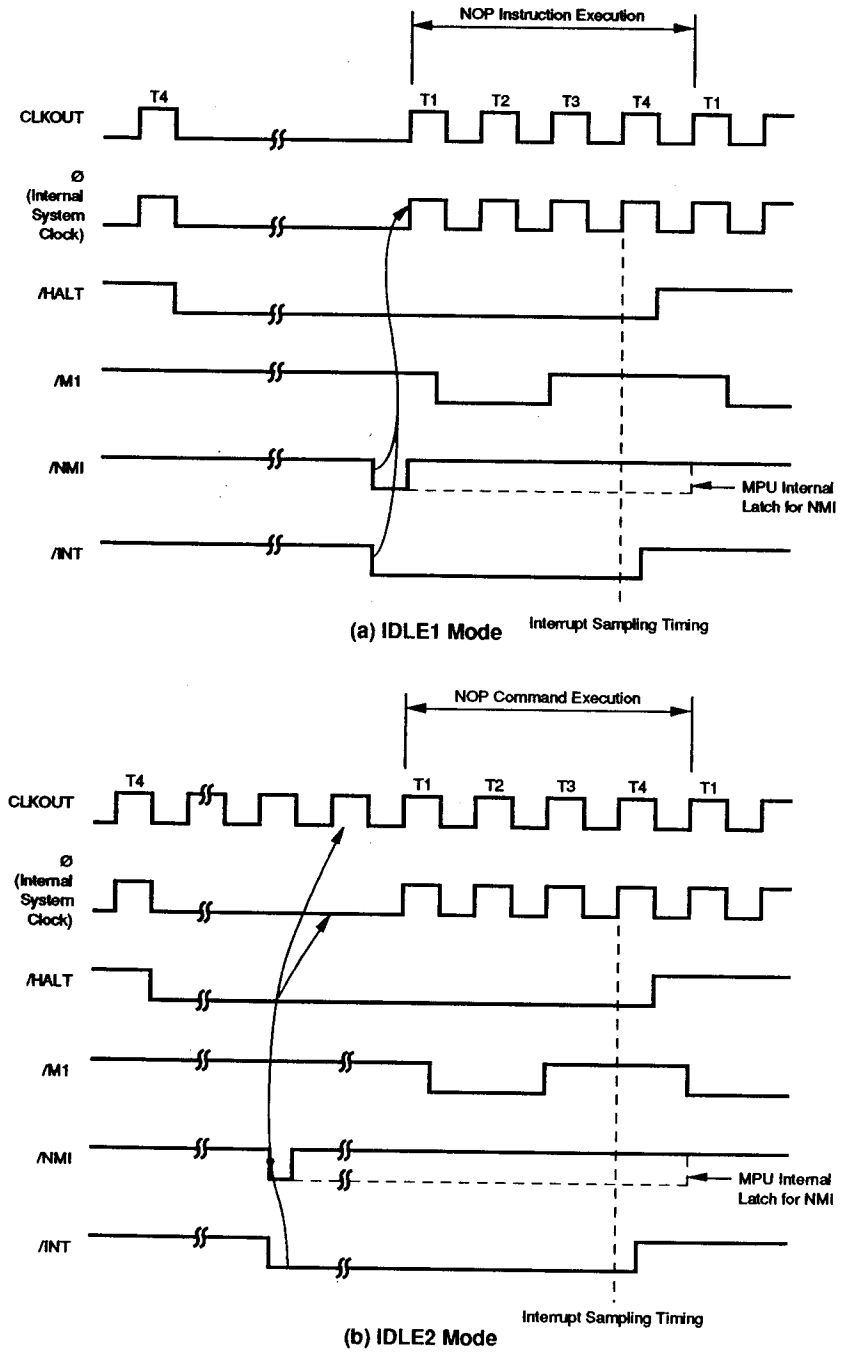



**Figure 37. Halt Release Operation Timing By Interrupt Request Signal in IDLE1/2 Mode**

When /RESET signal at "0" level is input into the IPC, the internal system clock is restarted and the IPC will execute an instruction stored in address 0000H.

At time of /RESET signal input, it is necessary to take the same care as that in resetting the IPC in RUN Mode.

**Halt release in STOP Mode (HALTM=10) by interrupt.** The halt release operation by interrupt signal in STOP Mode is shown in Figure 39.

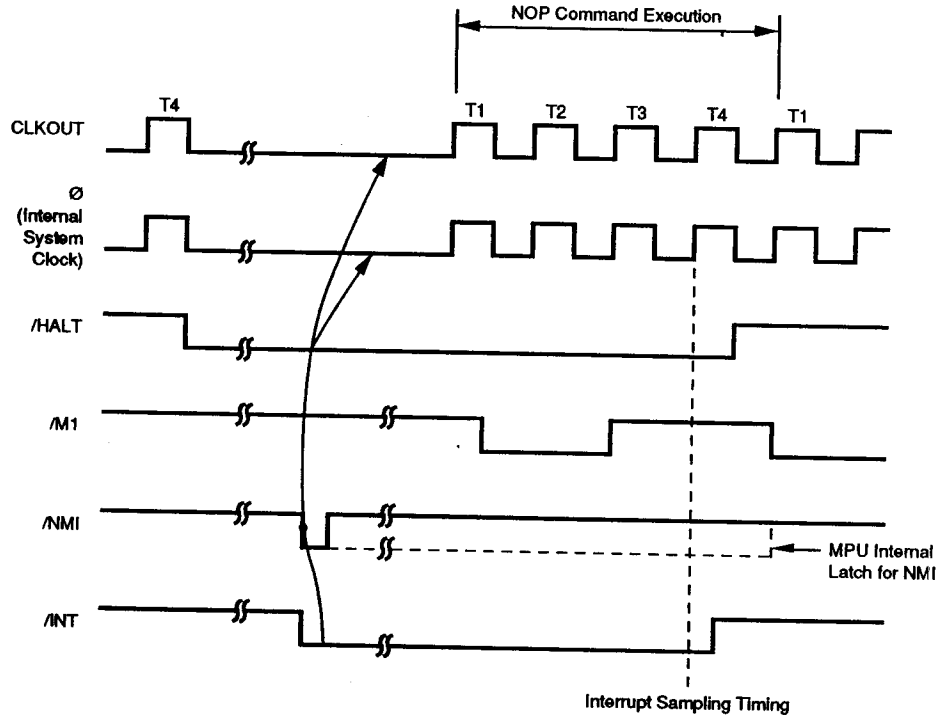



**Figure 39. Halt Release Operation Timing By Interrupt Request Signal in STOP Mode**

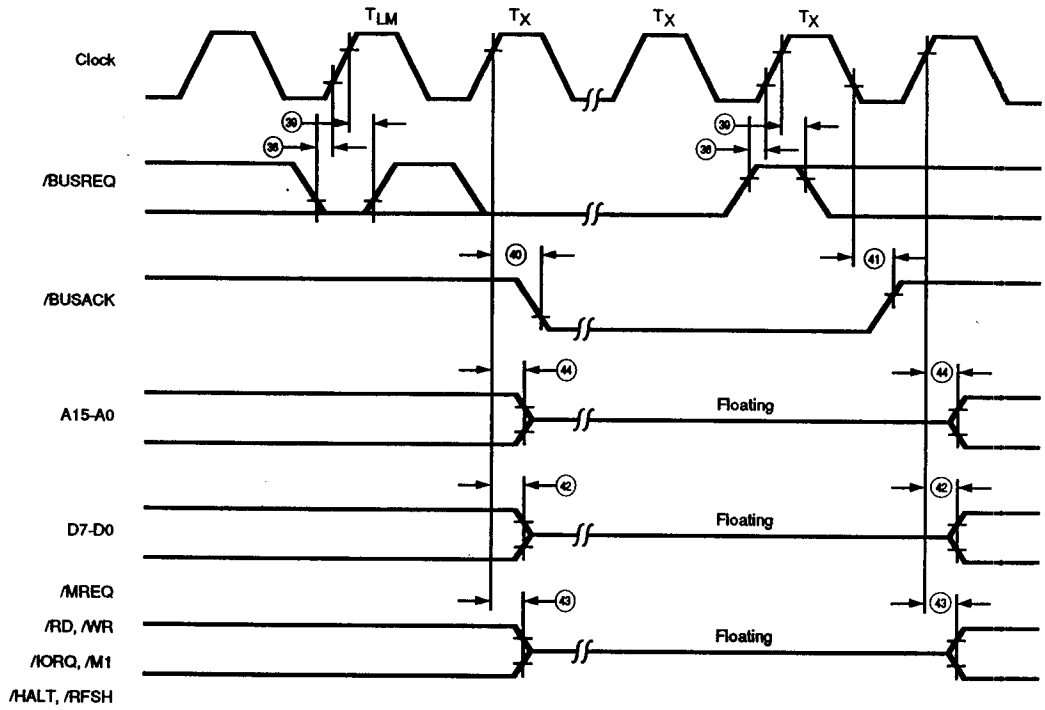
When the IPC receives an interrupt signal, the internal oscillator is restarted. To obtain stabilized oscillation, CLKOUT (and the internal system clock) are started after a start-up time of ($2^{14}$+2.5) TcC (TcC: Clock Cycle) by the internal counter.

CPU executes one NOP instruction after the internal system clock is restarted. At the same time, it samples an interrupt signal at the rise of T4 state during the execution of this NOP instruction. If the interrupt signal is accepted, CPU executes the interrupt process operation from the next cycle.

During interrupt signal input, it is necessary to take the same care as the interrupt signal input in IDLE1/2 Mode.

**Halt release in STOP Mode (HALTM=10) by /RESET.** When /RESET at "0" level is input into the IPC, the internal oscillator is restarted. However, the internal clock counter for warm-up does not operate. Therefore, the operation is not carried out properly due to unstable clock oscillation. It is necessary to hold /RESET at "0" level for sufficient time. The halt release operation by the IPC resetting in STOP Mode is shown in Figure 40.

**Bus Request/Acknowledge Cycle.** The CPU samples /BUSREQ with the rising edge of the last clock period of any machine cycle (Figure 46). If /BUSREQ is active, the CPU sets its address, data, and /MREQ to Inputs, and /IORQ, /RD and /WR lines set to an input for on-chip peripheral access from an external bus master with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.




Notes: 1) $T_{LM}$ = Last state of any M cycle

2) $T_X$ = An arbitrary clock cycle used by requesting device

**Figure 46. BUS Request/Acknowledge Cycle**
(See Table A)

**CTC Timing**

Figure 55 shows the timing for on-chip CTC.

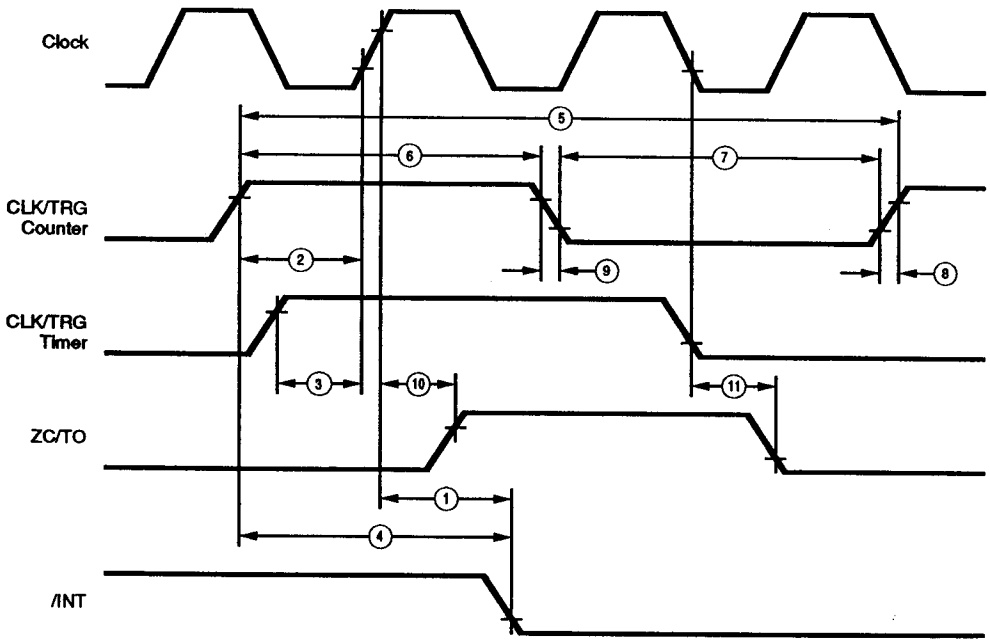



**Figure 55. Counter/Timer Timing**
(See Table E)

## SIO Timing

Figure 56 shows the timing for on-chip SIO.

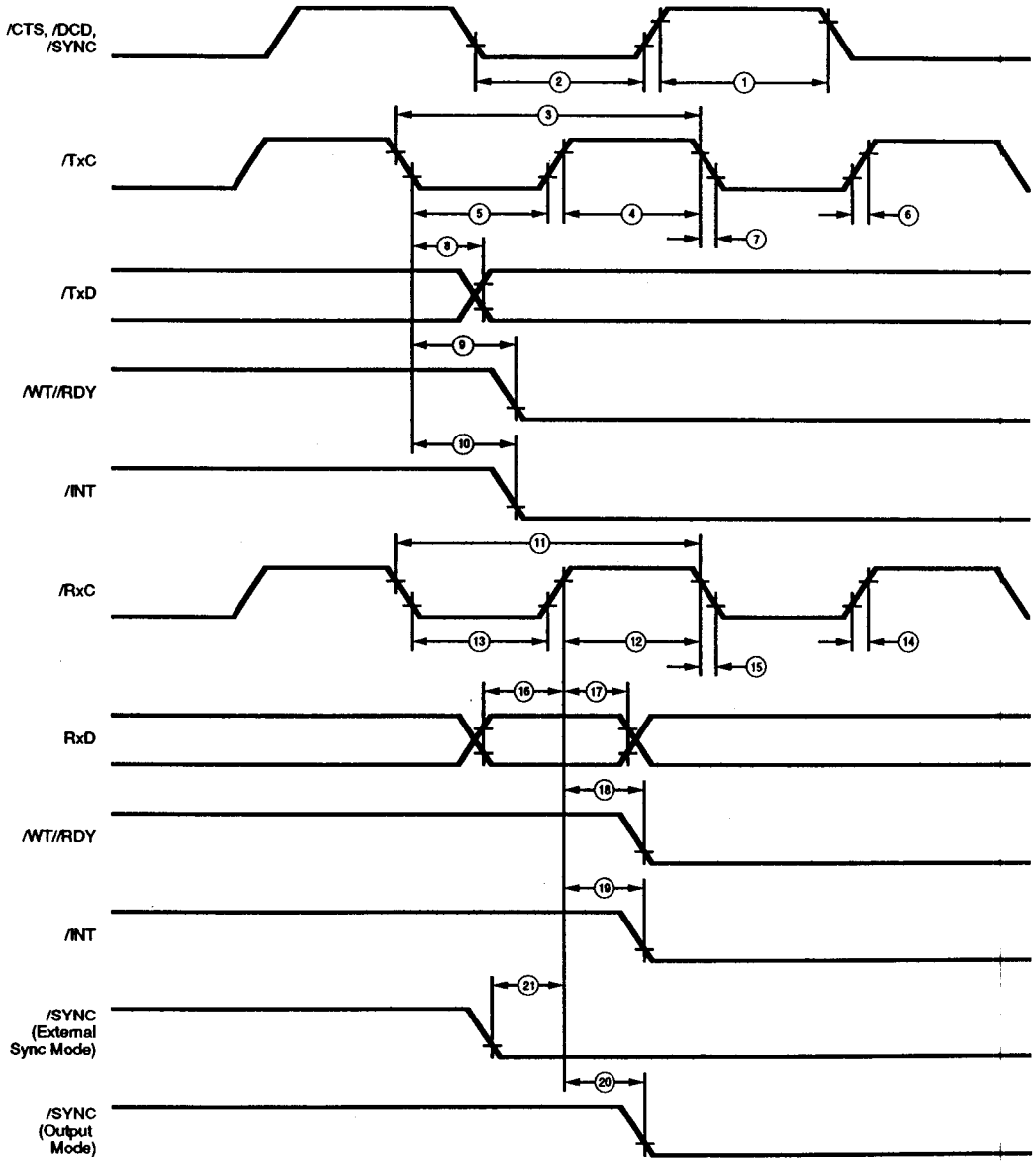



**Figure 56. SIO Timing**
(See Table F)

## STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature range is:
E = -40°C to 100°C
Voltage Supply Range:
+4.50V ≤ Vcc ≤ + 5.50V

All AC parameters assume a load capacitance of 100 pf. Add 10 ns delay for each 50 pf increase in load up to a maximum of 150 pf for the data bus and 100 pf for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pf.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

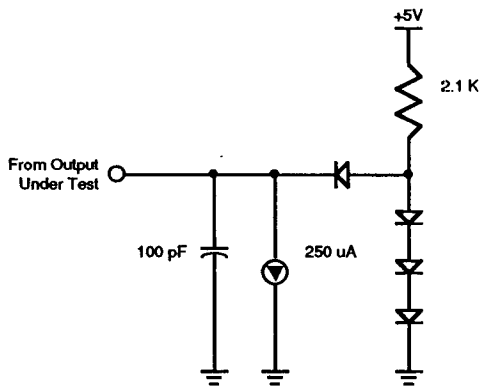



**Figure 58. Standard Test Load**

## CAPACITANCE

Guaranteed by design and characterization

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $C_{CLOCK}$ | Clock Capacitance | 35 | pF | |
| $C_{IN}$ | Input Capacitance | 5 | pF | |
| $C_{OUT}$ | Output Capacitance | 15 | pF | |

## AC CHARACTERISTICS (Continued)

**Table A. CPU Timing** (Continued)

| No | Symbol | Parameter | Z84X1306 Z84X1506 Min | Z84X1306 Z84X1506 Max | Z84X1310 Z84X1510 Min | Z84X1310 Z84X1510 Max | Z84C1316* Z84C1516 Min | Z84C1316* Z84C1516 Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| 41 | TdCf(BUSACKr) | Clock Fall to /BASACK Rise Delay | | 90 | | 75 | | 40 | ns | |
| 42 | TdCr(Dz) | Clock Rise to Data Float Delay | | 80 | | 65 | | 40 | ns | |
| 43 | TdCr(CTz) | Clock Rise to Control Outputs Float Delay (/MREQ, /IORQ, /RD and /WR) | | 70 | | 65 | | 40 | ns | |
| 44 | TdCr(Az) | Clock Rise to Address Float Delay | | 80 | | 75 | | 40 | ns | |
| 45 | TdCTr(A) | Address Hold Time from /MREQ, /IORQ, /RD or /WR | 35** | | 20** | | | 0 | ns | |
| 46 | TsRESET(Cr) | /RESET to Clock Rise Setup Time | 60 | | 40 | | 15 | | ns | |
| 47 | ThRESET(Cr) | /RESET to Clock Rise Hold Time | 10 | | 10 | | 10 | | ns | |
| 48 | TsINTf(Cr) | /INT Fall to Clock Rise Setup Time | 70 | | 50 | | 15 | | ns | |
| 49 | ThINTr(Cr) | /INT Rise to Clock Rise Hold Time | 10 | | 10 | | 10 | | ns | |
| 50 | TdM1f(IORQf) | /M1 Fall to /IORQ Fall Delay | 359** | | 220** | | 100 | | ns | |
| 51 | TdCf(IORQf) | Clock Fall to /IORQ Fall Delay | | 70 | | 55 | | 45 | ns | |
| 52 | TdCf(IORQr) | Clock Rise to /IORQ Rise Delay | | 70 | | 55 | | 45 | ns | |
| 53 | TdCf(D) | Clock Fall to Data Valid Delay | | 130 | | 110 | | 75 | ns | |
| 54 | TRDf(D) | /RD Fall to Output Data Valid | | TBD | | 60 | | 40 | ns | |
| 55 | TdIORQ(D) | /IORQ Fall to Output Data Valid | | TBD | | 70 | | 45 | ns | |
| 56 | TwRESET | /RESET Pulse Width 013/015, or C13/C15 with RESET Output Disabled | 3TcC | | 3TcC | | 3TcC | | ns | |
| 57 | TwRESEToe | /RESET Pulse Width RESET Output Enabled | 2TcC | | 2TcC | | 2TcC | | ns | |
| 58 | TwRESETdo | /RESET Drive Duration RESET Output Enabled | 16TcC | | 16TcC | | 16TcC | | ns | |
| 59 | TwRESETpor | /RESET drive duration on Power-On Sequence | 10 | 75 | 10 | 75 | 10 | 75 | ms | |

**Notes:**

* 16 MHz Timings are preliminary and subject to change. Only C version

** For clock period other than the minimum shown, calculate parameters using the formula on Table H.

[A1] These parameters apply to the external Clock input on CLKIN pin. For the cases where external Clock is fed from XTAL1, please refer to Table B.

[A2] For loading >= 50 pF, decrease width by 10 ns for each additional 50 pF.

| | 6MHz Min | Max | 10MHz Min | Max | 16MHz Min | Max |
|---|---|---|---|---|---|---|
| Input Buffer Delay | 10nS | | 10nS | | 10 nS | |
| Look ahead gate delay | 10nS | | 10nS | | 10 nS | |

| 6MHz | PIO part Min | Max | CTC part Min | Max | SIO part Min | Max |
|---|---|---|---|---|---|---|
| TdM1(IEO) | | 90nS | | 130nS | | 150nS |
| TsIEI(IO) | | 90nS | | 100nS | | 70nS |
| TdIEI(IEOf) | | 100nS | | 90nS | | 50nS |
| TdIEI(IEOr) | | 130nS | | 90nS | | 50nS |

| 10MHz | PIO part Min | Max | CTC part Min | Max | SIO part Min | Max |
|---|---|---|---|---|---|---|
| TdM1(IEO) | | 60nS | | 60nS | | 90nS |
| TsIEI(IO) | | 50nS | | 70nS | | 50nS |
| TdIEI(IEOf) | | 50nS | | 50nS | | 30nS |
| TdIEI(IEOr) | | 50nS | | 50nS | | 30nS |

**Preliminary**

| 16MHz* | PIO part Min | Max | CTC part Min | Max | SIO part Min | Max |
|---|---|---|---|---|---|---|
| TdM1(IEO) | | 55nS | | 55nS | | 90nS |
| TsIEI(IO) | | 45nS | | 65nS | | 45nS |
| TdIEI(IEOf) | | 45nS | | 45nS | | 30nS |
| TdIEI(IEOr) | | 45nS | | 45nS | | 30nS |

*** Note:**
16MHz is for C15 only.

If using an interrupt from only a portion of the IPC, these numbers are smaller than the values shown above. For more details about the "Z80 Daisy Chain Structure," please refer to the Application Note "Z80 Family Interrupt Structure" included in the Z80 Data book.