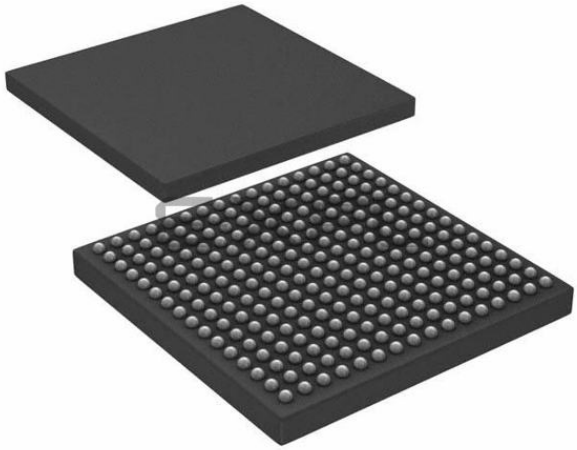

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	119
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-1fg256k

Speed Grade and Temperature Grade Matrix

	Std	–1	–2
K	AFS600 AFS1500 M1AFS600 M1AFS1500	AFS600 AFS1500 M1AFS600 M1AFS1500	NA

Note: K = Extended Temperature Range: –55°C to 100°C Junction

Summary of Differences Between Extended Temperature and Commercial/Industrial Grade Devices

Table 2 • Summary of Differences

Feature*	Extended Temperature	Commercial/Industrial Temperature
Temperature (junction)	–55°C to 100°C	0°C to 85°C / –40°C to 100°C
AV (negative voltage input)	Not supported between –40°C to –55°C	Supported across all temperatures
AC (positive voltage input)	Not supported between –40°C to –55°C	Supported across all temperatures
Sleep mode	Not supported between –40°C to –55°C	Supported across all temperatures
Pigeon Point ATCA IP support (P1)	Not Supported	Supported across all temperatures
MicroBlade Advanced Mezzanine Card support (U1)	Not Supported	Supported across all temperatures
Remainder of features	Supported across all temperatures	Supported across all temperatures

*Note: *This table lists only the differences in features. For additional details, refer to the "Device Architecture" section on page 2-1 and the "DC and Power Characteristics" section on page 3-1.*

Software Considerations for Extended Temperature Fusion

When designing with Libero® System-on-Chip (SoC) software, select the K package (example: 256 FBGA K) in the Device Selection Wizard. This enables the option of selecting the **EXT** temperature range under operating conditions.

Device Availability

Contact your local Microsemi SoC Products Group representative for device availability: (http://www.microsemi.com/soc/contact/offices/index.html).

diode. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADC MUX.

Figure 1-1 on page 1-5 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad measures the source of the power supply. The AC pad measures the voltage drop across an external sense resistor to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad measures the load-side voltage level.

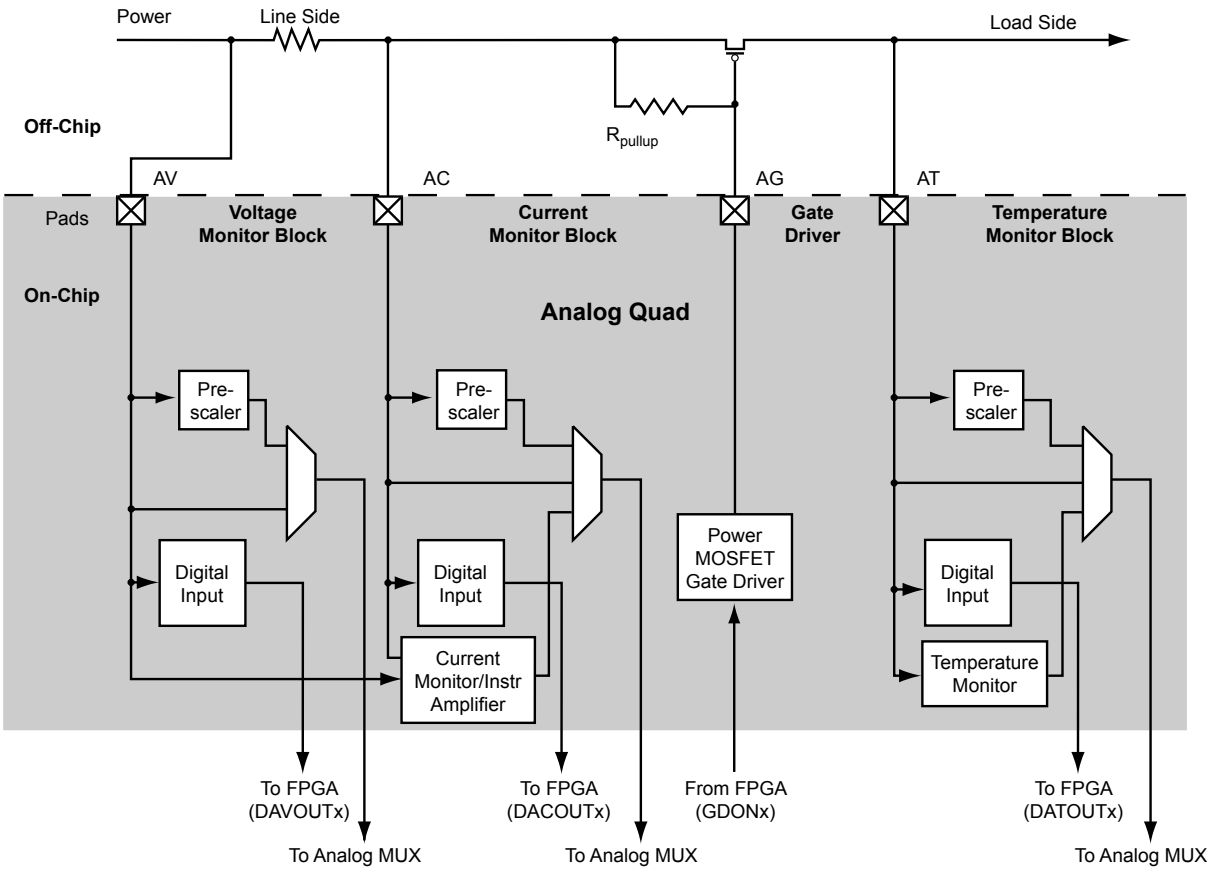


Figure 1-1 • **Analog Quad**

Embedded Memories

Flash Memory Blocks

The flash memory available in each Fusion device is composed of two to four flash blocks, each 2 Mbits in density. Each block operates independently with a dedicated flash controller and interface. Fusion flash memory blocks combine fast access times (60 ns random access and 10 ns access in Read-Ahead mode) with a configurable 8-, 16-, or 32-bit datapath, enabling high-speed flash operation without wait states. The memory block is organized in pages and sectors. Each page has 128 bytes, with 33 pages comprising one sector and 64 sectors per block. The flash block can support multiple partitions. The only constraint on size is that partition boundaries must coincide with page boundaries. The flexibility and granularity enable many use models and allow added granularity in programming updates.

Fusion devices support two methods of external access to the flash memory blocks. The first method is a serial interface that features a built-in JTAG-compliant port, which allows in-system programmability during user or monitor/test modes. This serial interface supports programming of an AES-encrypted stream. Secure data can be passed through the JTAG interface, decrypted, and then programmed in the flash block. The second method is a soft parallel interface.

The system application, Level 3, is the larger user application that utilizes one or more applets. Designing at the highest level of abstraction supported by the Fusion technology stack, the application can be easily created in FPGA gates by importing and configuring multiple applets.

In fact, in some cases an entire FPGA system design can be created without any HDL coding.

An optional MCU enables a combination of software and HDL-based design methodologies. The MCU can be on-chip or off-chip as system requirements dictate. System portioning is very flexible, allowing the MCU to reside above the applets or to absorb applets, or applets and backbone, if desired.

The Fusion technology stack enables a very flexible design environment. Users can engage in design across a continuum of abstraction from very low to very high.

Core Architecture

VersaTile

Based upon successful ProASIC3/E logic architecture, Fusion devices provide granularity comparable to gate arrays. The Fusion device core consists of a sea-of-VersaTiles architecture.

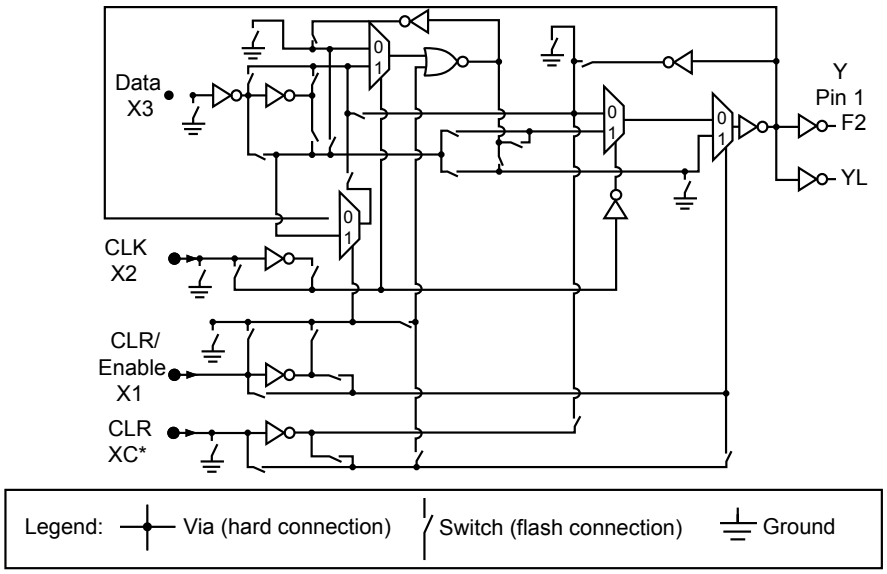
As illustrated in Figure 2-2, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a 4th input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR signal is supported by a fourth input, which can only be routed to the core cell over the VersaNet (global) network.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources (Figure 2-2).



*Note: *This input can only be connected to the global clock distribution network.*

Figure 2-2 • **Fusion Core VersaTile**

VersaNet Global Networks and Spine Access

The Fusion architecture contains a total of 18 segmented global networks that can access the VersaTiles, SRAM, and I/O tiles on the Fusion device. There are 6 chip (main) global networks that access the entire device and 12 quadrant networks (3 in each quadrant). Each device has a total of 18 globals. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 180 internal/external clocks (in an AFS1500 device) or other high-fanout nets in Fusion devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on Fusion devices.

The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device. There are four quadrant global network regions per device (Figure 2-12 on page 2-12).

The spines are the vertical branches of the global network tree, shown in Figure 2-11 on page 2-11. Each spine in a vertical column of a chip (main) global network is further divided into two equal-length spine segments: one in the top and one in the bottom half of the die.

Each spine and its associated ribs cover a certain area of the Fusion device (the "scope" of the spine; see Figure 2-11 on page 2-11). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or another net defined by the user (Figure 2-13). Quadrant spines can be driven from user I/Os on the north and south sides of the die, via analog I/Os configured as direct digital inputs. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

Details of the chip (main) global network spine-selection MUX are presented in Figure 2-13. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/Os on the north and south sides of the device. For details on using spines in Fusion devices, see the application note *Using Global Resources in Actel Fusion Devices*.

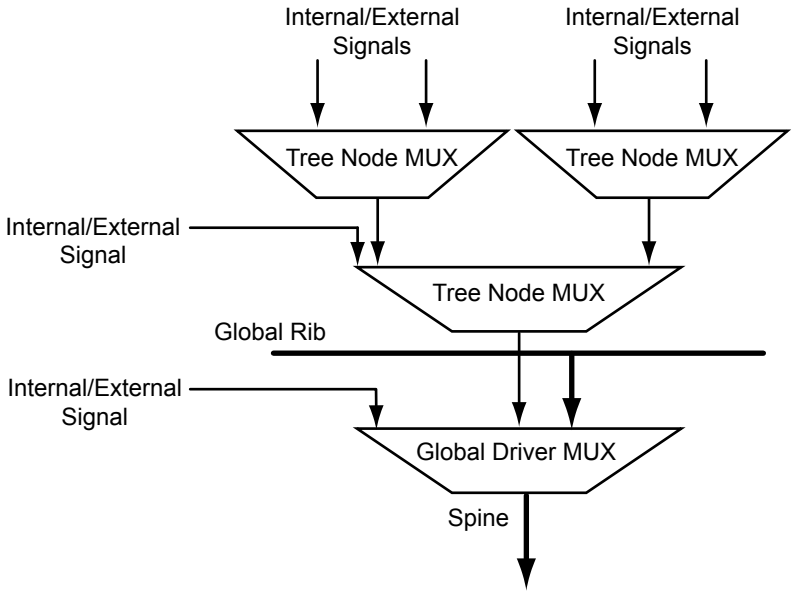


Figure 2-13 • **Spine-Selection MUX of Global Tree**

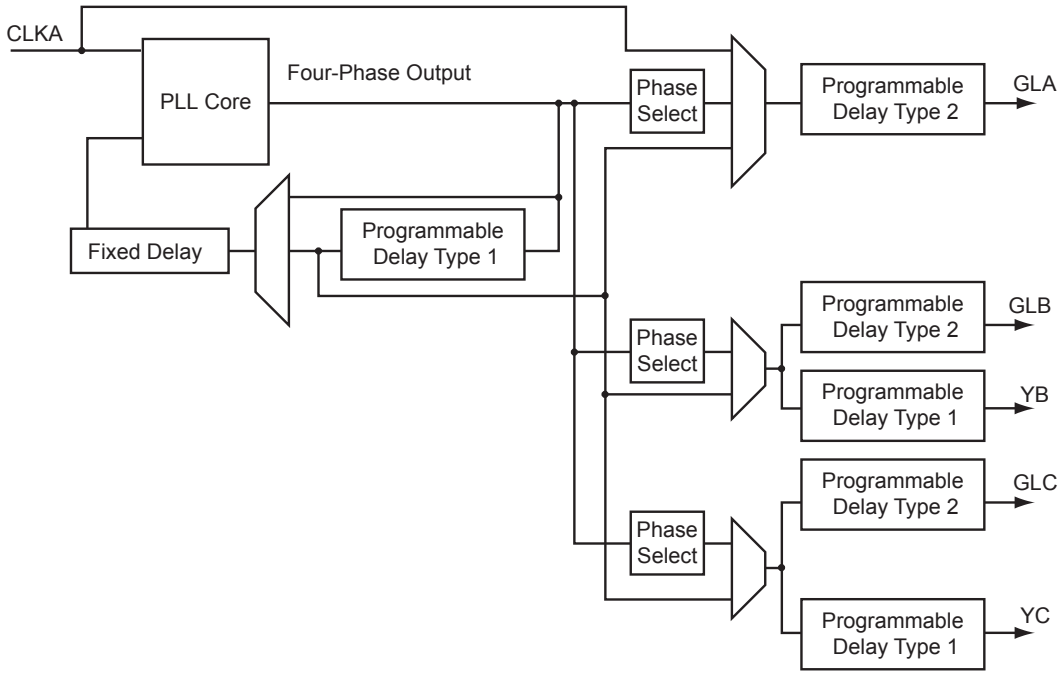
CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.

Figure 2-23 • **PLL Block**

Real-Time Counter (part of AB macro)

The RTC is a 40-bit loadable counter and used as the primary timekeeping element (Figure 2-29). The clock source, RTCCLK, must come from the CLKOUT signal of the crystal oscillator. The RTC can be configured to reset itself when a count value reaches the match value set in the Match Register.

The RTC is part of the Analog Block (AB) macro. The RTC is configured by the analog configuration MUX (ACM). Each address contains one byte of data. The circuitry in the RTC is powered by V_{CC33A}, so the RTC can be used in standby mode when the 1.5 V supply is not present.

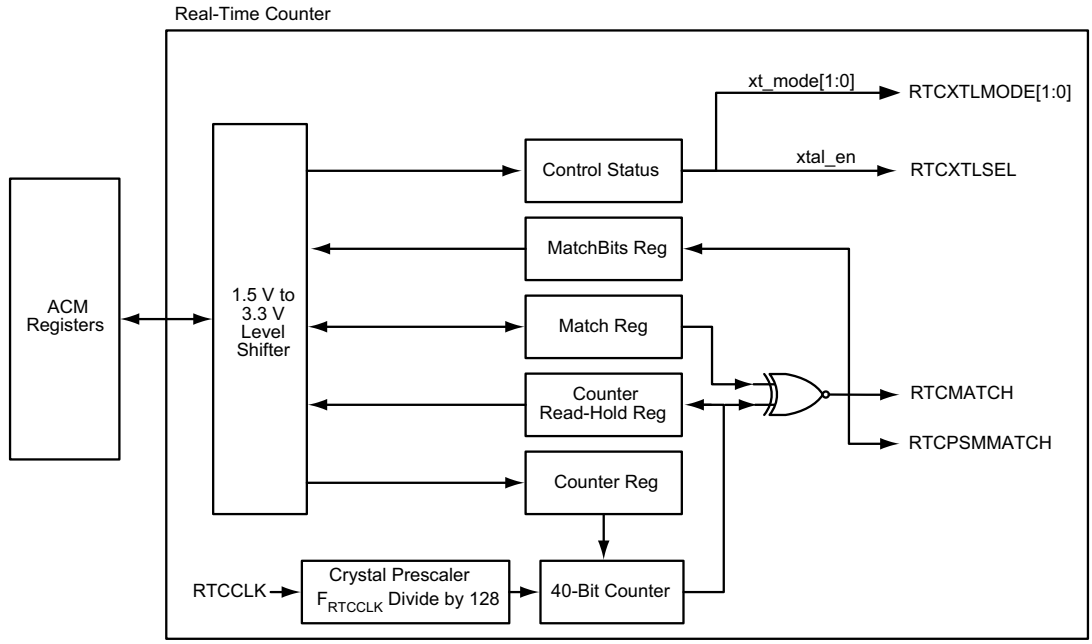


Figure 2-29 • **RTC Block Diagram**

Table 2-13 • **RTC Signal Description**

Signal Name	Width	Direction	Function
RTCCLK	1	In	Must come from CLKOUT of XTLOSC.
RTCXTLMODE[1:0]	2	Out	Controlled by xt_mode in CTRL_STAT. Signal must connect to the RTC_MODE signal in XTLOSC, as shown in Figure 2-27.
RTCXTLSEL	1	Out	Controlled by xtal_en from CTRL_STAT register. Signal must connect to RTC_MODE signal in XTLOSC in Figure 2-27.
RTCMATCH	1	Out	Match signal for FPGA 0 – Counter value does not equal the Match Register value. 1 – Counter value equals the Match Register value.
RTCPSMMATCH	1	Out	Same signal as RTCMATCH. Signal must connect to RTCPSMMATCH in VRPSM, as shown in Figure 2-27.

The 40-bit counter can be preloaded with an initial value as a starting point by the Counter Register. The count from the 40-bit counter can be read through the same set of address space. The count comes from a Read-Hold Register to avoid data changing during read.

When the counter value equals the Match Register value, all Match Bits Register values will be 0xFFFFFFFFFF. The RTCMATCH and RTCPSMMATCH signals will assert. The 40-bit counter can be configured to automatically reset to 0x0000000000 when the counter value equals the Match Register value. The automatic reset does not apply if the Match Register value is 0x0000000000.

The RTCCLK has a prescaler to divide the clock by 128 before it is used for the 40-bit counter. Below is an example of how to calculate the OFF time.

1.5 V Voltage Regulator

The 1.5 V voltage regulator uses an external pass transistor to generate 1.5 V from a 3.3 V supply. The base of the pass transistor is tied to PTBASE, the collector is tied to 3.3 V, and an emitter is tied to PTBASE and the 1.5 V supplies of the Fusion device. Figure 2-27 on page 2-31 shows the hook-up of the 1.5 V voltage regulator to an external pass transistor.

Microsemi recommends using a PN2222A or 2N2222A transistor. The gain of such a transistor is approximately 25, with a maximum base current of 20 mA. The maximum current that can be supported is 0.5 A. Transistors with different gain can also be used for different current requirements.

Table 2-17 • **Electrical Characteristics**
VCC33A = 3.3 V

Symbol	Parameter	Condition		Min	Typical	Max	Units
V_{OUT}	Output Voltage	T_J = 25ºC		1.425	1.5	1.575	V
I_{CC33A}	Operation Current	T_J = 25ºC	I_{LOAD} = 1 mA I_{LOAD} = 100 mA I_{LOAD} = 0.5 A		11 11 30		mA mA mA
Δ_{VOUT}	Load Regulation	T_J = 25ºC	I_{LOAD} = 1 mA to 0.5 A		90		mV
Δ_{VOUT}	Line Regulation	T_J = 25ºC	VCC33A = 2.97 V to 3.63 V I_{LOAD} = 1 mA VCC33A = 2.97 V to 3.63 V I_{LOAD} = 100 mA VCC33A = 2.97 V to 3.63 V I_{LOAD} = 500 mA		 10.6 12.1 10.6		 mV/V mV/V mV/V
	Dropout Voltage*	T_J = 25ºC	I_{LOAD} = 1 mA I_{LOAD} = 100 mA I_{LOAD} = 0.5 A		0.63 0.84 1.35		V V V
I_{PTBASE}	PTBase Current	T_J = 25ºC	I_{LOAD} = 1 mA I_{LOAD} = 100 mA I_{LOAD} = 0.5 A		48 736 12	 20	µA µA mA

*Note: *Data collected with 2N2222A.*

Embedded Memories

Fusion devices include four types of embedded memory: flash block, FlashROM, SRAM, and FIFO.

Flash Memory Block

Fusion is the first FPGA that offers a flash memory block (FB). Each FB block stores 2 Mbits of data. The flash memory block macro is illustrated in Figure 2-32. The port pin name and descriptions are detailed on Table 2-18 on page 2-40. All flash memory block signals are active high, except for CLK and active low RESET. All flash memory operations are synchronous to the rising edge of CLK.

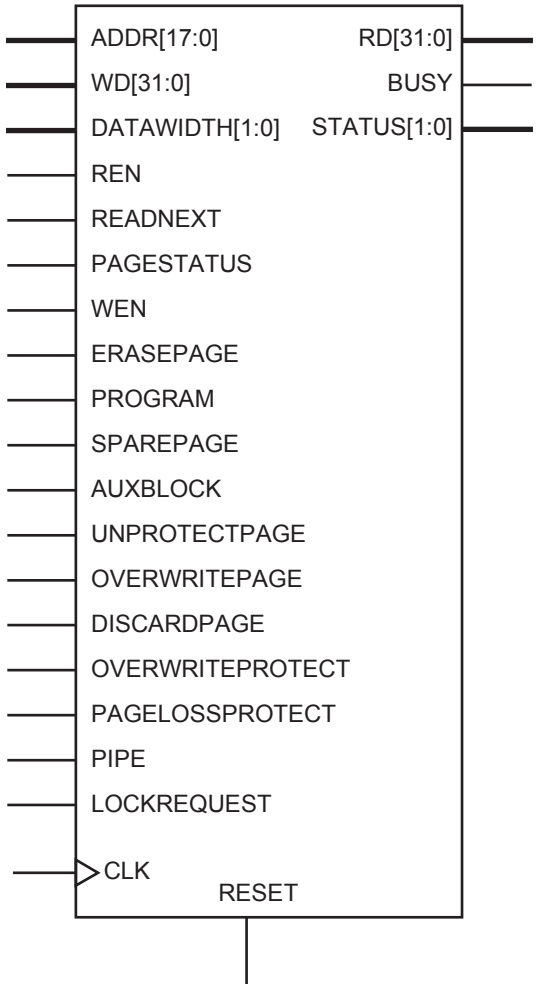


Figure 2-32 • **Flash Memory Block**

The following signals are used to configure the RAM4K9 memory element:

WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 2-26).

Table 2-26 • Allowable Aspect Ratio Settings for WIDTHA[1:0]

WIDTHA1, WIDTHA0	WIDTHB1, WIDTHB0	D×W
00	00	4k×1
01	01	2k×2
10	10	1k×4
11	11	512×9

Note: The aspect ratio settings are constant and cannot be changed on the fly.

BLKA and BLKB

These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, the corresponding port's outputs hold the previous value.

WENA and WENB

These signals switch the RAM between read and write mode for the respective ports. A Low on these signals indicates a write operation, and a High indicates a read.

CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A Low on PIPEA or PIPEB indicates a nonpipelined read, and the data appears on the corresponding output in the same clock cycle. A High indicates a pipelined, read and data appears on the corresponding output in the next clock cycle.

WMODEA and WMODEB

These signals are used to configure the behavior of the output when the RAM is in write mode. A Low on these signals makes the output retain data from the previous read. A High indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

RESET

This active low signal resets the output to zero, disables reads and writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.

ADDRA and ADDRB

These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 2-27).

Table 2-27 • Address Pins Unused/Used for Various Supported Bus Widths

	ADDRx	
D×W	Unused	Used
4k×1	None	[11:0]
2k×2	[11]	[10:0]
1k×4	[11:10]	[9:0]
512×9	[11:9]	[8:0]

Note: The "x" in ADDRx implies A or B.

Voltage Monitor

The Fusion Analog Quad offers a robust set of voltage-monitoring capabilities unique in the FPGA industry. The Analog Quad comprises three analog input pads—Analog Voltage (AV), Analog Current (AC), and Analog Temperature (AT)—and a single gate driver output pad, Analog Gate (AG). There are many common characteristics among the analog input pads. Each analog input can be configured to connect directly to the input MUX of the ADC. When configured in this manner (Figure 2-65), there will be no prescaling of the input signal. Care must be taken in this mode not to drive the ADC into saturation by applying an input voltage greater than the reference voltage. The internal reference voltage of the ADC is 2.56 V. Optionally, an external reference can be supplied by the user. The external reference can be a maximum of 3.3 V DC.

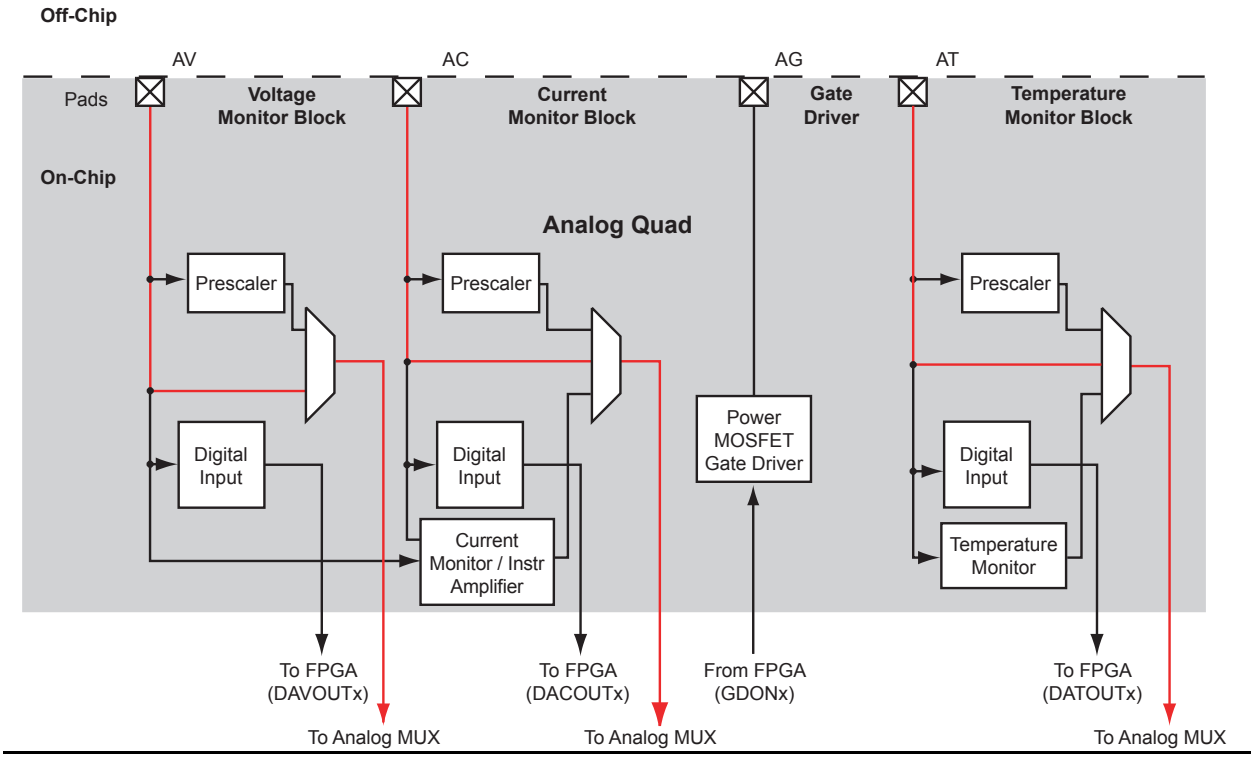


Figure 2-65 • **Analog Quad Direct Connect**

Current Monitor

The Fusion Analog Quad is an excellent element for voltage- and current-monitoring applications. In addition to supporting the same functionality offered by the AV pad, the AC pad can be configured to monitor current across an external sense resistor (Figure 2-69). To support this current monitor function, a differential amplifier with 10x gain passes the amplified voltage drop between the AV and AC pads to the ADC. The amplifier enables the user to use very small resistor values, thereby limiting any impact on the circuit. This function of the AC pad does not limit AV pad operation. The AV pad can still be configured for use as a direct voltage input or scaled through the AV prescaler independently of it's use as an input to the AC pad's differential amplifier.

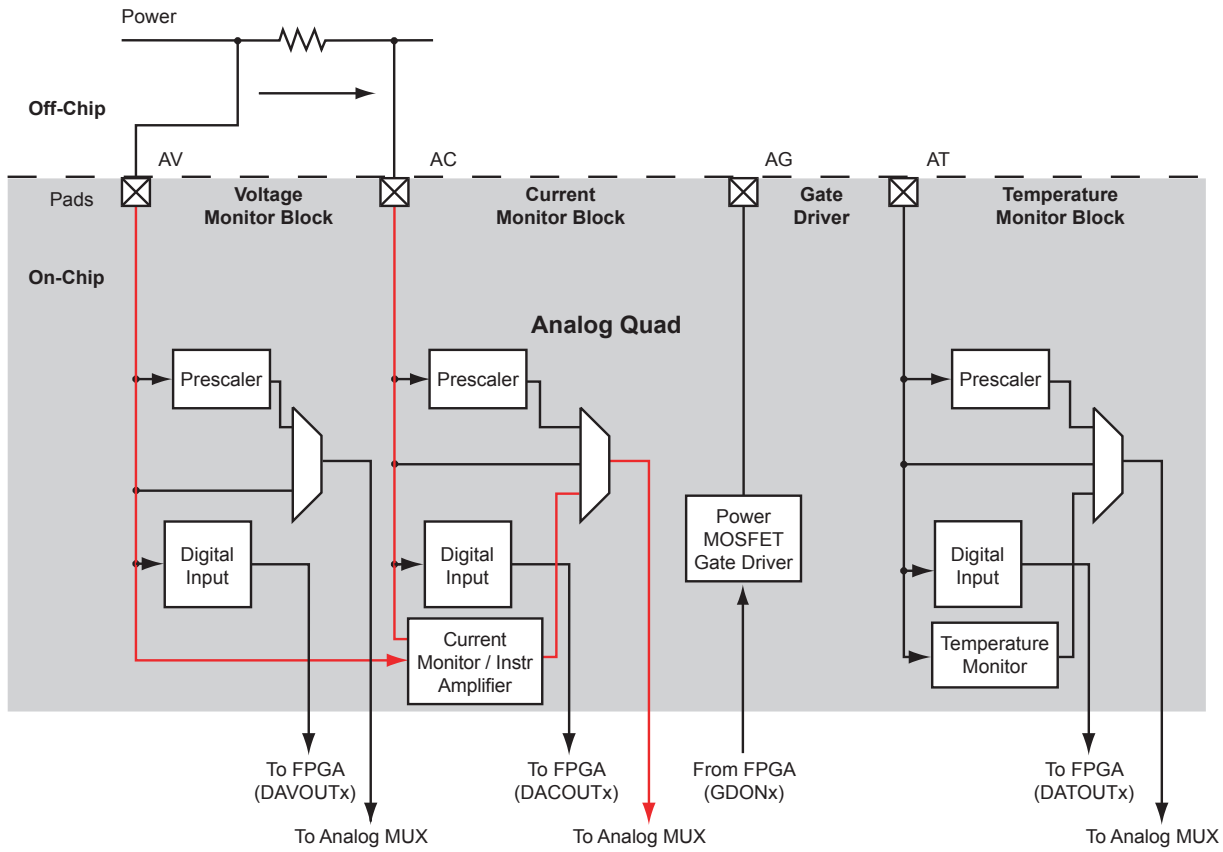


Figure 2-69 • **Analog Quad Current Monitor Configuration**

Gate Driver

The Fusion Analog Quad includes a Gate Driver connected to the Quad's AG pin (Figure 2-73). Designed to work with external p- or n-channel MOSFETs, the Gate driver is a configurable current sink or source and requires an external pull-up or pull-down resistor. The AG supports 4 selectable gate drive levels: 1 µA, 3 µA, 10 µA, and 30 µA (Figure 2-74 on page 2-91). The AG also supports a High Current Drive mode in which it can sink 20 mA; in this mode the switching rate is approximately 1.3 MHz with 100 ns turn-on time and 600 ns turn-off time. Modeled on an open-drain-style output, it does not output a voltage level without an appropriate pull-up or pull-down resistor. If 1 V is forced on the drain, the current sinking/sourcing will exceed the ability of the transistor, and the device could be damaged.

The AG pad is turned on via the corresponding GDON*x* pin in the Analog Block macro, where *x* is the number of the corresponding Analog Quad for the AG pad to be enabled (GDON0 to GDON9).

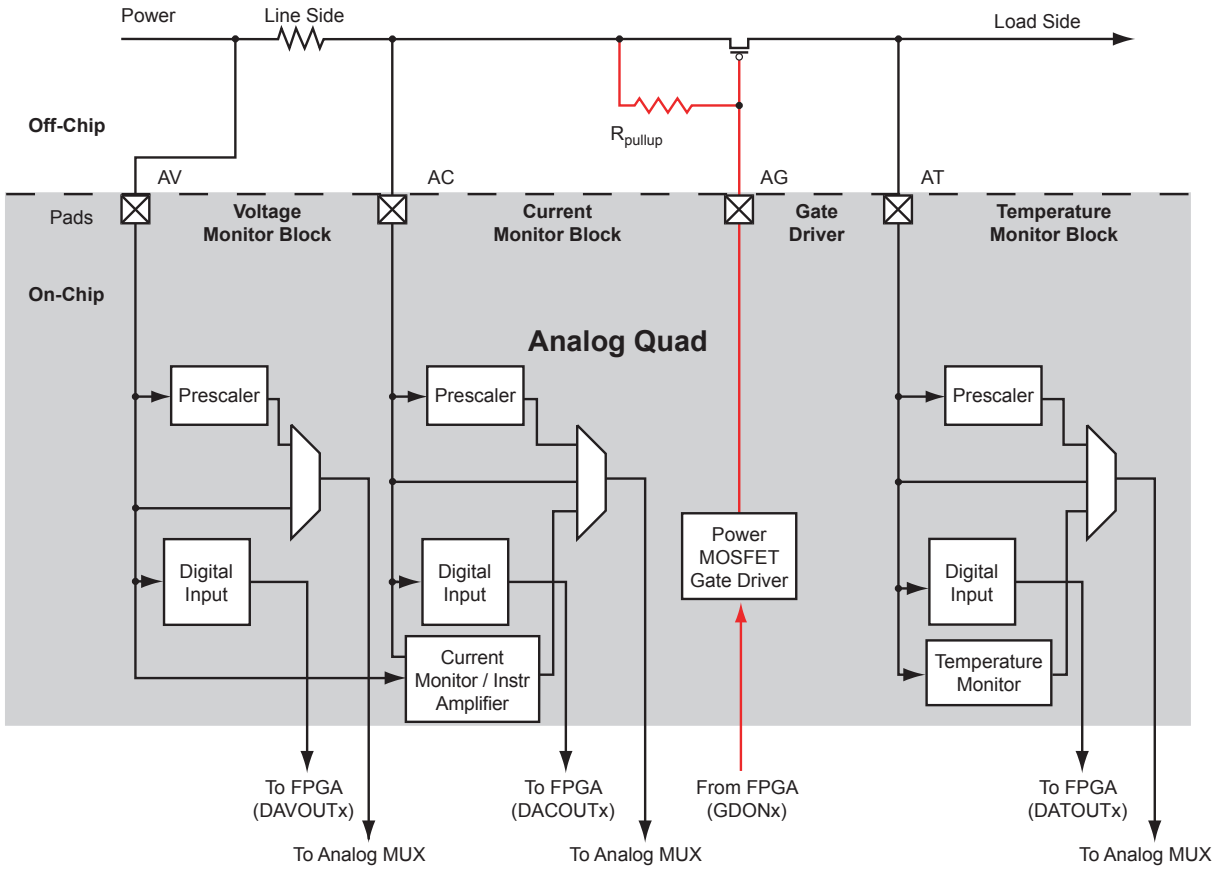


Figure 2-73 • **Gate Driver**

The gate-to-source voltage (V_{gs}) of the external MOSFET is limited to the programmable drive current times the external pull-up or pull-down resistor value (EQ 5).

$$V_{gs} \leq I_g \times (R_{pullup} \text{ or } R_{pulldown})$$

EQ 5

The rate at which the gate voltage of the external MOSFET slews is determined by the current, I_g, sourced or sunk by the AG pin and the gate-to-source capacitance, C_{GS}, of the external MOSFET. As an approximation, the slew rate is given by EQ 6.

$$dv/dt = I_g / C_{GS}$$

EQ 6

Table 2-57 details the settings available to control the prescaler values of the AV, AC, and AT pins. Note that the AT pin has a reduced number of available prescaler values.

Table 2-57 • **Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[2:0]	Scaling Factor, Pad to ADC Input	LSB for an 8-Bit Conversion (mV)[1]	LSB for a 10-Bit Conversion (mV)[1]	LSB for a 12-Bit Conversion (mV)[1]	Full Scale Voltage in 10-Bit Mode[2]	Range Name
000[3]	0.15625	64	16	4	16.368 V	16 V
001	0.3125	32	8	2	8.184 V	8 V
010[3]	0.625	16	4	1	4.092 V	4 V
011	1.25	8	2	0.5	2.046 V	2 V
100	2.5	4	1	0.25	1.023 V	1 V
101	5.0	2	0.5	0.125	0.5115 V	0.5 V
110	10.0	1	0.25	0.0625	0.25575 V	0.25 V
111	20.0	0.5	0.125	0.03125	0.127875 V	0.125 V

Notes:

1. *LSB voltage equivalences assume VAREF = 2.56 V.*
2. *Full Scale voltage for n-bit mode: ((2^n) - 1) x (LSB for a n-bit Conversion).*
3. *These are the only valid ranges for the temperature monitor block prescaler.*

Table 2-58 details the settings available to control the MUX within each of the AV, AC, and AT circuits. This MUX determines whether the signal routed to the ADC is the direct analog input, prescaled signal, or output of either the Current Monitor Block or the Temperature Monitor Block.

Table 2-58 • **Analog Multiplexer Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[4]	Control Lines Bx[3]	ADC Connected To
0	0	Prescaler
0	1	Direct input
1	0	Current amplifier* temperature monitor
1	1	Not valid

*Note: *Current monitor is not supported between –40°C and –55°C.*

Table 2-59 details the settings available to control the Direct Analog Input switch for the AV, AC, and AT pins.

Table 2-59 • **Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[5]	Direct Input Switch
0	Off
1	On

Table 2-60 details the settings available to control the polarity of the signals coming to the AV, AC, and AT pins. Note that the only valid setting for the AT pin is logic 0 to support positive voltages.

Table 2-60 • **Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)***

Control Lines Bx[6]	Input Signal Polarity
0 [1]	Positive

5 V Input Tolerance

I/Os can support 5 V input tolerance when LVTTL 3.3 V, LVCMOS 3.3 V, LVCMOS 2.5 V / 5 V, and LVCMOS 2.5 V configurations are used (see Table 2-78 on page 2-148 for more details). There are four recommended solutions (see Figure 2-102 to Figure 2-105 on page 2-147 for details of board and macro setups) to achieve 5 V receiver tolerance. All the solutions meet a common requirement of limiting the voltage at the input to 3.6 V or less. In fact, the I/O absolute maximum voltage rating is 3.6 V, and any voltage above 3.6 V may cause long-term gate oxide failures.

Solution 1

The board-level design needs to ensure that the reflected waveform at the pad does not exceed the limits provided in Table 3-4 on page 3-5. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI / PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the two external resistors, as explained below. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

The following are some examples of possible resistor values (based on a simplified simulation model with no line effects and 10 Ω transmitter output resistance, where Rtx_out_high = (VCCI – VOH) / I_{OH}, Rtx_out_low = VOL / I_{OL}).

Example 1 (high speed, high current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 36 Ω (±5%), P(r1)min = 0.069 Ω

R2 = 82 Ω (±5%), P(r2)min = 0.158 Ω

Imax_tx = 5.5 V / (82 * 0.95 + 36 * 0.95 + 10) = 45.04 mA

t_{RISE} = t_{FALL} = 0.85 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Example 2 (low–medium speed, medium current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 220 Ω (±5%), P(r1)min = 0.018 Ω

R2 = 390 Ω (±5%), P(r2)min = 0.032 Ω

Imax_tx = 5.5 V / (220 * 0.95 + 390 * 0.95 + 10) = 9.17 mA

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 20 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Other values of resistors are also allowed as long as the resistors are sized appropriately to limit the voltage at the receiving end to 2.5 V < Vin(rx) < 3.6 V when the transmitter sends a logic 1. This range of Vin_dc(rx) must be assured for any combination of transmitter supply (5 V ± 0.5 V), transmitter output resistance, and board resistor tolerances.

Table 2-109 • 2.5 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	12.02	0.05	1.38	0.44	11.83	12.02	2.82	2.33	14.19	14.38	ns
	–1	0.58	10.22	0.04	1.18	0.38	10.06	10.22	2.40	1.98	12.07	12.23	ns
	–2	0.51	8.97	0.03	1.03	0.33	8.83	8.97	2.11	1.74	10.59	10.74	ns
8 mA	Std.	0.68	8.39	0.05	1.38	0.44	8.55	8.24	3.22	3.05	10.91	10.60	ns
	–1	0.58	7.14	0.04	1.18	0.38	7.27	7.01	2.74	2.59	9.28	9.02	ns
	–2	0.51	6.27	0.03	1.03	0.33	6.38	6.15	2.40	2.28	8.15	7.91	ns
12 mA	Std.	0.68	6.52	0.05	1.38	0.44	6.64	6.24	3.48	3.50	8.99	8.60	ns
	–1	0.58	5.54	0.04	1.18	0.38	5.65	5.31	2.96	2.98	7.65	7.31	ns
	–2	0.51	4.87	0.03	1.03	0.33	4.96	4.66	2.60	2.62	6.72	6.42	ns
16 mA	Std.	0.68	6.08	0.05	1.38	0.44	6.19	5.83	3.54	3.63	8.55	8.18	ns
	–1	0.58	5.17	0.04	1.18	0.38	5.27	4.96	3.01	3.08	7.27	6.96	ns
	–2	0.51	4.54	0.03	1.03	0.33	4.62	4.35	2.65	2.71	6.38	6.11	ns
24 mA	Std.	0.68	5.81	0.05	1.38	0.44	5.80	5.81	3.62	4.08	8.16	8.16	ns
	–1	0.58	4.94	0.04	1.18	0.38	4.94	4.94	3.08	3.47	6.94	6.95	ns
	–2	0.51	4.34	0.03	1.03	0.33	4.33	4.34	2.70	3.05	6.09	6.10	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Timing Characteristics

Table 2-119 • 1.5 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	14.88	0.05	1.52	2.26	0.44	15.15	13.85	3.59	2.83	17.51	16.21	ns
	–1	0.58	12.66	0.04	1.29	1.92	0.38	12.89	11.78	3.05	2.40	14.90	13.79	ns
	–2	0.51	11.11	0.03	1.13	1.69	0.33	11.32	10.34	2.68	2.11	13.08	12.11	ns
4 mA	Std.	0.68	11.84	0.05	1.52	2.26	0.44	12.06	10.40	3.97	3.54	14.42	12.76	ns
	–1	0.58	10.07	0.04	1.29	1.92	0.38	10.26	8.85	3.38	3.01	12.27	10.86	ns
	–2	0.51	8.84	0.03	1.13	1.69	0.33	9.01	7.77	2.97	2.64	10.77	9.53	ns
6 mA	Std.	0.68	11.02	0.05	1.52	2.26	0.44	11.23	9.75	4.05	3.74	13.58	12.10	ns
	–1	0.58	9.38	0.04	1.29	1.92	0.38	9.55	8.29	3.45	3.18	11.56	10.30	ns
	–2	0.51	8.23	0.03	1.13	1.69	0.33	8.38	7.28	3.03	2.80	10.14	9.04	ns
8 mA	Std.	0.68	10.57	0.05	1.52	2.26	0.44	10.76	9.73	4.19	4.45	13.12	12.09	ns
	–1	0.58	8.99	0.04	1.29	1.92	0.38	9.15	8.28	3.56	3.78	11.16	10.29	ns
	–2	0.51	7.89	0.03	1.13	1.69	0.33	8.04	7.27	3.13	3.32	9.80	9.03	ns
12 mA	Std.	0.68	9.39	0.05	1.52	2.26	0.44	9.57	9.38	4.17	4.27	11.93	11.74	ns
	–1	0.58	2.99	0.04	1.29	1.92	0.38	8.14	7.98	3.55	3.63	10.14	9.98	ns
	–2	0.51	7.01	0.03	1.13	1.69	0.33	7.14	7.00	3.11	3.19	8.91	8.76	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-136 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
33 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33	124	169	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

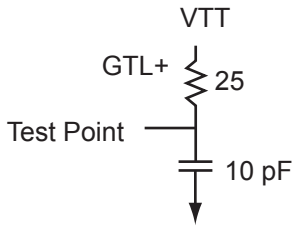


Figure 2-125 • AC Loading

Table 2-137 • 2.5 V GTL+ AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

Table 2-138 • 2.5 V GTL+
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.33	0.05	1.60	0.44	2.37	2.21			4.73	4.57	ns
–1	0.58	1.98	0.04	1.36	0.38	2.02	1.88			4.02	3.89	ns
–2	0.51	1.74	0.03	1.19	0.33	1.77	1.65			3.53	3.41	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Static Power Consumption of Various Internal Resources

***Table 3-13* • Different Components Contributing to the Static Power Consumption in Fusion Devices**

Parameter	Definition	Power Supply		Device-Specific Static Contributions		Units
		Name	Setting	AFS1500	AFS600	
PDC1	Core static power contribution in operating mode	VCC	1.5 V	18	7.5	mW
PDC2	Device static power contribution in sleep mode*	VCC33A	3.3 V	0.66		mW
PDC3	Device static power contribution in standby mode	VCC33A	3.3 V	0.03		mW
PDC4	NVM static power contribution	VCC	1.5 V	1.19		mW
PDC5	Analog Block static power contribution of ADC	VCC33A	3.3 V	8.25		mW
PDC6	Analog Block static power contribution per Quad	VCC33A	3.3 V	3.3		mW
PDC7	Static contribution per input pin – standard dependent contribution	VCCI	See Table 3-10 on page 3-15			
PDC8	Static contribution per output pin – standard dependent contribution	VCCI	See Table 3-11 on page 3-17			
PDC9	Static contribution for PLL	VCC	1.5 V	2.55		mW

*Note: *Sleep mode is not supported between –40°C and –55°C.*

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of NVM blocks used in the design
- The number of Analog Quads used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 3-14 on page 3-23.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 3-15 on page 3-23.
- Read rate and write rate to the RAM—guidelines are provided for typical applications in Table 3-15 on page 3-23.
- Read rate to the NVM blocks

The calculation should be repeated for each clock domain defined in the design.

FG256		
Pin Number	AFS600 Function	AFS1500 Function
A1	GND	GND
A2	VCCIB0	VCCIB0
A3	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
A4	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0
A5	GND	GND
A6	IO10PDB0V1	IO07PDB0V1
A7	IO12PDB0V1	IO13PDB0V2
A8	IO12NDB0V1	IO13NDB0V2
A9	IO22NDB1V0	IO24NDB1V0
A10	IO22PDB1V0	IO24PDB1V0
A11	IO24NDB1V1	IO29NDB1V1
A12	GND	GND
A13	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2
A14	IO29NDB1V1	IO43NDB1V2
A15	VCCIB1	VCCIB1
A16	GND	GND
B1	V_{COMPLA}	VCOMPLA
B2	VCCPLA	VCCPLA
B3	IO00NDB0V0	IO00NDB0V0
B4	IO00PDB0V0	IO00PDB0V0
B5	GAB1/IO02PPB0V0	GAB1/IO02PPB0V0
B6	IO10NDB0V1	IO07NDB0V1
B7	VCCIB0	VCCIB0
B8	IO18NDB1V0	IO22NDB1V0
B9	IO18PDB1V0	IO22PDB1V0
B10	VCCIB1	VCCIB1
B11	IO24PDB1V1	IO29PDB1V1
B12	GBC0/IO26NPB1V1	GBC0/IO40NPB1V2
B13	GBA1/IO28PDB1V1	GBA1/IO42PDB1V2
B14	IO29PDB1V1	IO43PDB1V2
B15	VCCPLB	VCCPLB
B16	VCOMPLB	VCOMPLB
C1	VCCIB4	VCCIB4
C2	GND	GND
C3	VCCIB4	VCCIB4
C4	VCCIB0	VCCIB0
C5	VCCIB0	VCCIB0

FG256		
Pin Number	AFS600 Function	AFS1500 Function
C6	GAC1/IO03PDB0V0	GAC1/IO03PDB0V0
C7	IO06NDB0V0	IO09NDB0V1
C8	IO16PDB1V0	IO23PDB1V0
C9	IO16NDB1V0	IO23NDB1V0
C10	IO25NDB1V1	IO31NDB1V1
C11	IO25PDB1V1	IO31PDB1V1
C12	VCCIB1	VCCIB1
C13	GBC1/IO26PPB1V1	GBC1/IO40PPB1V2
C14	VCCIB2	VCCIB2
C15	GND	GND
C16	VCCIB2	VCCIB2
D1	IO84NDB4V0	IO124NDB4V0
D2	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0
D3	IO85NDB4V0	IO125NDB4V0
D4	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0
D5	GAB0/IO02NPB0V0	GAB0/IO02NPB0V0
D6	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0
D7	IO06PDB0V0	IO09PDB0V1
D8	IO14NDB0V1	IO15NDB0V2
D9	IO14PDB0V1	IO15PDB0V2
D10	IO23PDB1V1	IO37PDB1V2
D11	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2
D12	VCCIB1	VCCIB1
D13	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0
D14	IO30NDB2V0	IO44NDB2V0
D15	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0
D16	IO31NDB2V0	IO45NDB2V0
E1	GND	GND
E2	IO81NDB4V0	IO118NDB4V0
E3	IO81PDB4V0	IO118PDB4V0
E4	VCCIB4	VCCIB4
E5	IO83NPB4V0	IO123NPB4V0
E6	IO04NPB0V0	IO05NPB0V1
E7	GND	GND
E8	IO08PDB0V1	IO11PDB0V1
E9	IO20NDB1V0	IO27NDB1V1
E10	GND	GND

FG484		
Pin Number	AFS600 Function	AFS1500 Function
L17	VCCIB2	VCCIB2
L18	IO46PDB2V0	IO69PDB2V0
L19	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0
L20	VCCIB2	VCCIB2
L21	GCC0/IO43NDB2V0	GCC0/IO62NDB2V0
L22	GCC1/IO43PDB2V0	GCC1/IO62PDB2V0
M1	NC	IO103PDB4V0
M2	XTAL1	XTAL1
M3	VCCIB4	VCCIB4
M4	GNDOSC	GNDOSC
M5	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0
M6	VCCIB4	VCCIB4
M7	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0
M8	VCCIB4	VCCIB4
M9	VCC	VCC
M10	GND	GND
M11	VCC	VCC
M12	GND	GND
M13	VCC	VCC
M14	GND	GND
M15	VCCIB2	VCCIB2
M16	IO48NDB2V0	IO70NDB2V0
M17	VCCIB2	VCCIB2
M18	IO46NDB2V0	IO69NDB2V0
M19	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0
M20	VCCIB2	VCCIB2
M21	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0
M22	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0
N1	NC	IO103NDB4V0
N2	GND	GND
N3	IO68PDB4V0	IO101PDB4V0
N4	NC	IO100NPB4V0
N5	GND	GND
N6	NC	IO99PDB4V0
N7	NC	IO97PDB4V0

FG484		
Pin Number	AFS600 Function	AFS1500 Function
N8	GND	GND
N9	GND	GND
N10	VCC	VCC
N11	GND	GND
N12	VCC	VCC
N13	GND	GND
N14	VCC	VCC
N15	GND	GND
N16	GDB2/IO56PDB2V0	GDB2/IO83PDB2V0
N17	NC	IO78PDB2V0
N18	GND	GND
N19	IO47NDB2V0	IO72NDB2V0
N20	IO47PDB2V0	IO72PDB2V0
N21	GND	GND
N22	IO49PDB2V0	IO71PDB2V0
P1	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0
P2	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0
P3	IO68NDB4V0	IO101NDB4V0
P4	IO65PDB4V0	IO96PDB4V0
P5	IO65NDB4V0	IO96NDB4V0
P6	NC	IO99NDB4V0
P7	NC	IO97NDB4V0
P8	VCCIB4	VCCIB4
P9	VCC	VCC
P10	GND	GND
P11	VCC	VCC
P12	GND	GND
P13	VCC	VCC
P14	GND	GND
P15	VCCIB2	VCCIB2
P16	IO56NDB2V0	IO83NDB2V0
P17	NC	IO78NDB2V0
P18	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0
P19	GDB1/IO53PDB2V0	GDB1/IO80PDB2V0
P20	IO51NDB2V0	IO73NDB2V0