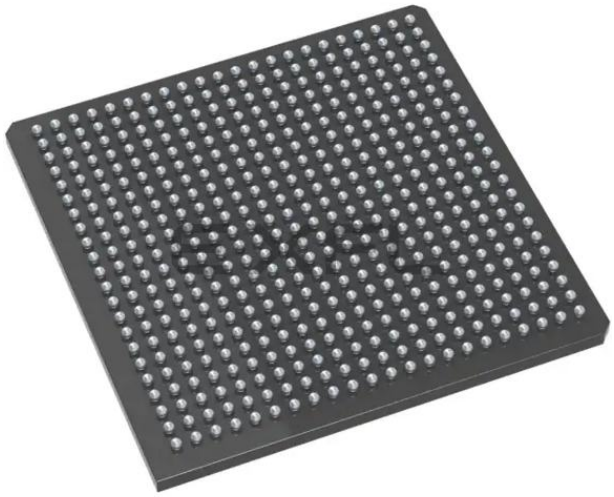

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-1fg484k

The on-chip crystal and RC oscillators work in conjunction with the integrated phase-locked loops (PLLs) to provide clocking support to the FPGA array and on-chip resources. In addition to supporting typical RTC uses such as watchdog timer, the Fusion RTC can control the on-chip voltage regulator to power down the device (FPGA fabric, flash memory block, and ADC), enabling a low power standby mode.

The Fusion family offers revolutionary features, never before available in an FPGA. The nonvolatile flash technology gives the Fusion solution the advantage of being a secure, low power, single-chip solution that is Instant On. Fusion is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flash-based Fusion devices are Instant On and do not need to be loaded from an external boot PROM. On-board security mechanisms prevent access to the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades, with confidence that valuable IP cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm with MAC data authentication on the device. The Fusion family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the Fusion family a cost-effective ASIC replacement solution for applications in the consumer, networking and communications, computing, and avionics markets.

Security

As the nonvolatile, flash-based Fusion family requires no boot PROM, there is no vulnerable external bitstream. Fusion devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Fusion devices utilize a 128-bit flash-based key lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the industry-leading AES-128 block cipher encryption standard (FIPS Publication 192). The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the DES standard, which was adopted in 1977. Fusion devices have a built-in AES decryption engine and a flash-based AES key that make Fusion devices the most comprehensive programmable logic device security solution available today. Fusion devices with AES-based security provide a high level of protection for remote field updates over public networks, such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the Fusion family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. Fusion with FlashLock and AES security is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. A Fusion device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Fusion FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

The system application, Level 3, is the larger user application that utilizes one or more applets. Designing at the highest level of abstraction supported by the Fusion technology stack, the application can be easily created in FPGA gates by importing and configuring multiple applets.

In fact, in some cases an entire FPGA system design can be created without any HDL coding.

An optional MCU enables a combination of software and HDL-based design methodologies. The MCU can be on-chip or off-chip as system requirements dictate. System portioning is very flexible, allowing the MCU to reside above the applets or to absorb applets, or applets and backbone, if desired.

The Fusion technology stack enables a very flexible design environment. Users can engage in design across a continuum of abstraction from very low to very high.

Core Architecture

VersaTile

Based upon successful ProASIC3/E logic architecture, Fusion devices provide granularity comparable to gate arrays. The Fusion device core consists of a sea-of-VersaTiles architecture.

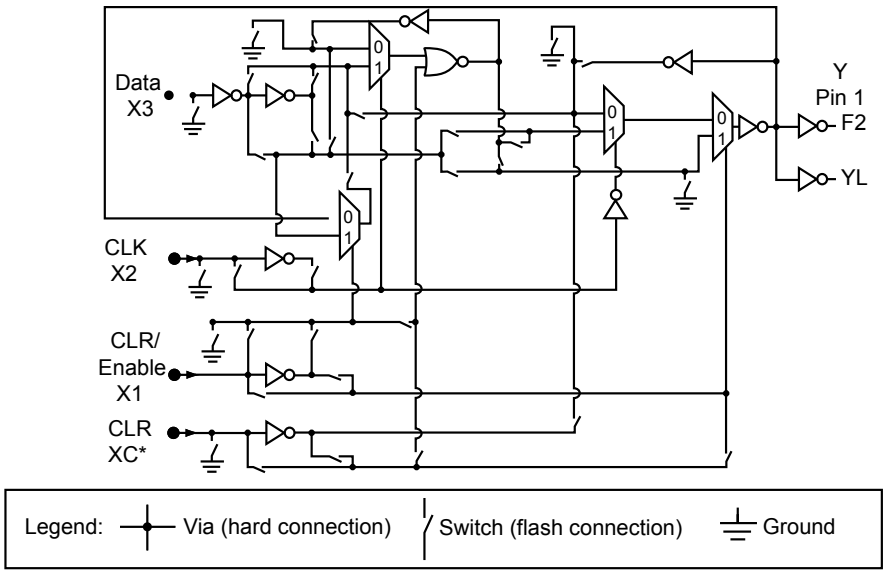
As illustrated in Figure 2-2, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a 4th input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR signal is supported by a fourth input, which can only be routed to the core cell over the VersaNet (global) network.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources (Figure 2-2).



*Note: *This input can only be connected to the global clock distribution network.*

Figure 2-2 • **Fusion Core VersaTile**

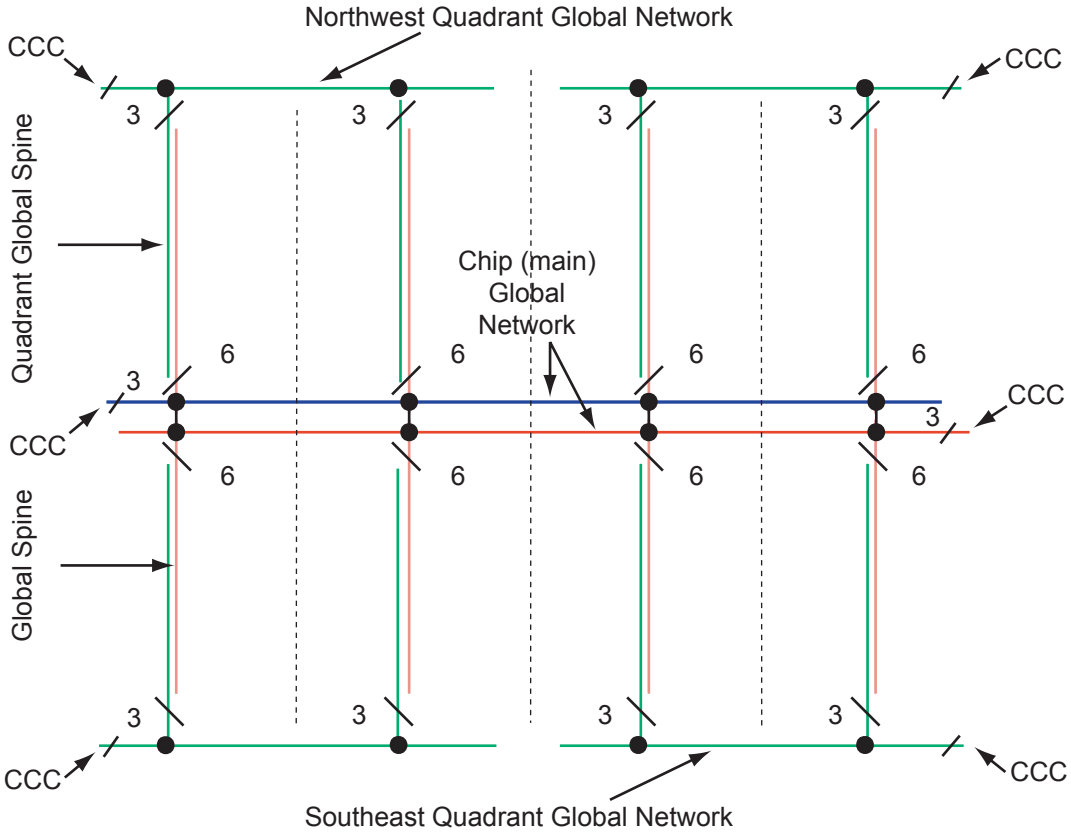


Figure 2-12 • **Global Network Architecture**

Table 2-4 • **Globals/Spines/Rows by Device**

	AFS600	AFS1500
Global VersaNets (trees)*	9	9
VersaNet Spines/Tree	12	20
Total Spines	108	180
VersaTiles in Each Top or Bottom Spine	1,152	1,920
Total VersaTiles	13,824	38,400

*Note: *There are six chip (main) globals and three globals per quadrant.*

Clock Conditioning Circuits

In Fusion devices, the CCCs are used to implement frequency division, frequency multiplication, phase shifting, and delay operations.

The CCCs are available in six chip locations—each of the four chip corners and the middle of the east and west chip sides.

Each CCC can implement up to three independent global buffers (with or without programmable delay), or a PLL function (programmable frequency division/multiplication, phase shift, and delays) with up to three global outputs. Unused global outputs of a PLL can be used to implement independent global buffers, up to a maximum of three global outputs for a given CCC.

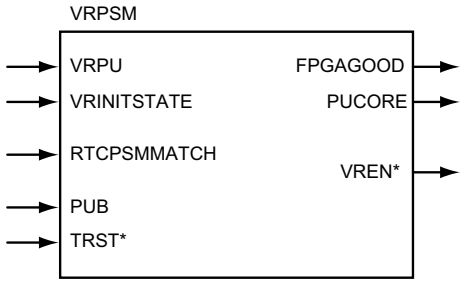
A global buffer can be placed in any of the three global locations (CLKA-GLA, CLKB-GLB, and CLKC-GLC) of a given CCC.

A PLL macro uses the CLKA CCC input to drive its reference clock. It uses the GLA and, optionally, the GLB and GLC global outputs to drive the global networks. A PLL macro can also drive the YB and YC regular core outputs. The GLB (or GLC) global output cannot be reused if the YB (or YC) output is used (Figure 2-19). Refer to the "PLL Macro" section on page 2-27 for more information.

Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core

The CCC block is fully configurable, either via flash configuration bits set in the programming bitstream or through an asynchronous interface. This asynchronous interface is dynamically accessible from inside the Fusion device to permit changes of parameters (such as divide ratios) during device operation. To increase the versatility and flexibility of the clock conditioning system, the CCC configuration is determined either by the user during the design process, with configuration data being stored in flash memory as part of the device programming procedure, or by writing data into a dedicated shift register during normal device operation. This latter mode allows the user to dynamically reconfigure the CCC without the need for core programming. The shift register is accessed through a simple serial interface. Refer to the "UJTAG Applications in Microsemi's Low-Power Flash Devices" chapter of the *Fusion FPGA Fabric User's Guide* and the "CCC and PLL Characteristics" section on page 2-28 for more information.



*Note: *Signals are hardwired internally and do not exist in the macro core.*

Figure 2-30 • **VRPSM Macro**

Table 2-16 • **VRPSM Signal Descriptions**

Signal Name	Width	Dir.	Function
VRPU	1	In	Voltage Regulator Power-Up 0 – Voltage regulator disabled. PUB must be floated or pulled up, and the TRST pin must be grounded to disable the voltage regulator. 1 – Voltage regulator enabled
VRINITSTATE	1	In	Voltage Regulator Initial State Defines the voltage regulator status upon power-up of the 3.3 V. The signal is configured by Libero SoC when the VRPSM macro is generated. Tie off to 1 – Voltage regulator enables when 3.3 V is powered. Tie off to 0 – Voltage regulator disables when 3.3 V is powered.
RTCPSMMATCH	1	In	RTC Power System Management Match Connect from RTCPSMATCH signal from RTC in AB 0 transition to 1 turns on the voltage regulator
PUB	1	In	External pin, built-in weak pull-up Power-Up bar 0 – Enables voltage regulator at all times
TRST*	1	In	External pin, JTAG Test Reset 1 – Enables voltage regulator at all times
FPGAGOOD	1	Out	Indicator that the FPGA is powered and functional No need to connect if it is not used. 1 – Indicates that the FPGA is powered up and functional. 0 – Not possible to read by FPGA since it has already powered off.
PUCORE	1	Out	Power-Up Core Inverted signal of PUB. No need to connect if it is not used.
VREN*	1	Out	Voltage Regulator Enable Connected to 1.5 V voltage regulator in Fusion device internally. 0 – Voltage regulator disables 1 – Voltage regulator enables

*Note: *Signals are hardwired internally and do not exist in the macro core.*

1.5 V Voltage Regulator

The 1.5 V voltage regulator uses an external pass transistor to generate 1.5 V from a 3.3 V supply. The base of the pass transistor is tied to PTBASE, the collector is tied to 3.3 V, and an emitter is tied to PTBASE and the 1.5 V supplies of the Fusion device. Figure 2-27 on page 2-31 shows the hook-up of the 1.5 V voltage regulator to an external pass transistor.

Microsemi recommends using a PN2222A or 2N2222A transistor. The gain of such a transistor is approximately 25, with a maximum base current of 20 mA. The maximum current that can be supported is 0.5 A. Transistors with different gain can also be used for different current requirements.

Table 2-17 • **Electrical Characteristics**
VCC33A = 3.3 V

Symbol	Parameter	Condition		Min	Typical	Max	Units
V_{OUT}	Output Voltage	T_J = 25ºC		1.425	1.5	1.575	V
I_{CC33A}	Operation Current	T_J = 25ºC	I_{LOAD} = 1 mA I_{LOAD} = 100 mA I_{LOAD} = 0.5 A		11 11 30		mA mA mA
Δ_{VOUT}	Load Regulation	T_J = 25ºC	I_{LOAD} = 1 mA to 0.5 A		90		mV
Δ_{VOUT}	Line Regulation	T_J = 25ºC	VCC33A = 2.97 V to 3.63 V I_{LOAD} = 1 mA VCC33A = 2.97 V to 3.63 V I_{LOAD} = 100 mA VCC33A = 2.97 V to 3.63 V I_{LOAD} = 500 mA		 10.6 12.1 10.6		 mV/V mV/V mV/V
	Dropout Voltage*	T_J = 25ºC	I_{LOAD} = 1 mA I_{LOAD} = 100 mA I_{LOAD} = 0.5 A		0.63 0.84 1.35		V V V
I_{PTBASE}	PTBase Current	T_J = 25ºC	I_{LOAD} = 1 mA I_{LOAD} = 100 mA I_{LOAD} = 0.5 A		48 736 12	 20	µA µA mA

*Note: *Data collected with 2N2222A.*

Table 2-18 • **Flash Memory Block Pin Names (continued)**

Interface Name	Width	Direction	Description
STATUS[1:0]	2	Out	Status of the last operation completed: 00: Successful completion 01: Read-/Unprotect-Page: single error detected and corrected Write: operation addressed a write-protected page Erase-Page: protection violation Program: Page Buffer is unmodified Protection violation 10: Read-/Unprotect-Page: two or more errors detected 11: Write: attempt to write to another page before programming current page Erase-Page/Program: page write count has exceeded the 10-year retention threshold
UNPROTECTPAGE	1	In	When asserted, the page addressed is copied into the Page Buffer and the Page Buffer is made writable.
WD[31:0]	32	In	Write data
WEN	1	In	When asserted, stores WD in the page buffer.

All flash memory block input signals are active high, except for RESET.

Table 2-24 • Flash Memory Block Timing, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V (continued)

Parameter	Description	–2	–1	Std.	Units
$t_{SUPGLOSSPRO}$	Page Loss Protect Setup Time for the Control Logic	1.74	1.99	2.34	ns
$t_{HDPGLOSSPRO}$	Page Loss Protect Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUPGSTAT}$	Page Status Setup Time for the Control Logic	2.56	2.92	3.43	ns
$t_{HDPGSTAT}$	Page Status Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUOVERWRPG}$	Over Write Page Setup Time for the Control Logic	1.94	2.21	2.60	ns
$t_{HDOVERWRPG}$	Over Write Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SULOCKREQUEST}$	Lock Request Setup Time for the Control Logic	0.90	1.02	1.20	ns
$t_{HDLOCKREQUEST}$	Lock Request Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{RECARNVM}$	Reset Recovery Time	0.97	1.10	1.29	ns
$t_{REMARNVM}$	Reset Removal Time	0.00	0.00	0.00	ns
$t_{MPWARNVM}$	Asynchronous Reset Minimum Pulse Width for the Control Logic	12.50	15.63	15.63	ns
$t_{MPWCLKNVM}$	Clock Minimum Pulse Width for the Control Logic	5.00	6.25	6.25	ns
$t_{FMAXCLKNVM}$	Maximum Frequency for Clock for the Control Logic	80.00	64.00	64.00	MHz

Timing Characteristics

Table 2-34 • FIFO, Worst Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup time	5.01	5.70	6.70	ns
t_{ENH}	REN, WEN Hold time	0.02	0.02	0.03	ns
t_{BKS}	BLK Setup time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold time	0.00	0.00	0.00	ns
t_{DS}	Input data (WD) Setup time	0.19	0.22	0.25	ns
t_{DH}	Input data (WD) Hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.43	2.77	3.25	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.92	1.05	1.23	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.77	2.02	2.37	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.68	1.92	2.25	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.38	7.27	8.55	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.75	1.99	2.34	ns
t_{RSTAF}	RESET Low to Almost-Empty/Full Flag Valid	6.32	7.20	8.46	ns
t_{RSTBQ}	RESET Low to Data out Low on RD (flow-through)	0.95	1.08	1.27	ns
	RESET Low to Data out Low on RD (pipelined)	0.95	1.08	1.27	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.34	0.39	ns
$t_{RECRSTB}$	RESET Recovery	1.55	1.76	2.07	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.22	0.25	0.29	ns
t_{CYC}	Clock Cycle time	3.33	3.79	4.46	ns
FMAX	Maximum Frequency for FIFO	300	264	224	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10 for derating values.

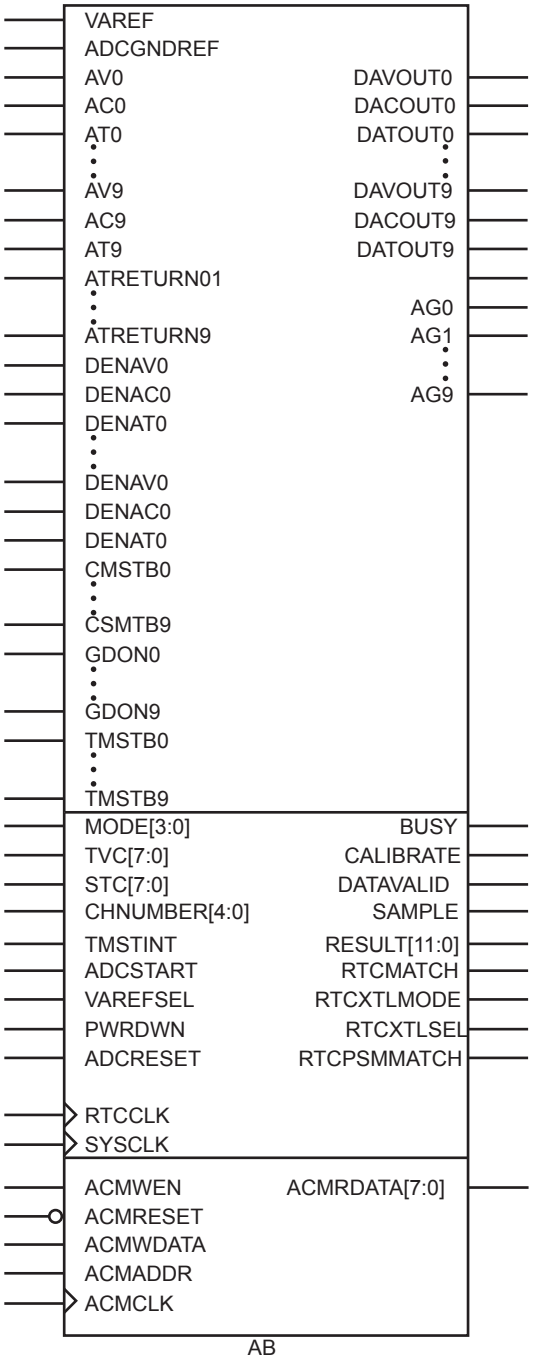


Figure 2-63 • **Analog Block Macro**

User I/Os

Introduction

Fusion devices feature a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. Table 2-68, Table 2-69, Table 2-70, and Table 2-71 on page 2-136 show the voltages and the compatible I/O standards. I/Os provide programmable slew rates, drive strengths, weak pull-up, and weak pull-down circuits. 3.3 V PCI and 3.3 V PCI-X are 5 V–tolerant. See the "5 V Input Tolerance" section on page 2-145 for possible implementations of 5 V tolerance.

All I/Os are in a known state during power-up, and any power-up sequence is allowed without current impact. Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset" section on page 3-6 for more information. In low power standby or sleep mode (V_{CC} is OFF, V_{CC33A} is ON, V_{CCI} is ON) or when the resource is not used, digital inputs are tristated, digital outputs are tristated, and digital bibufs (input/output) are tristated.

I/O Tile

The Fusion I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile in selected I/O banks can be used to support high-performance register inputs and outputs, with register enable if desired (Figure 2-98 on page 2-134). The registers can also be used to support the JESD-79C DDR standard within the I/O structure (see the "Double Data Rate (DDR) Support" section on page 2-140 for more information).

As depicted in Figure 2-99 on page 2-139, all I/O registers share one CLR port. The output register and output enable register share one CLK port. Refer to the "I/O Registers" section on page 2-139 for more information.

I/O Banks and I/O Standards Compatibility

The digital I/Os are grouped into I/O voltage banks. There are four digital I/O banks on the AFS600 and AFS1500 devices. Figure 2-112 on page 2-159 shows the bank configuration. The north side of the I/O in the AFS600 and AFS1500 devices comprises two banks of Pro I/Os. The Pro I/Os support a wide number of voltage-referenced I/O standards in addition to the multitude of single-ended and differential I/O standards common throughout all digital I/Os. Each I/O voltage bank has dedicated I/O supply and ground voltages (VCCI/GNDQ for input buffers and V_{CCI}/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. Table 2-69 and Table 2-70 on page 2-135 show the required voltage compatibility values for each of these voltages.

For more information about I/O and global assignments to I/O banks, refer to the specific pin table of the device in the "Pin Assignments" section on page 4-1 and the "User I/O Naming Convention" section on page 2-159.

Each Pro I/O bank is divided into minibanks. Any user I/O in a VREF minibank (a minibank is the region of scope of a VREF pin) can be configured as a VREF pin (Figure 2-98 on page 2-134). Only one VREF pin is needed to control the entire VREF minibank. The location and scope of the VREF minibanks can be determined by the I/O name. For details, see the "User I/O Naming Convention" section on page 2-159.

Table 2-70 on page 2-135 shows the I/O standards supported by Fusion devices and the corresponding voltage levels.

I/O standards are compatible if the following are true:

- Their VCCI values are identical.
- If both of the standards need a VREF, their VREF values must be identical (Pro I/O only).

Table 2-83 • **Fusion Pro I/O Supported Standards and Corresponding VREF and VTT Voltages Applicable to all I/O Bank types**

I/O Standard	Input/Output Supply Voltage (VMVtyp/VCCI_TYP)	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_TYP)
LVTTL/LVCMOS 3.3 V	3.30 V	–	–
LVCMOS 2.5 V	2.50 V	–	–
LVCMOS 2.5 V / 5.0 V Input	2.50 V	–	–
LVCMOS 1.8 V	1.80 V	–	–
LVCMOS 1.5 V	1.50 V	–	–
PCI 3.3 V	3.30 V	–	–
PCI-X 3.3 V	3.30 V	–	–
GTL+ 3.3 V	3.30 V	1.00 V	1.50 V
GTL+ 2.5 V	2.50 V	1.00 V	1.50 V
GTL 3.3 V	3.30 V	0.80 V	1.20 V
GTL 2.5 V	2.50 V	0.80 V	1.20 V
HSTL Class I	1.50 V	0.75 V	0.75 V
HSTL Class II	1.50 V	0.75 V	0.75 V
SSTL3 Class I	3.30 V	1.50 V	1.50 V
SSTL3 Class II	3.30 V	1.50 V	1.50 V
SSTL2 Class I	2.50 V	1.25 V	1.25 V
SSTL2 Class II	2.50 V	1.25 V	1.25 V
LVDS	2.50 V	–	–
LVPECL	3.30 V	–	–

Table 2-103 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J =100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	8.31	0.05	1.27	1.65	0.44	8.47	7.07	2.84	2.73	10.82	9.43	ns
	–1	0.58	7.07	0.04	1.08	1.40	0.38	7.20	6.01	2.41	2.32	9.21	8.02	ns
	–2	0.51	6.21	0.03	0.95	1.23	0.33	6.32	5.28	2.12	2.04	8.08	7.04	s
8 mA	Std.	0.68	5.35	0.05	1.27	1.65	0.44	5.45	4.37	3.21	3.39	7.81	6.73	ns
	–1	0.58	4.55	0.04	1.08	1.40	0.38	4.64	3.72	2.73	2.88	6.64	5.72	ns
	–2	0.51	4.00	0.03	0.95	1.23	0.33	4.07	3.26	2.40	2.53	5.83	5.02	ns
12 mA	Std.	0.68	3.87	0.05	1.27	1.65	0.44	3.94	3.03	3.45	3.81	6.30	5.38	ns
	–1	0.58	3.29	0.04	1.08	1.40	0.38	3.35	2.57	2.94	3.24	5.36	4.58	ns
	–2	0.51	2.89	0.03	0.95	1.23	0.33	2.94	2.26	2.58	2.85	4.70	4.02	ns
16 mA	Std.	0.68	3.65	0.05	1.27	1.65	0.44	3.72	2.75	3.51	3.93	6.08	5.11	ns
	–1	0.58	3.11	0.04	1.08	1.40	0.38	3.16	2.34	2.99	3.34	5.17	4.34	ns
	–2	0.51	2.73	0.03	0.95	1.23	0.33	2.78	2.05	2.62	2.93	4.54	3.81	ns
24 mA	Std.	0.68	3.38	0.05	1.27	1.65	0.44	3.44	2.27	3.57	4.35	5.80	4.63	ns
	–1	0.58	2.88	0.04	1.08	1.40	0.38	2.93	1.93	3.04	3.70	4.94	3.94	ns
	–2	0.51	2.53	0.03	0.95	1.23	0.33	2.57	1.70	2.67	3.25	4.33	3.46	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Differential I/O Characteristics

Configuration of the I/O modules as a differential pair is handled by the Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-132. The building blocks of the LVDS transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

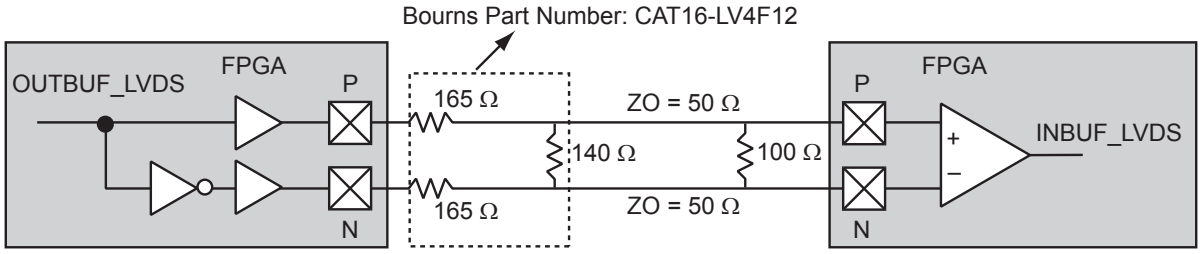


***Figure 2-132* • LVDS Circuit Diagram and Board-Level Implementation**

***Table 2-157* • LVDS Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL [1]	Output Lower Current	0.65	0.91	1.16	mA
IOH [1]	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIL [2,3]	Input High Leakage Current			10	µA
IIH [2,4]	Input Low Leakage Current			10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350		mV

Notes:

1. *IOL/IOH defined by* I/O diff*/(Resistor Network)*
2. *Currents are measured at 85°C junction temperature.*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

***Table 2-165* • Parameter Definitions and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L,DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

*Note: *See Figure 2-135 on page 2-211 for more information.*

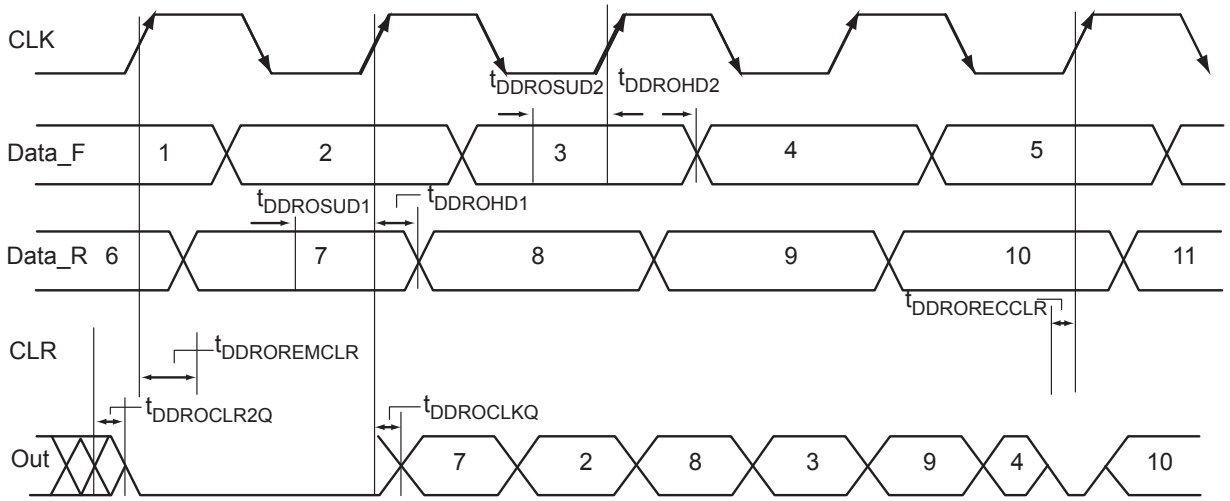


***Figure 2-143* • Output DDR Timing Diagram**

Timing Characteristics

***Table 2-173* • Output DDR Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.72	0.82	0.97	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.39	0.44	0.52	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.39	0.43	0.52	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.83	0.94	1.11	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	0.26	0.31	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.36	0.41	0.48	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.37	0.43	ns
FDDOMAX	Maximum Frequency for the Output DDR	1,404	1,232	1,048	MHz

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Don't Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

NCAP **Negative Capacitor**

Negative Capacitor is where the negative terminal of the charge pump capacitor is connected. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP.

PCAP **Positive Capacitor**

Positive Capacitor is where the positive terminal of the charge pump capacitor is connected. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP.

PUB **Push Button**

Push button is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator and can be floating if not used.

PTBASE **Pass Transistor Base**

Pass Transistor Base is the control signal of the voltage regulator. This pin should be connected to the base of the external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.

PTEM **Pass Transistor Emitter**

Pass Transistor Emitter is the feedback input of the voltage regulator.

This pin should be connected to the emitter of the external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.

XTAL1 **Crystal Oscillator Circuit Input**

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

XTAL2 **Crystal Oscillator Circuit Input**

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

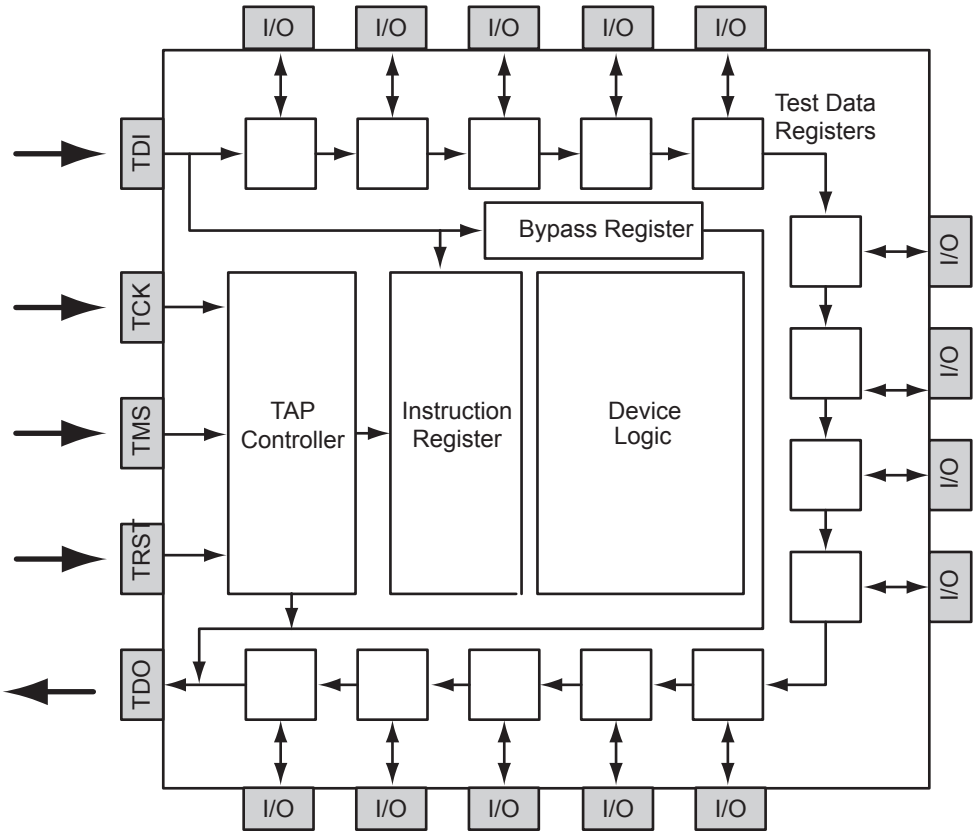


***Figure 2-144* • Boundary Scan Chain in Fusion**

***Table 2-176* • Boundary Scan Opcodes**

	Hex Opcode
EXTEST	00
HIGHZ	07
USERCODE	0E
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF

Static Power Consumption of Various Internal Resources

***Table 3-13* • Different Components Contributing to the Static Power Consumption in Fusion Devices**

Parameter	Definition	Power Supply		Device-Specific Static Contributions		Units
		Name	Setting	AFS1500	AFS600	
PDC1	Core static power contribution in operating mode	VCC	1.5 V	18	7.5	mW
PDC2	Device static power contribution in sleep mode*	VCC33A	3.3 V	0.66		mW
PDC3	Device static power contribution in standby mode	VCC33A	3.3 V	0.03		mW
PDC4	NVM static power contribution	VCC	1.5 V	1.19		mW
PDC5	Analog Block static power contribution of ADC	VCC33A	3.3 V	8.25		mW
PDC6	Analog Block static power contribution per Quad	VCC33A	3.3 V	3.3		mW
PDC7	Static contribution per input pin – standard dependent contribution	VCCI	See Table 3-10 on page 3-15			
PDC8	Static contribution per output pin – standard dependent contribution	VCCI	See Table 3-11 on page 3-17			
PDC9	Static contribution for PLL	VCC	1.5 V	2.55		mW

*Note: *Sleep mode is not supported between –40°C and –55°C.*

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of NVM blocks used in the design
- The number of Analog Quads used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 3-14 on page 3-23.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 3-15 on page 3-23.
- Read rate and write rate to the RAM—guidelines are provided for typical applications in Table 3-15 on page 3-23.
- Read rate to the NVM blocks

The calculation should be repeated for each clock domain defined in the design.

Standby Mode and Sleep Mode

$P_{OUTPUTS}$ = 0 W

RAM Dynamic Contribution—P_{MEMORY}

Operating Mode

$P_{MEMORY} = (N_{BLOCKS} * PAC11 * \beta_2 * F_{READ\text{-}CLOCK}) + (N_{BLOCKS} * PAC12 * \beta_3 * F_{WRITE\text{-}CLOCK})$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 3-15 on page 3-23.

β_3 the RAM enable rate for write operations—guidelines are provided in Table 3-15 on page 3-23.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

Standby Mode and Sleep Mode

P_{MEMORY} = 0 W

PLL/CCC Dynamic Contribution—P_{PLL}

Operating Mode

$P_{PLL} = PAC13 * F_{CLKOUT}$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

Standby Mode and Sleep Mode

P_{PLL} = 0 W

Nonvolatile Memory Dynamic Contribution—P_{NVM}

Operating Mode

The NVM dynamic power consumption is a piecewise linear function of frequency.

$P_{NVM} = N_{NVM\text{-}BLOCKS} * \beta_4 * PAC15 * F_{READ\text{-}NVM}$ when $F_{READ\text{-}NVM} \leq 33$ MHz,

$P_{NVM} = N_{NVM\text{-}BLOCKS} * \beta_4 *(PAC16 + PAC17 * F_{READ\text{-}NVM}$ when $F_{READ\text{-}NVM} > 33$ MHz

$N_{NVM\text{-}BLOCKS}$ is the number of NVM blocks used in the design (2 inAFS600).

β_4 is the NVM enable rate for read operations. Default is 0 (NVM mainly in idle state).

$F_{READ\text{-}NVM}$ is the NVM read clock frequency.

Standby Mode and Sleep Mode

P_{NVM} = 0 W

Crystal Oscillator Dynamic Contribution—$P_{XTL\text{-}OSC}$

Operating Mode

$P_{XTL\text{-}OSC} = PAC18$

Standby Mode

$P_{XTL\text{-}OSC} = PAC18$

Sleep Mode

$P_{XTL\text{-}OSC}$ = 0 W

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*