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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	119
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-1fgg256k

VersaTile Characteristics

Sample VersaTile Specifications—Combinatorial Module

The Fusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library (Figure 2-3). For more details, refer to the *IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide*.

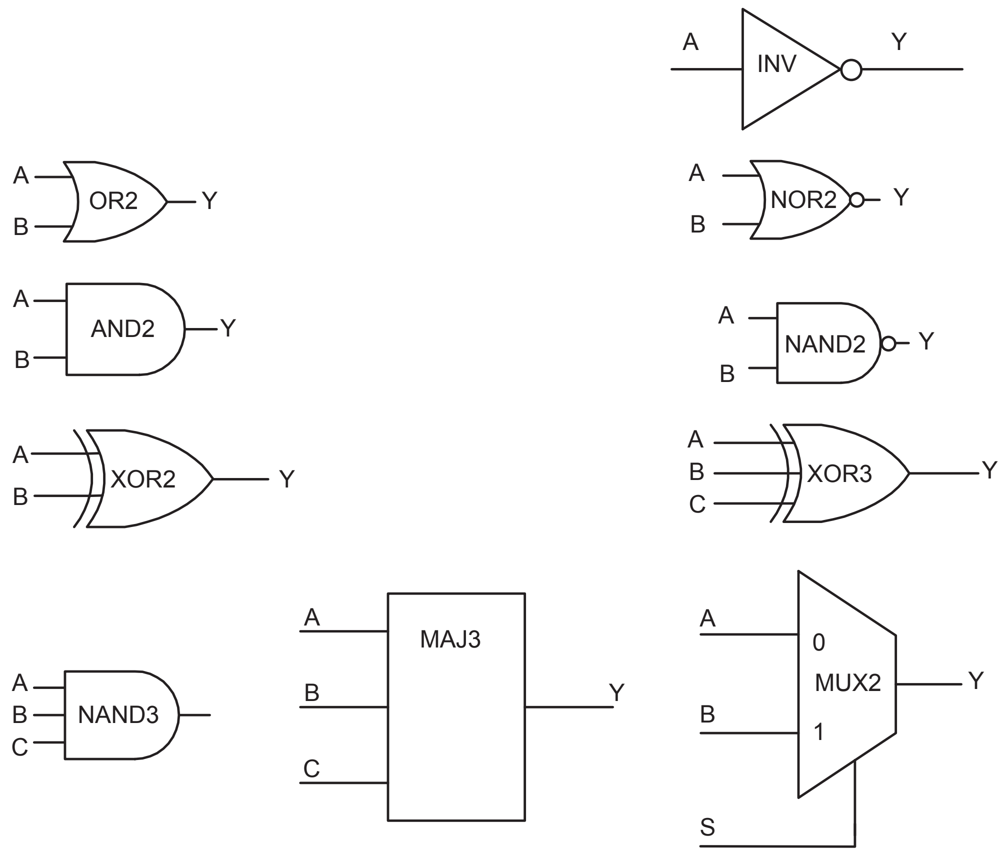


Figure 2-3 • **Sample of Combinatorial Cells**

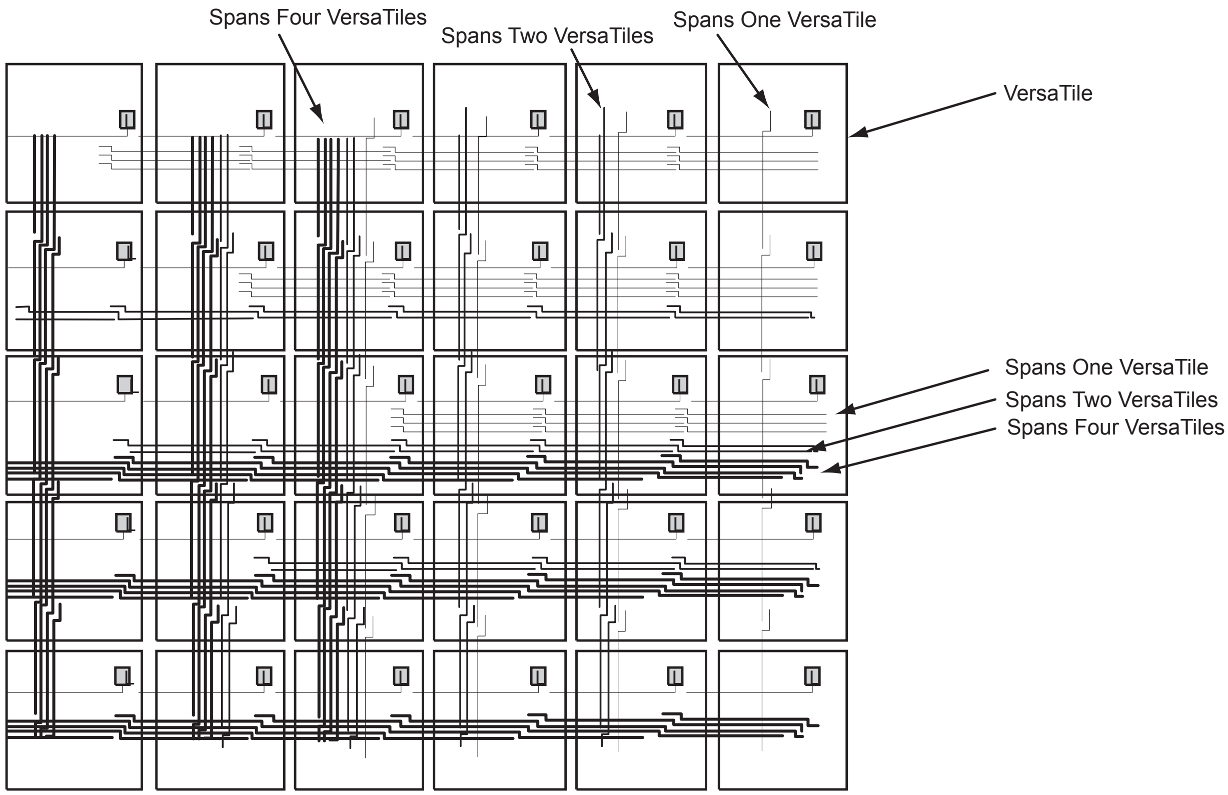


Figure 2-9 • **Efficient Long-Line Resources**

PLL Macro

The PLL functionality of the clock conditioning block is supported by the PLL macro. Note that the PLL macro reference clock uses the CLKA input of the CCC block, which is only accessible from the global A[2:0] package pins. Refer to Figure 2-22 on page 2-25 for more information.

The PLL macro provides five derived clocks (three independent) from a single reference clock. The PLL feedback loop can be driven either internally or externally. The PLL macro also provides power-down input and lock output signals. During power-up, POWERDOWN should be asserted Low until V_{CC} is up. See Figure 2-19 on page 2-22 for more information.

Inputs:

- CLKA: selected clock input
- POWERDOWN (active low): disables PLLs. The default state is power-down on (active low).

Outputs:

- LOCK (active high): indicates that PLL output has locked on the input reference signal
- GLA, GLB, GLC: outputs to respective global networks
- YB, YC: allows output from the CCC to be routed back to the FPGA core

As previously described, the PLL allows up to five flexible and independently configurable clock outputs. Figure 2-23 on page 2-26 illustrates the various clock output options and delay elements.

As illustrated, the PLL supports three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global networks, respectively, and/or routed to the device core (YB and YC).

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

There is also a delay element in the feedback loop that can be used to advance the clock relative to the reference clock.

The PLL macro reference clock can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate it from the hardwired I/O connection described earlier.

The visual PLL configuration in SmartGen, available with the Libero SoC and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user. SmartGen allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLKA) and the derived clocks (GLA, GLB, GLC, YB, and YC). SmartGen also allows the user to select where the input clock is coming from. SmartGen automatically instantiates the special macro, PLLINT, when needed.

The NGMUX macro is simplified to show the two clock options that have been selected by the GLMUXCFG[1:0] bits. Figure 2-25 illustrates the NGMUX macro. During design, the two clock sources are connected to CLK0 and CLK1 and are controlled by GLMUXSEL[1:0] to determine which signal is to be passed through the MUX.

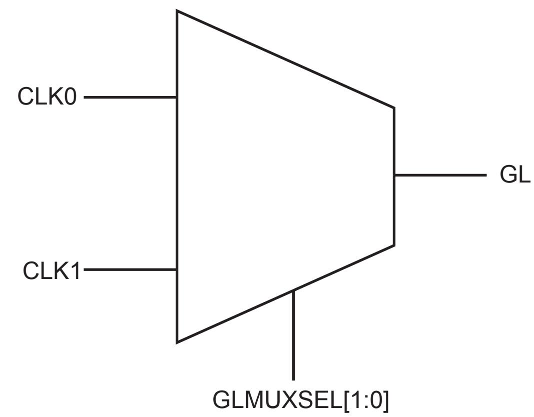


Figure 2-25 **• NGMUX Macro**

The sequence of switching between two clock sources (from CLK0 to CLK1) is as follows (Figure 2-26):

- GLMUXSEL[1:0] transitions to initiate a switch.
- GL drives one last complete CLK0 positive pulse (i.e., one rising edge followed by one falling edge).
- From that point, GL stays Low until the second rising edge of CLK1 occurs.
- At the second CLK1 rising edge, GL will begin to continuously deliver the CLK1 signal.
- Minimum t_{sw} = 0.05 ns at 25°C (typical conditions)

For examples of NGMUX operation, refer to the *Fusion FPGA Fabric User's Guide*.

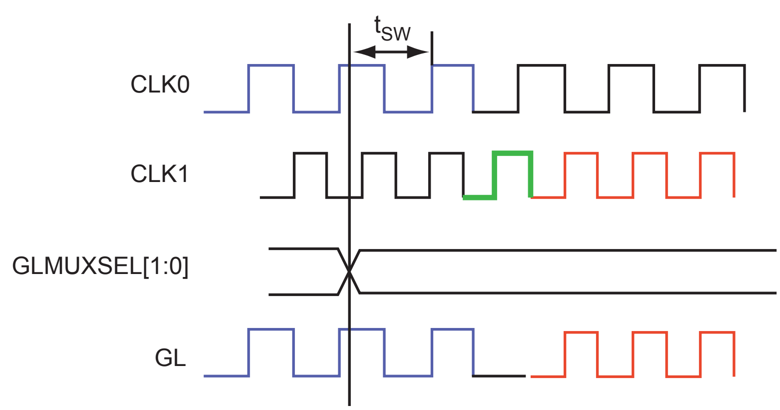


Figure 2-26 **• NGMUX Waveform**

Real-Time Counter System

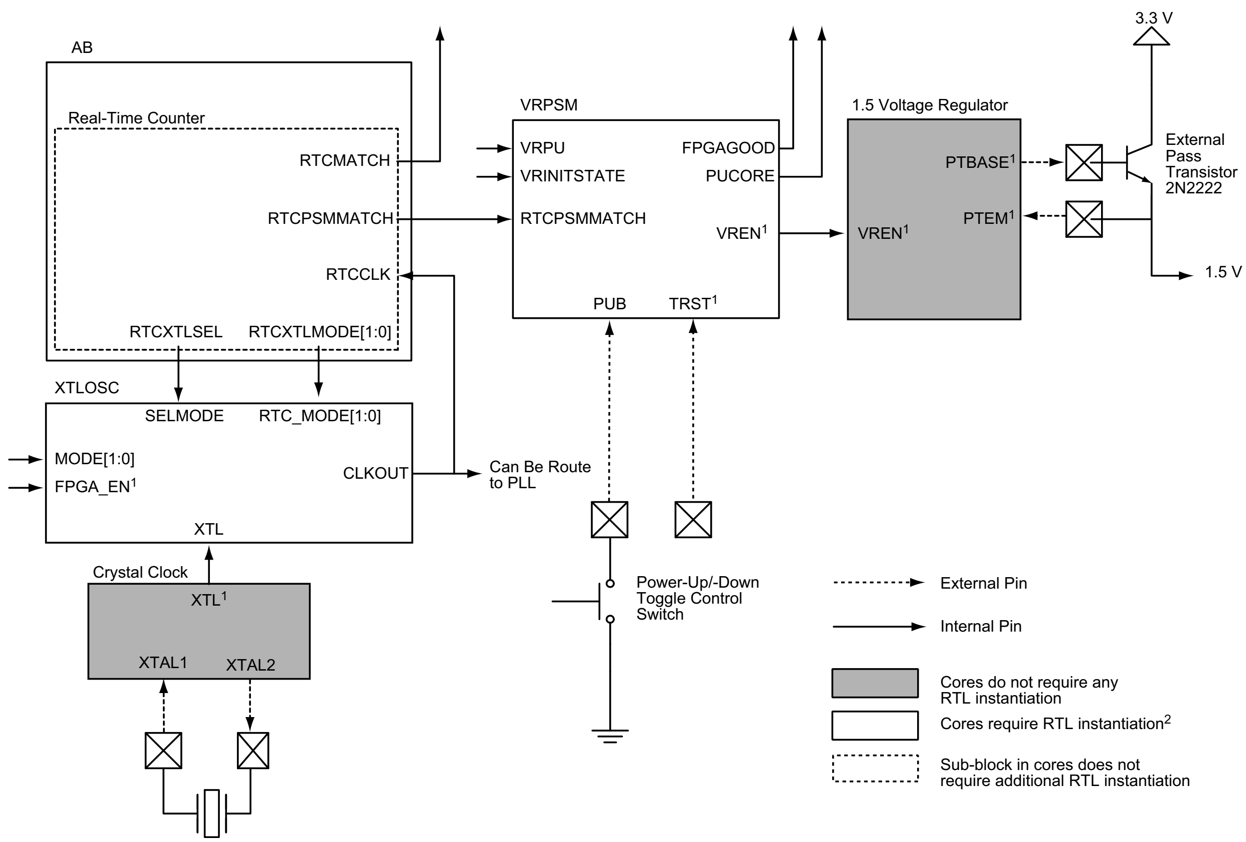
The RTC system enables Fusion devices to support standby and sleep modes of operation to reduce power consumption in many applications.

- Sleep mode, typical 10 µA
- Standby mode (RTC running), typical 3 mA with 20 MHz

The RTC system is composed of five cores:

- RTC sub-block inside Analog Block (AB)
- Voltage Regulator and Power System Monitor (VRPSM)
- Crystal oscillator (XTLOSC); refer to the "Crystal Oscillator" section in the Fusion Clock Resources chapter of the *Fusion FPGA Fabric User's Guide* for more detail.
- Crystal clock; does not require instantiation in RTL
- 1.5 V voltage regulator; does not require instantiation in RTL

All cores are powered by 3.3 V supplies, so the RTC system is operational without a 1.5 V supply during standby mode. Figure 2-27 shows their connection.



Notes:

1. *Signals are hardwired internally and do not exist in the macro core.*
2. *User is only required to instantiate the VRPSM macro if the user wishes to specify PUPO behavior of the voltage regulator to be different from the default, or employ user logic to shut the voltage regulator off.*

***Figure 2-27* • Real-Time Counter System (not all the signals are shown for the AB macro)**

Unprotect Page Operation

An Unprotect Page operation will clear the protection for a page addressed on the ADDR input. It is initiated by setting the UNPROTECTPAGE signal on the interface along with the page address on ADDR.

If the page is not in the Page Buffer, the Unprotect Page operation will copy the page into the Page Buffer. The Copy Page operation occurs only if the current page in the Page Buffer is not Page Loss Protected.

The waveform for an Unprotect Page operation is shown in Figure 2-42.

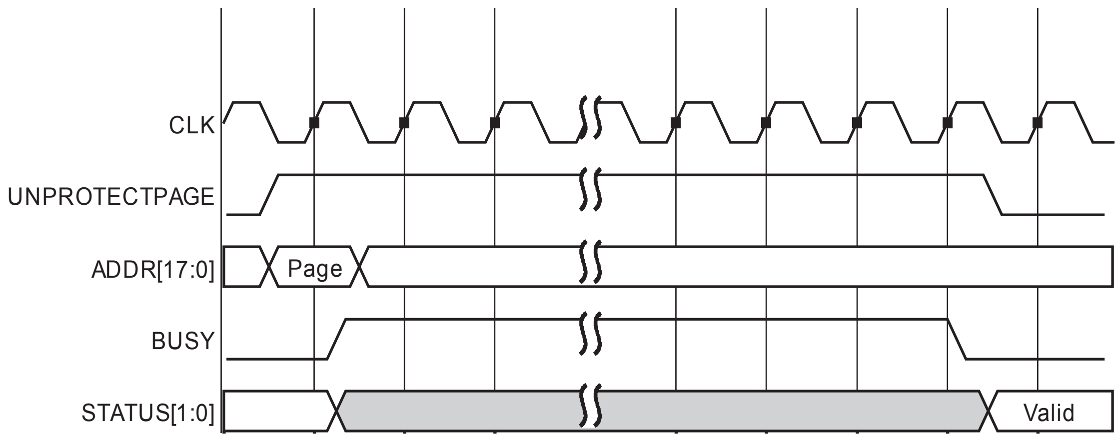


Figure 2-42 **• FB Unprotected Page Waveform**

The Unprotect Page operation can incur the following error conditions:

1. If the copy of the page to the Page Buffer determines that the page has a single-bit correctable error in the data, it will report a STATUS = '01'.
2. If the address on ADDR does not match the address of the Page Buffer, PAGELOSSPROTECT is asserted, and the Page Buffer has been modified, then STATUS = '11' and the addressed page is not loaded into the Page Buffer.
3. If the copy of the page to the Page Buffer determines that at least one block in the page has a double-bit uncorrectable error, STATUS = '10' and the Page Buffer will contain the corrupted data.

Discard Page Operation

If the contents of the modified Page Buffer have to be discarded, the DISCARDPAGE signal should be asserted. This command results in the Page Buffer being marked as unmodified.

The timing for the operation is shown in Figure 2-43. The BUSY signal will remain asserted until the operation has completed.

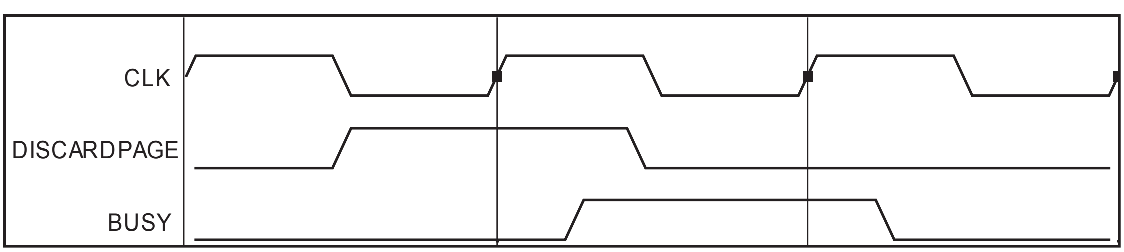


Figure 2-43 **• FB Discard Page Waveform**

SRAM and FIFO

All Fusion devices have SRAM blocks along the north side of the device. Additionally, AFS600 and AFS1500 devices have an SRAM block on the south side of the device. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz. The following configurations are available:

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—two read, two write or one read, one write)
- 512×9, 256×18 (two-port RAM—one read and one write)
- Sync write, sync pipelined/nonpipelined read

The Fusion SRAM memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY).

During RAM operation, addresses are sourced by the user logic, and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to Figure 2-47 for more information about the implementation of the embedded FIFO controller.

The Fusion architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. This is done with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1. For example, the write size can be set to 256×18 and the read size to 512×9.

Both the write and read widths for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in Table 2-26 on page 2-58.

When a width of one, two, or four is selected, the ninth bit is unused. For example, when writing 9-bit values and reading 4-bit values, only the first four bits and the second four bits of each 9-bit value are addressable for read operations. The ninth bit is not accessible.

Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.

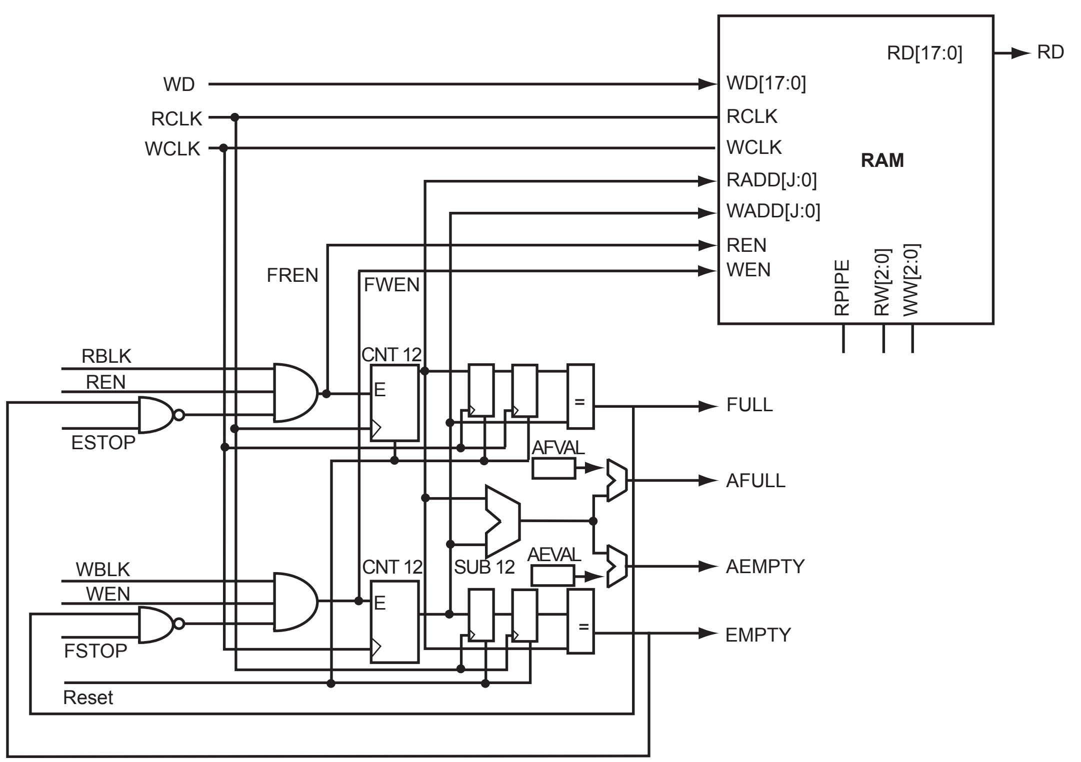


Figure 2-47 **• Fusion RAM Block with Embedded FIFO Controller**

RAM4K9 Description

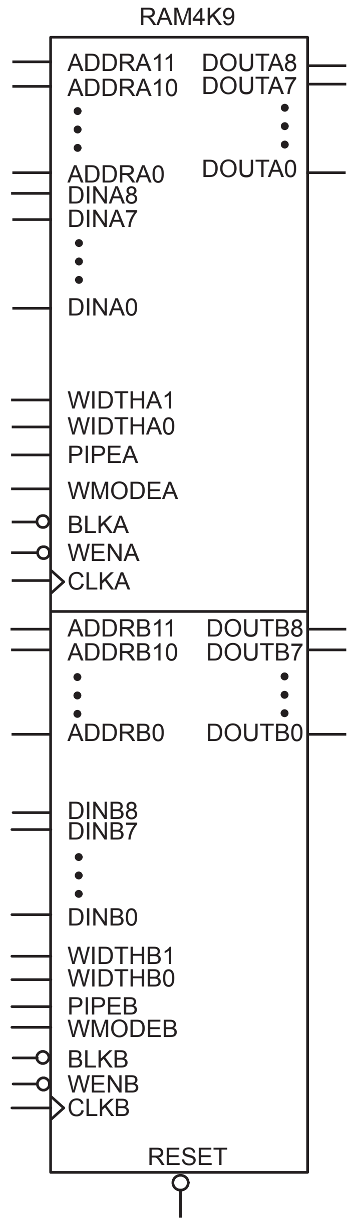


***Figure 2-48* • RAM4K9**

Direct Digital Input

The AV, AC, and AT pads can also be configured as high-voltage digital inputs (Figure 2-68). As these pads are 12 V–tolerant, the digital input can also be up to 12 V. However, the frequency at which these pads can operate is limited to 10 MHz.

To enable one of these analog input pads to operate as a digital input, its corresponding Digital Input Enable (DENA*xy*) pin on the Analog Block must be pulled High, where *x* is either V, C, or T (for AV, AC, or AT pads, respectively) and *y* is in the range 0 to 9, corresponding to the appropriate Analog Quad.

When the pad is configured as a digital input, the signal will come out of the Analog Block macro on the appropriate DA*x*OUT*y* pin, where *x* represents the pad type (V for AV pad, C for AC pad, or T for AT pad) and *y* represents the appropriate Analog Quad number. Example: If the AT pad in Analog Quad 5 is configured as a digital input, it will come out on the DATOUT5 pin of the Analog Block macro.

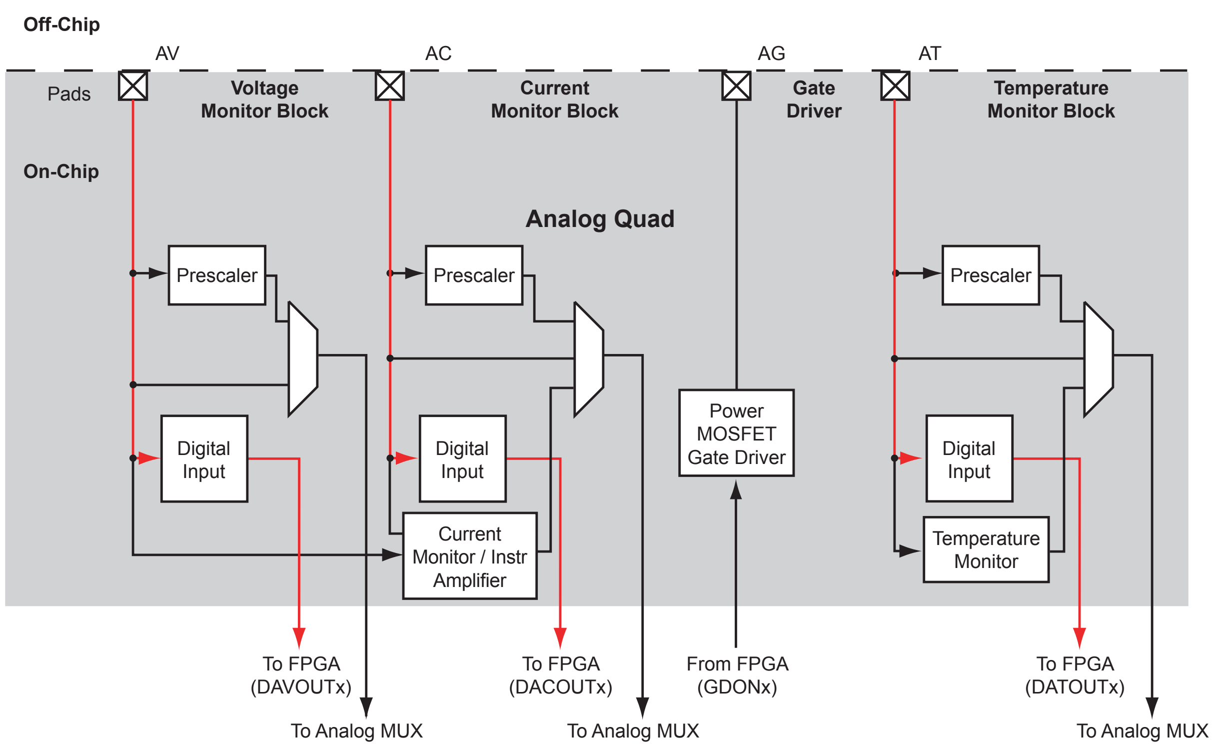


***Figure 2-68* • Analog Quad Direct Digital Input Configuration**

ADC Input Multiplexer

At the input to the Fusion ADC is a 32:1 multiplexer. Of the 32 input channels, up to 30 are user definable. Two of these channels are hardwired internally. Channel 31 connects to an internal temperature diode so the temperature of the Fusion device itself can be monitored. Channel 0 is wired to the FPGA's 1.5 V VCC supply, enabling the Fusion device to monitor its own power supply. Doing this internally makes it unnecessary to use an analog I/O to support these functions. The balance of the MUX inputs are connected to Analog Quads (see the "Analog Quad" section on page 2-80). Table 2-39 defines which Analog Quad inputs are associated with which specific analog MUX channels. The number of Analog Quads present is device-dependent; refer to the family list in the "Fusion Extended Temperature Devices" table on page I of this datasheet for the number of quads per device. Regardless of the number of quads populated in a device, the internal connections to both VCC and the internal temperature diode remain on Channels 0 and 31, respectively. To sample the internal temperature monitor, it must be strobed (similar to the AT pads). The TMSTBINT pin on the Analog Block macro is the control for strobing the internal temperature measurement diode.

To determine which channel is selected for conversion, there is a five-pin interface on the Analog Block, CHNUMBER[4:0], defined in Table 2-38.

Table 2-38 • **Channel Selection**

Channel Number	CHNUMBER[4:0]
0	00000
1	00001
2	00010
3	00011
. . .	. . .
30	11110
31	11111

Table 2-39 shows the correlation between the analog MUX input channels and the analog input pins.

Table 2-39 • **Analog MUX Channels**

Analog MUX Channel	Signal	Analog Quad Number
0	Vcc_analog	
1	AV0	Analog Quad 0
2	AC0	
3	AT0	
4	AV1	Analog Quad 1
5	AC1	
6	AT1	
7	AV2	Analog Quad 2
8	AC2	
9	AT2	
10	AV3	Analog Quad 3
11	AC3	
12	AT3	
13	AV4	Analog Quad 4
14	AC4	
15	AT4	

Table 2-39 • **Analog MUX Channels (continued)**

Analog MUX Channel	Signal	Analog Quad Number
16	AV5	Analog Quad 5
17	AC5	
18	AT5	
19	AV6	Analog Quad 6
20	AC6	
21	AT6	
22	AV7	Analog Quad 7
23	AC7	
24	AT7	
25	AV8	Analog Quad 8
26	AC8	
27	AT8	
28	AV9	Analog Quad 9
29	AC9	
30	AT9	
31	Internal temperature monitor	

The ADC can be powered down independently of the FPGA core, as an additional control or for power-saving considerations, via the PWRDWN pin of the Analog Block. The PWRDWN pin controls only the comparators in the ADC.

ADC Modes

The Fusion ADC can be configured to operate in 8-, 10-, or 12-bit modes, power-down after conversion, and dynamic calibration. This is controlled by MODE[3:0], as defined in Table 2-40.

The output of the ADC is the RESULT[11:0] signal. In 8-bit mode, the Most Significant 8 Bits RESULT[11:4] are used as the ADC value and the Least Significant 4 Bits RESULT[3:0] are logical '0's. In 10-bit mode, RESULT[11:2] are used the ADC value and RESULT[1:0] are logical 0s.

Table 2-40 • **Mode Bits Function**

Name	Bits	Function
MODE	3	0 – Internal calibration after every conversion; two ADCCLK cycles are used after the conversion. 1 – No calibration after every conversion
MODE	2	0 – Power-down after conversion 1 – No Power-down after conversion
MODE	1:0	00 – 10-bit 01 – 12-bit 10 – 8-bit 11 – Unused

Integrated Voltage Reference

The Fusion device has an integrated on-chip 2.56 V reference voltage for the ADC. The value of this reference voltage was chosen to make the prescaling and postscaling factors for the prescaler blocks change in a binary fashion. However, if desired, an external reference voltage of up to 3.3 V can be (conversion that starts before a previously started conversion is finished). The total time for calibration still remains 3,840 ADCCLK cycles.

ADC Configuration Example

This example shows how to choose the correct settings to achieve the fastest sample time in 10-bit mode for a system that runs at 66 MHz. Assume the acquisition times defined in Table 2-43 on page 2-108 for 10-bit mode, which gives 0.549 µs as a minimum hold time.

The period of SYSCLK: t_{SYSCLK} = 1/66 MHz = 0.015 µs

Choosing TVC between 1 and 33 will meet the maximum and minimum period for the ADCCLK requirement. A higher TVC leads to a higher ADCCLK period.

The minimum TVC is chosen so that $t_{distrib}$ and $t_{post\text{-}cal}$ can be run faster. The period of ADCCLK with a TVC of 1 can be computed by EQ 24.

$$t_{ADCCLK} = 4 \times (1 + TVC) \times t_{SYSCLK} = 4 \times (1 + 1) \times 0.015\ \mu s = 0.12\ \mu s$$

EQ 24

The STC value can now be computed by using the minimum sample/hold time from Table 2-43 on page 2-108, as shown in EQ 25.

$$STC = \frac{t_{sample}}{t_{ADCCLK}} - 2 = \frac{0.549\ \mu s}{0.12\ \mu s} - 2 = 4.575 - 2 = 2.575$$

EQ 25

You must round up to 3 to accommodate the minimum sample time requirement. The actual sample time, t_{sample}, with an STC of 3, is now equal to 0.6 µs, as shown in EQ 26

$$t_{sample} = (2 + STC) \times t_{ADCCLK} = (2 + 3) \times t_{ADCCLK} = 5 \times 0.12\ \mu s = 0.6\ \mu s$$

EQ 26

Microsemi recommends post-calibration for temperature drift over time, so post-calibration is enabled.

The post-calibration time, $t_{post\text{-}cal}$, can be computed by EQ 27. The post-calibration time is 0.24 µs.

$$t_{post\text{-}cal} = 2 \times t_{ADCCLK} = 0.24\ \mu s$$

EQ 27

The distribution time, $t_{distrib}$, is equal to 1.2 µs and can be computed as shown in EQ 28 (N is number of bits, referring back to EQ 8 on page 2-94).

$$t_{distrib} = N \times t_{ADCCLK} = 10 \times 0.12 = 1.2\ \mu s$$

EQ 28

The total conversion time can now be summated, as shown in EQ 29 (referring to EQ 23 on page 2-109).

$$t_{sync\_read} + t_{sample} + t_{distrib} + t_{post\text{-}cal} + tsync\_write = (0.015 + 0.60 + 1.2 + 0.24 + 0.015)\ \mu s = 2.07\ \mu s$$

EQ 29

The optimal setting for the system running at 66 MHz with an ADC for 10-bit mode chosen is shown in Table 2-46:

***Table 2-46* • Optimal Setting at 66 MHz in 10-Bit Mode**

TVC[7:0]	= 1	= 0x01
STC[7:0]	= 3	= 0x03
MODE[3:0]	= b'0100	= 0x4*

Note: No power-down after every conversion is chosen in this case; however, if the application is power-sensitive, the MODE[2] can be set to '0', as described above, and it will not affect any performance.

Table 2-71 • **Fusion Advanced I/O Features**

I/O Bank Voltage (typical)	Minibank Voltage (typical)	LVTTL/LVCMOS 3.3 V	LVCMOS 2.5 V	LVCMOS 1.8 V	LVCMOS 1.5 V	3.3 V PCI / PCI-X	GTL + (3.3 V)	GTL + (2.5 V)	GTL (3.3 V)	GTL (2.5 V)	HSTL Class I and II (1.5 V)	SSTL2 Class I and II (2.5 V)	SSTL3 Class I and II (3.3 V)	LVDS (2.5 V ± 5%)	LVPECL (3.3 V)
3.3 V	–	White	Gray	Gray	Gray	White	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray	White
	0.80 V	White	Gray	Gray	Gray	White	Gray	Gray	White	Gray	Gray	Gray	Gray	Gray	White
	1.00 V	White	Gray	Gray	Gray	White	White	Gray	Gray	Gray	Gray	Gray	Gray	Gray	White
	1.50 V	White	Gray	Gray	Gray	White	Gray	Gray	Gray	Gray	Gray	Gray	White	White	White
2.5 V	–	Gray	White	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray
	0.80 V	Gray	White	Gray	Gray	Gray	Gray	Gray	Gray	White	Gray	Gray	Gray	White	Gray
	1.00 V	Gray	White	Gray	Gray	Gray	Gray	White	Gray	Gray	Gray	Gray	Gray	White	Gray
	1.25 V	Gray	White	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray	White	Gray	White	Gray
1.8 V	–	Gray	Gray	White	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray
1.5 V	–	Gray	Gray	Gray	White	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray	Gray
	0.75 V	Gray	Gray	Gray	White	Gray	Gray	Gray	Gray	Gray	White	Gray	Gray	Gray	Gray

Note: *White box: Allowable I/O standard combinations*
Gray box: Illegal I/O standard combinations

Double Data Rate (DDR) Support

Fusion Pro I/Os support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making it very efficient for implementing very high-speed systems.

DDR interfaces can be implemented using HSTL, SSTL, LVDS, and LVPECL I/O standards. In addition, high-speed DDR interfaces can be implemented using LVDS I/O.

Input Support for DDR

The basic structure to support a DDR input is shown in Figure 2-100. Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock.

Each I/O tile on Fusion devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in Figure 2-101 on page 2-141. New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

Refer to the application note *Using DDR for Fusion Devices* for more information.

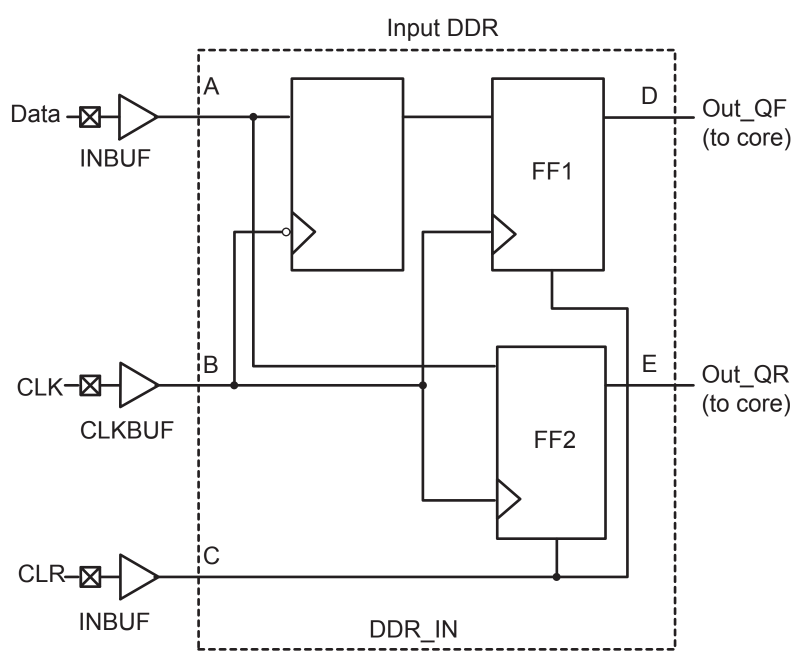


Figure 2-100 **• DDR Input Register Support in Fusion Devices**

Table 2-82 • **Advanced I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	Refer to the following tables for more information: Table 2-79 on page 2-153 Table 2-80 on page 2-153	Refer to the following tables for more information: Table 2-79 on page 2-153 Table 2-80 on page 2-153	Off	None	35 pF	–
LVCMOS 2.5 V			Off	None	35 pF	–
LVCMOS 2.5/5.0 V			Off	None	35 pF	–
LVCMOS 1.8 V			Off	None	35 pF	–
LVCMOS 1.5 V			Off	None	35 pF	–
PCI (3.3 V)			Off	None	10 pF	–
PCI-X (3.3 V)			Off	None	10 pF	–
LVDS, B-LVDS, M-LVDS			Off	None	–	–
LVPECL			Off	None	–	–

Table 2-120 **• 1.5 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	8.82	0.05	1.52	2.26	0.44	7.20	8.82	3.57	2.92	9.55	11.18	ns
	–1	0.58	7.50	0.04	1.29	1.92	0.38	6.12	7.50	3.04	2.48	8.13	9.51	ns
	–2	0.51	6.59	0.03	1.13	1.69	0.33	5.37	6.59	2.67	2.18	7.13	8.35	ns
4 mA	Std.	0.68	5.60	0.05	1.52	2.26	0.44	5.11	5.60	3.94	3.59	7.47	7.96	ns
	–1	0.58	4.77	0.04	1.29	1.92	0.38	4.35	4.77	3.36	3.05	6.36	6.77	ns
	–2	0.51	4.18	0.03	1.13	1.69	0.33	3.82	4.18	2.95	2.68	5.58	5.95	ns
6 mA	Std.	0.68	5.07	0.05	1.52	2.26	0.44	4.80	4.92	4.03	3.76	7.15	7.28	ns
	–1	0.58	4.31	0.04	1.29	1.92	0.38	4.08	4.19	3.43	3.20	6.09	6.19	ns
	–2	0.51	3.78	0.03	1.13	1.69	0.33	3.58	3.68	3.01	2.81	5.34	5.44	ns
8 mA	Std.	0.68	4.66	0.05	1.52	2.26	0.44	4.38	3.77	4.16	4.43	6.74	6.13	ns
	–1	0.58	3.96	0.04	1.29	1.92	0.38	3.73	3.21	3.54	3.77	5.73	5.21	ns
	–2	0.51	3.48	0.03	1.13	1.69	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns
12 mA	Std.	0.68	4.30	0.05	1.52	2.26	0.44	4.38	3.77	4.16	4.43	6.74	6.13	ns
	–1	0.58	3.66	0.04	1.29	1.92	0.38	3.73	3.21	3.54	3.77	5.73	5.21	ns
	–2	0.51	3.21	0.03	1.13	1.69	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Output Register

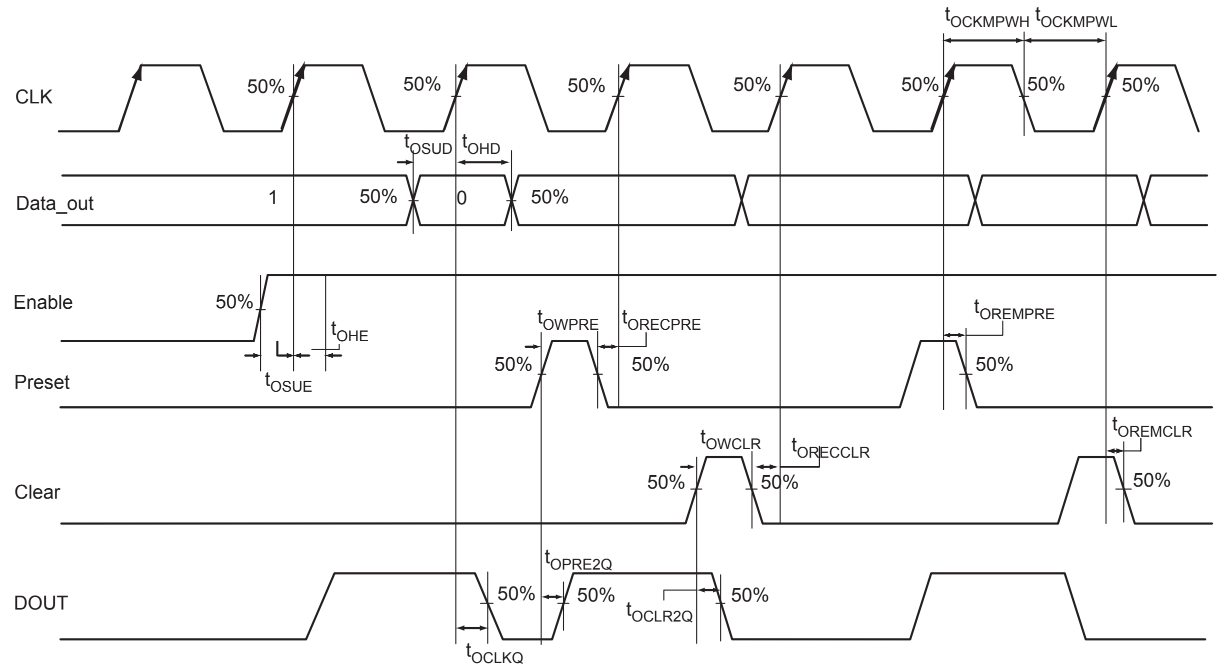


Figure 2-138 **• Output Register Timing Diagram**

Timing Characteristics

Table 2-168 **• Output Data Register Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.61	0.69	0.81	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	0.37	0.43	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.45	0.51	0.60	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.83	0.94	1.11	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.83	0.94	1.11	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	0.26	0.31	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	0.26	0.31	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Output Enable Register

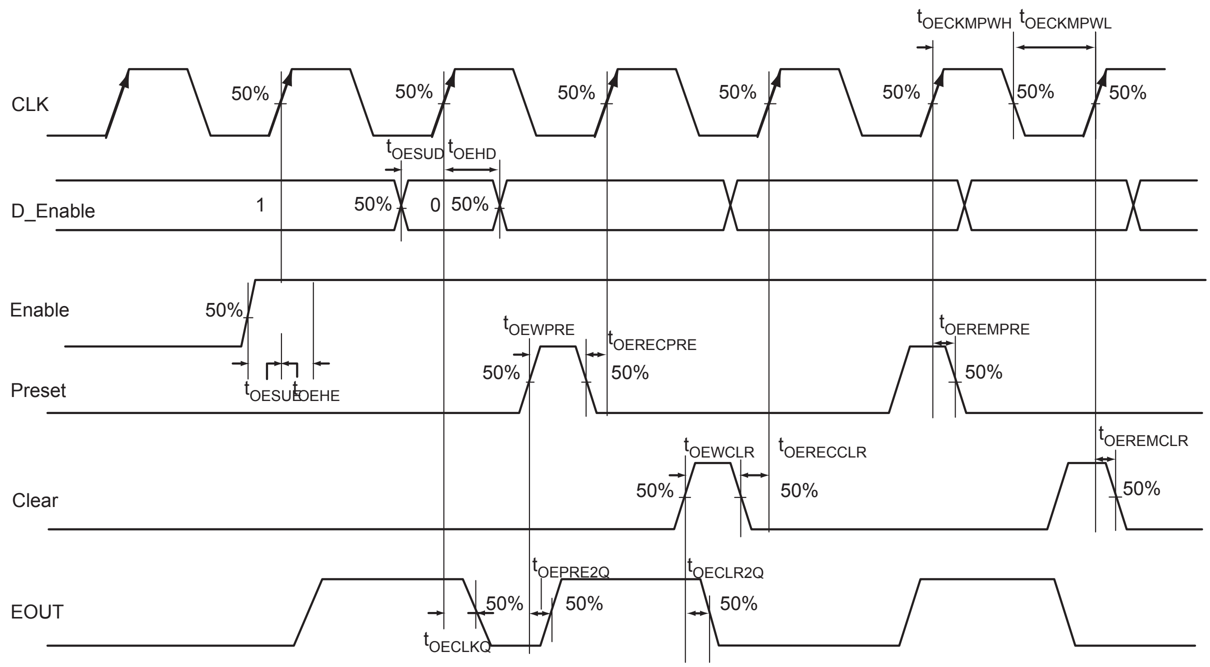


***Figure 2-139* • Output Enable Register Timing Diagram**

Timing Characteristics

***Table 2-169* • Output Enable Register Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.46	0.52	0.61	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.32	0.37	0.43	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.45	0.51	0.60	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.69	0.78	0.92	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.69	0.78	0.92	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.23	0.26	0.31	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.23	0.26	0.31	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Output DDR

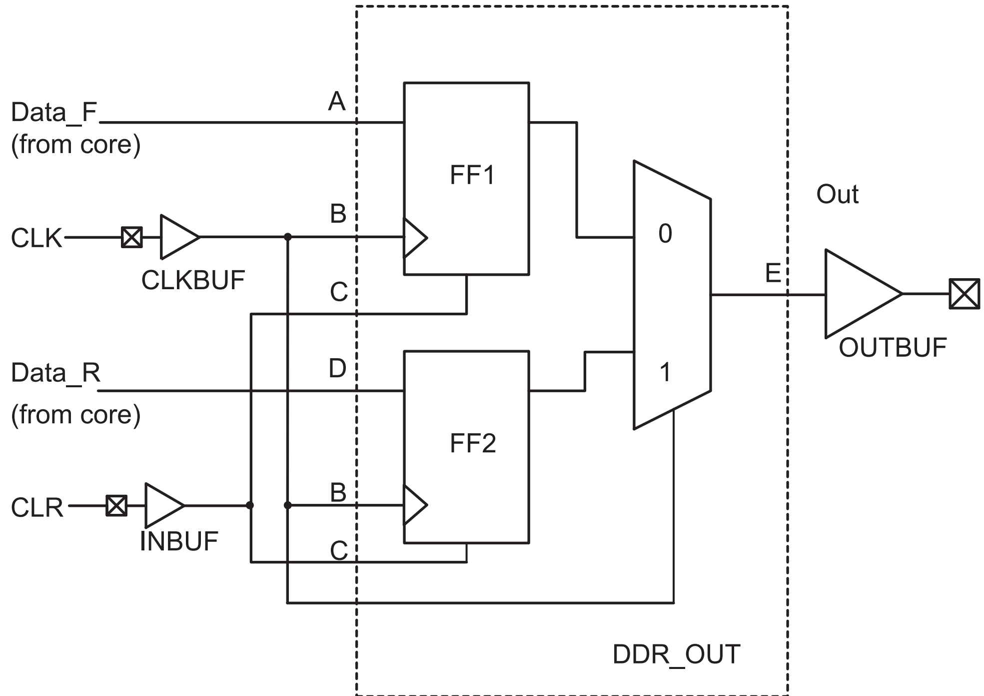


***Figure 2-142* • Output DDR Timing Model**

***Table 2-172* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Datasheet Categories

Categories

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