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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 276480 |
| Number of I/O | 119 |
| Number of Gates | 1500000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -55°C ~ 100°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/afs1500-fgg256k |

# Clocking Resources

The Fusion family has a robust collection of clocking peripherals, as shown in the block diagram in Figure 2-16. These on-chip resources enable the creation, manipulation, and distribution of many clock signals. The Fusion integrated RC oscillator produces a 100 MHz clock source with no external components. For systems requiring more precise clock signals, the Fusion family supports an on-chip crystal oscillator circuit. The integrated PLLs in each Fusion device can use the RC oscillator, crystal oscillator, or another on-chip clock signal as a source. These PLLs offer a variety of capabilities to modify the clock source (multiply, divide, synchronize, advance, or delay). Utilizing the CCC found in the popular ProASIC3 family, Fusion incorporates six CCC blocks. The CCCs allow access to Fusion global and local clock distribution nets, as described in the "Global Resources (VersaNets)" section on page 2-11.

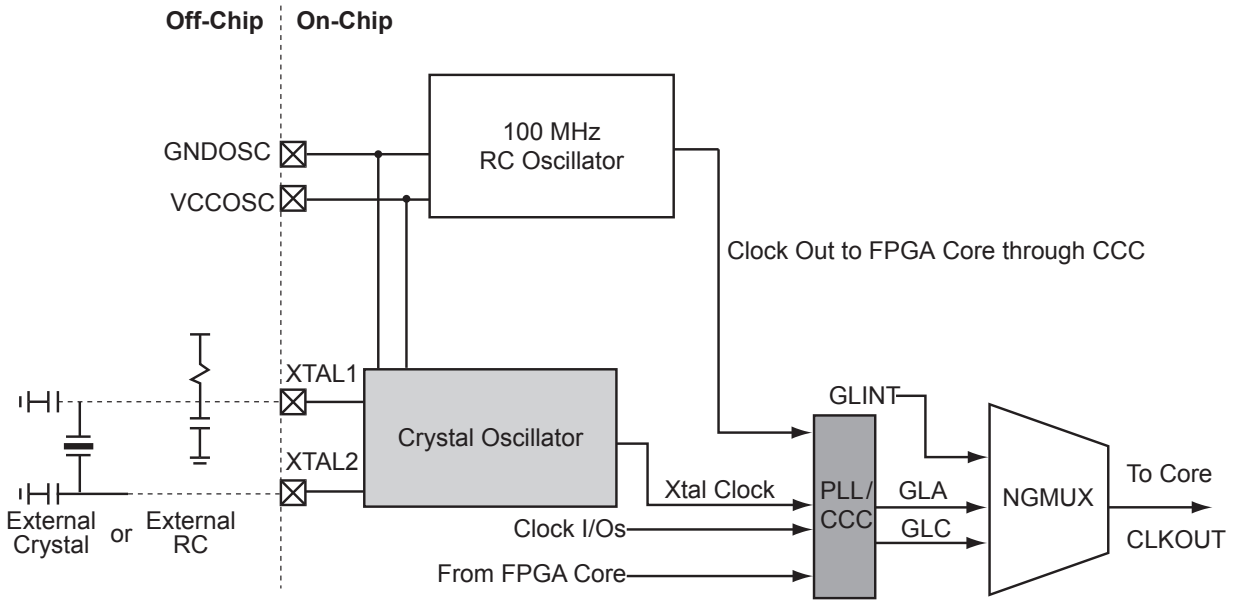
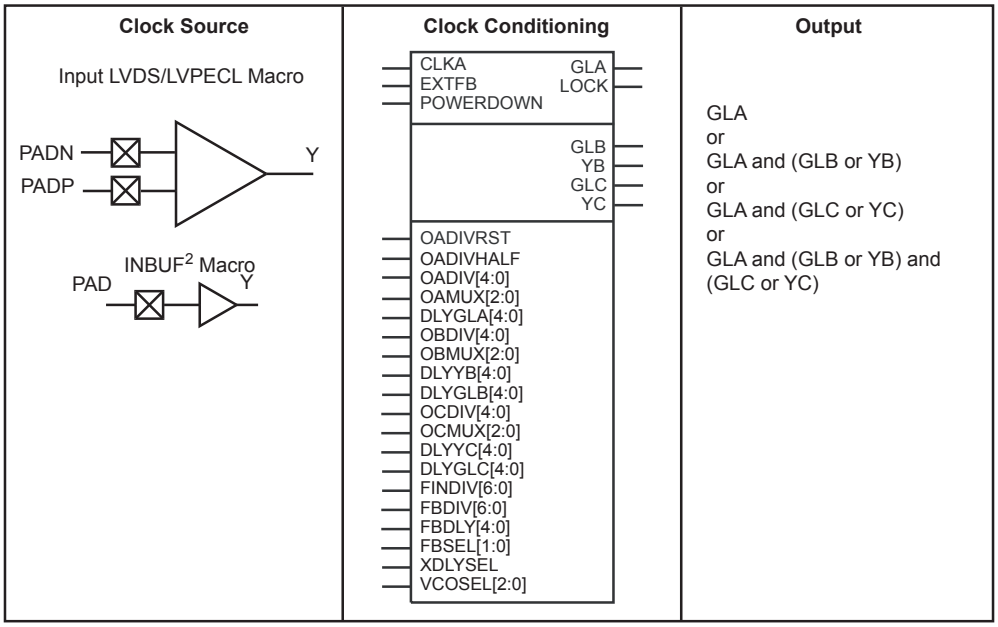



***Figure 2-16 •*** **Fusion Clocking Options**




*Notes:*

1. *Visit the Microsemi SoC Products Group website for future application notes concerning dynamic PLL reconfiguration. Refer to the "PLL Macro" section on page 2-27 for signal descriptions.*
2. *Many specific INBUF macros support the wide variety of single-ended and differential I/O standards for the Fusion family.*
3. *Refer to the IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide for more information.*

***Figure 2-19 •*** **Fusion CCC Options: Global Buffers with the PLL Macro**

***Table 2-10 •*** **Available Selections of I/O Standards within CLKBUF and CLKBUF_LVDS/LVPECL Macros**

| CLKBUF Macros |
|---|
| CLKBUF_LVCMOS5 |
| CLKBUF_LVCMOS33[1] |
| CLKBUF_LVCMOS18 |
| CLKBUF_LVCMOS15 |
| CLKBUF_PCI |
| CLKBUF_LVDS[2] |
| CLKBUF_LVPECL |

*Notes:*

1. *This is the default macro. For more details, refer to the IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide.*
2. *The B-LVDS and M-LVDS standards are supported with CLKBUF_LVDS.*

## Global Buffers with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay (Figure 2-21). The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

The CLKDLY macro can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the Fusion family. The available INBUF macros are described in the *IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide.*

The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Libero SoC and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.

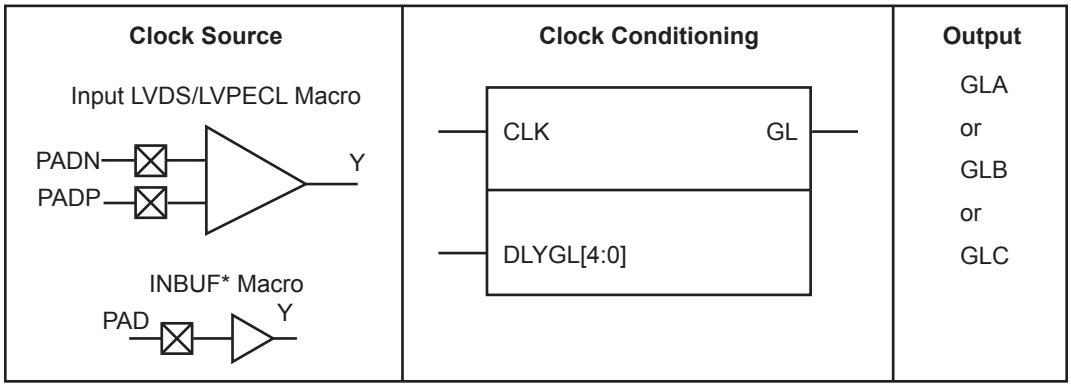



***Figure 2-21 •*** **Fusion CCC Options: Global Buffers with Programmable Delay**

### Example: Calculation for Match Count

To put the Fusion device on standby for one hour using an external crystal of 32.768 KHz:

The period of the crystal oscillator is $T_{crystal}$:

$T_{crystal}$ = 1 / 32.768 KHz = 30.518 µs

The period of the counter is $T_{counter}$:

$T_{counter}$ = 30.518 us X 128 = 3.90625 ms

The Match Count for 1 hour is ∆tmatch:

∆tmatch / $T_{counter}$ = (1 hr X 60 min/hr X 60 sec/min) / 3.90625 ms = 921600 or 0xE1000

Using a 32.768 KHz crystal, the maximum standby time of the 40-bit counter is 4,294,967,296 seconds, which is 136 years.

***Table 2-14 •*** **Memory Map for RTC in ACM Register and Description**

| ACMADDR | Register Name | Description | Use | Default Value |
|---|---|---|---|---|
| 0x40 | COUNTER0 | Counter bits 7:0 | Used to preload the counter to a specified start point. | 0x00 |
| 0x41 | COUNTER1 | Counter bits 15:8 | | 0x00 |
| 0x42 | COUNTER2 | Counter bits 23:16 | | 0x00 |
| 0x43 | COUNTER3 | Counter bits 31:24 | | 0x00 |
| 0x44 | COUNTER4 | Counter bits 39:32 | | 0x00 |
| 0x48 | MATCHREG0 | Match register bits 7:0 | The RTC comparison bits | 0x00 |
| 0x49 | MATCHREG1 | Match register bits 15:8 | | 0x00 |
| 0x4A | MATCHREG2 | Match register bits 23:16 | | 0x00 |
| 0x4B | MATCHREG3 | Match register bits 31:24 | | 0x00 |
| 0x4C | MATCHREG4 | Match register bits 39:32 | | 0x00 |
| 0x50 | MATCHBIT0 | Individual match bits 7:0 | The output of the XNOR gates<br>0 – Not matched<br>1 – Matched | 0x00 |
| 0x51 | MATCHBIT1 | Individual match bits 15:8 | | 0x00 |
| 0x52 | MATCHBIT2 | Individual match bits 23:16 | | 0x00 |
| 0x53 | MATCHBIT3 | Individual match bits 31:24 | | 0x00 |
| 0x54 | MATCHBIT4 | Individual match bits 29:32 | | 0x00 |
| 0x58 | CTRL_STAT | Control (write/read) / Status (read only) register bits | Refer to Table 2-15 on page 2-35 for details. | 0x00 |

The following error indications are possible for Read operations:

1. STATUS = '01' when a single-bit data error was detected and corrected within the block addressed.
2. STATUS = '10' when a double-bit error was detected in the block addressed (note that the error is uncorrected).

In addition to data reads, users can read the status of any page in the FB by asserting PAGESTATUS along with REN. The format of the data returned by a page status read is shown in Table 2-22, and the definition of the page status bits is shown in Table 2-23.

***Table 2-22 •*** **Page Status Read Data Format**

| 31 | 8 | 7 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Write Count | | Reserved | | Over Threshold | Read Protected | Write Protected | Overwrite Protected |

***Table 2-23 •*** **Page Status Bit Definition**

| Page Status Bit(s) | Definition |
|---|---|
| 31–8 | The number of times the page addressed has been programmed/erased |
| 7–4 | Reserved; read as 0 |
| 3 | Over Threshold indicator (see the "Program Operation" section on page 2-46) |
| 2 | Read Protected; read protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value. |
| 1 | Write Protected; write protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value. |
| 0 | Overwrite Protected; designates that the user has set the OVERWRITEPROTECT bit on the interface while doing a Program operation. The page cannot be written without first performing an Unprotect Page operation. |

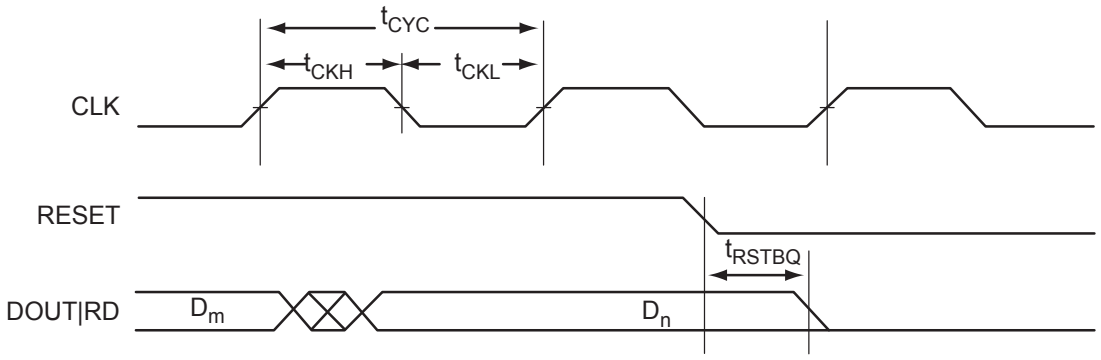



***Figure 2-54* • RAM Reset. Applicable to Both RAM4K9 and RAM512x18**.

### FIFO Flag Usage Considerations

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values, respectively. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag to assert when the write address exceeds the read address by at least a predefined value. In a 2k×8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

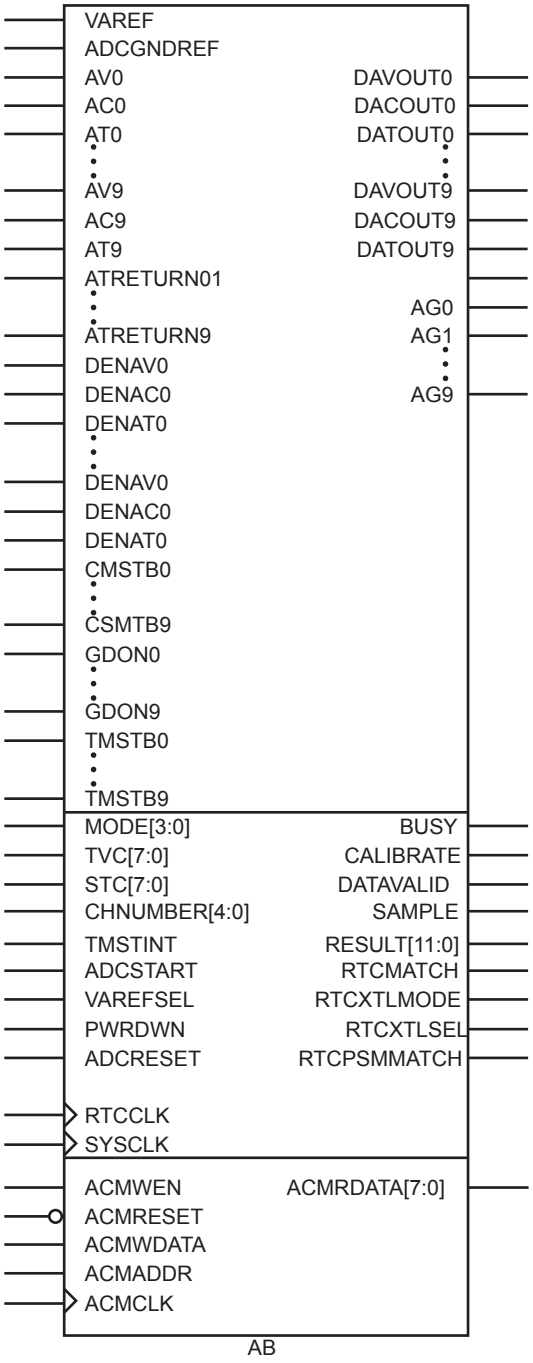
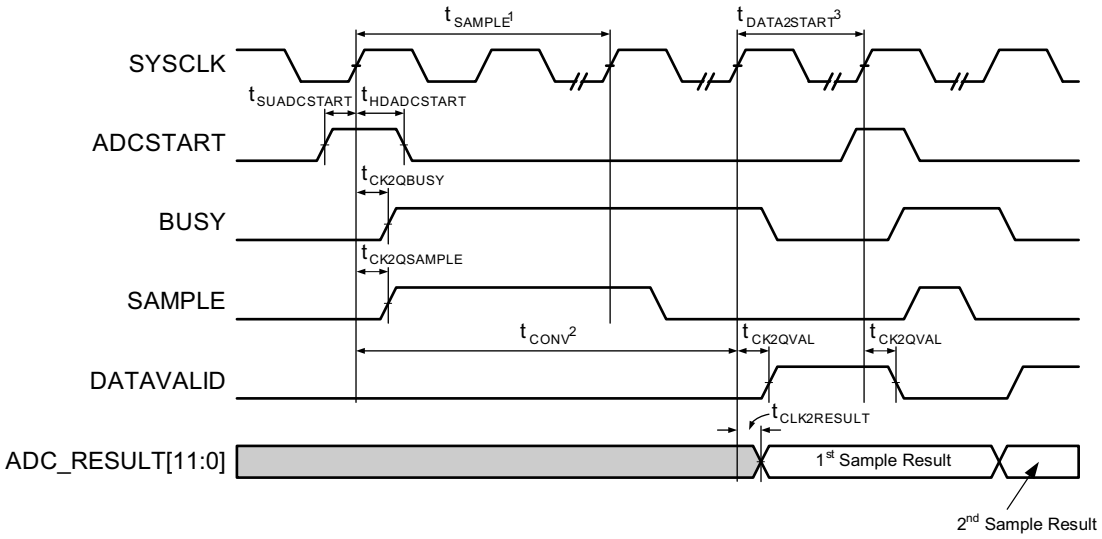



***Figure 2-63 •*** **Analog Block Macro**

### Standard Conversion

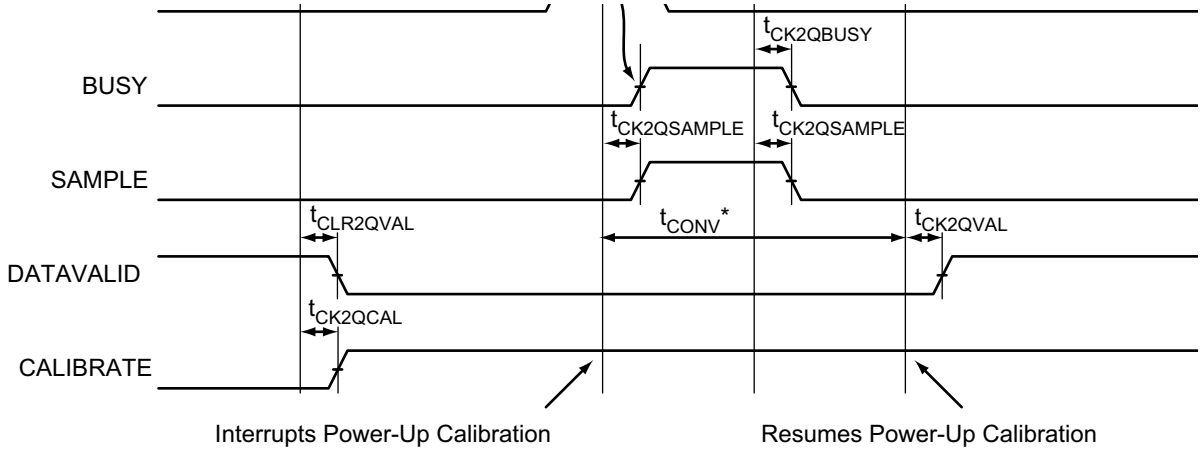



*Notes:*

1. *Refer to EQ 20 on page 2-108 for the calculation on the sample time, $t_{SAMPLE}$.*
2. *See EQ 23 on page 2-109 for calculation on the conversion time, $t_{CONV}$.*
3. *Minimum time to issue an ADCSTART after DATAVALID is 1 SYSCLK period*

***Figure 2-90 •*** **Standard Conversion Status Signal Timing Diagram**

### Intra-Conversion




*Note: *$t_{CONV}$ represents the conversion time of the second conversion. See EQ 23 on page 2-109 for calculation of the conversion time, $t_{CONV}$.*

***Figure 2-91 •*** **Intra-Conversion Timing Diagram**

***Table 2-71 •*** **Fusion Advanced I/O Features**

| I/O Bank Voltage (typical) | Minibank Voltage (typical) | LVTTL/LVCMOS 3.3 V | LVCMOS 2.5 V | LVCMOS 1.8 V | LVCMOS 1.5 V | 3.3 V PCI / PCI-X | GTL + (3.3 V) | GTL + (2.5 V) | GTL (3.3 V) | GTL (2.5 V) | HSTL Class I and II (1.5 V) | SSTL2 Class I and II (2.5 V) | SSTL3 Class I and II (3.3 V) | LVDS (2.5 V ± 5%) | LVPECL (3.3 V) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V | – | | | | | | | | | | | | | | |
| | 0.80 V | | | | | | | | | | | | | | |
| | 1.00 V | | | | | | | | | | | | | | |
| | 1.50 V | | | | | | | | | | | | | | |
| 2.5 V | – | | | | | | | | | | | | | | |
| | 0.80 V | | | | | | | | | | | | | | |
| | 1.00 V | | | | | | | | | | | | | | |
| | 1.25 V | | | | | | | | | | | | | | |
| 1.8 V | – | | | | | | | | | | | | | | |
| 1.5 V | – | | | | | | | | | | | | | | |
| | 0.75 V | | | | | | | | | | | | | | |

*Note: White box: Allowable I/O standard combinations*
*Gray box: Illegal I/O standard combinations*

Temporary overshoots are allowed according to Table 3-4 on page 3-5.

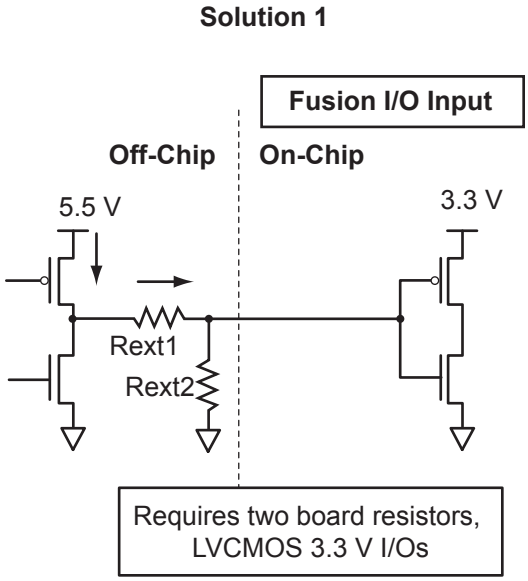



***Figure 2-102 •*** **Solution 1**

## *Solution 2*

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-5. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and Zener, as shown in Figure 2-103. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

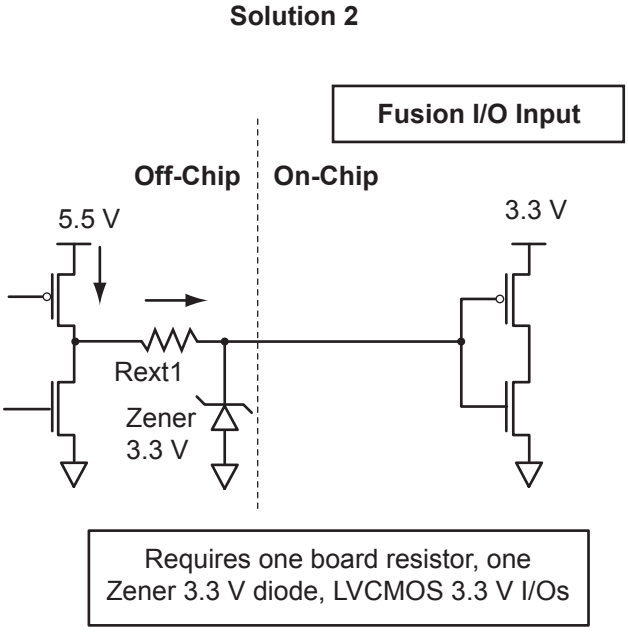



***Figure 2-103 •*** **Solution 2**

***Table 2-81 •*** **Fusion Pro I/O Default Attributes**

| I/O Standards | SLEW (output only) | OUT_DRIVE (output only) | SKEW (tribuf and bibuf only) | RES_PULL | OUT_LOAD (output only) | COMBINE_REGISTER | IN_DELAY (input only) | IN_DELAY_VAL (input only) | SCHMITT_TRIGGER (input only) |
|---|---|---|---|---|---|---|---|---|---|
| LVTTL/LVCMOS 3.3 V | Refer to the following tables for more information:<br>Table 2-79 on page 2-153<br>Table 2-80 on page 2-153 | Refer to the following tables for more information:<br>Table 2-79 on page 2-153<br>Table 2-80 on page 2-153 | Off | None | 35 pF | – | Off | 0 | Off |
| LVCMOS 2.5 V | | | Off | None | 35 pF | – | Off | 0 | Off |
| LVCMOS 2.5/5.0 V | | | Off | None | 35 pF | – | Off | 0 | Off |
| LVCMOS 1.8 V | | | Off | None | 35 pF | – | Off | 0 | Off |
| LVCMOS 1.5 V | | | Off | None | 35 pF | – | Off | 0 | Off |
| PCI (3.3 V) | | | Off | None | 10 pF | – | Off | 0 | Off |
| PCI-X (3.3 V) | | | Off | None | 10 pF | – | Off | 0 | Off |
| GTL+ (3.3 V) | | | Off | None | 10 pF | – | Off | 0 | Off |
| GTL+ (2.5 V) | | | Off | None | 10 pF | – | Off | 0 | Off |
| GTL (3.3 V) | | | Off | None | 10 pF | – | Off | 0 | Off |
| GTL (2.5 V) | | | Off | None | 10 pF | – | Off | 0 | Off |
| HSTL Class I | | | Off | None | 20 pF | – | Off | 0 | Off |
| HSTL Class II | | | Off | None | 20 pF | – | Off | 0 | Off |
| SSTL2 Class I and II | | | Off | None | 30 pF | – | Off | 0 | Off |
| SSTL3 Class I and II | | | Off | None | 30 pF | – | Off | 0 | Off |
| LVDS, B-LVDS, M-LVDS | | | Off | None | 0 pF | – | Off | 0 | Off |
| LVPECL | | | Off | None | 0 pF | – | Off | 0 | Off |

***Table 2-96 •*** **I/O Short Currents IOSH/IOSL**

| | Drive Strength | IOSH (mA)* | IOSL (mA)* |
|---|---|---|---|
| **Applicable to Pro I/O Banks** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 4 mA | 25 | 27 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |
| 2.5 V LVCMOS | 4 mA | 16 | 18 |
| | 8 mA | 32 | 37 |
| | 12 mA | 65 | 74 |
| | 16 mA | 83 | 87 |
| | 24 mA | 169 | 124 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| | 6 mA | 35 | 44 |
| | 8 mA | 45 | 51 |
| | 12 mA | 91 | 74 |
| | 16 mA | 91 | 74 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| | 4 mA | 25 | 33 |
| | 6 mA | 32 | 39 |
| | 8 mA | 66 | 55 |
| | 12 mA | 66 | 55 |
| **Applicable to Advanced I/O Banks** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |
| 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |

*Note:* *$T_J$ = 100°C

**Table 2-103 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew, Extended Temperature Case Conditions: $T_J$ =100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.68 | 8.31 | 0.05 | 1.27 | 1.65 | 0.44 | 8.47 | 7.07 | 2.84 | 2.73 | 10.82 | 9.43 | ns |
| | –1 | 0.58 | 7.07 | 0.04 | 1.08 | 1.40 | 0.38 | 7.20 | 6.01 | 2.41 | 2.32 | 9.21 | 8.02 | ns |
| | –2 | 0.51 | 6.21 | 0.03 | 0.95 | 1.23 | 0.33 | 6.32 | 5.28 | 2.12 | 2.04 | 8.08 | 7.04 | s |
| 8 mA | Std. | 0.68 | 5.35 | 0.05 | 1.27 | 1.65 | 0.44 | 5.45 | 4.37 | 3.21 | 3.39 | 7.81 | 6.73 | ns |
| | –1 | 0.58 | 4.55 | 0.04 | 1.08 | 1.40 | 0.38 | 4.64 | 3.72 | 2.73 | 2.88 | 6.64 | 5.72 | ns |
| | –2 | 0.51 | 4.00 | 0.03 | 0.95 | 1.23 | 0.33 | 4.07 | 3.26 | 2.40 | 2.53 | 5.83 | 5.02 | ns |
| 12 mA | Std. | 0.68 | 3.87 | 0.05 | 1.27 | 1.65 | 0.44 | 3.94 | 3.03 | 3.45 | 3.81 | 6.30 | 5.38 | ns |
| | –1 | 0.58 | 3.29 | 0.04 | 1.08 | 1.40 | 0.38 | 3.35 | 2.57 | 2.94 | 3.24 | 5.36 | 4.58 | ns |
| | –2 | 0.51 | 2.89 | 0.03 | 0.95 | 1.23 | 0.33 | 2.94 | 2.26 | 2.58 | 2.85 | 4.70 | 4.02 | ns |
| 16 mA | Std. | 0.68 | 3.65 | 0.05 | 1.27 | 1.65 | 0.44 | 3.72 | 2.75 | 3.51 | 3.93 | 6.08 | 5.11 | ns |
| | –1 | 0.58 | 3.11 | 0.04 | 1.08 | 1.40 | 0.38 | 3.16 | 2.34 | 2.99 | 3.34 | 5.17 | 4.34 | ns |
| | –2 | 0.51 | 2.73 | 0.03 | 0.95 | 1.23 | 0.33 | 2.78 | 2.05 | 2.62 | 2.93 | 4.54 | 3.81 | ns |
| 24 mA | Std. | 0.68 | 3.38 | 0.05 | 1.27 | 1.65 | 0.44 | 3.44 | 2.27 | 3.57 | 4.35 | 5.80 | 4.63 | ns |
| | –1 | 0.58 | 2.88 | 0.04 | 1.08 | 1.40 | 0.38 | 2.93 | 1.93 | 3.04 | 3.70 | 4.94 | 3.94 | ns |
| | –2 | 0.51 | 2.53 | 0.03 | 0.95 | 1.23 | 0.33 | 2.57 | 1.70 | 2.67 | 3.25 | 4.33 | 3.46 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.*

### Output Register

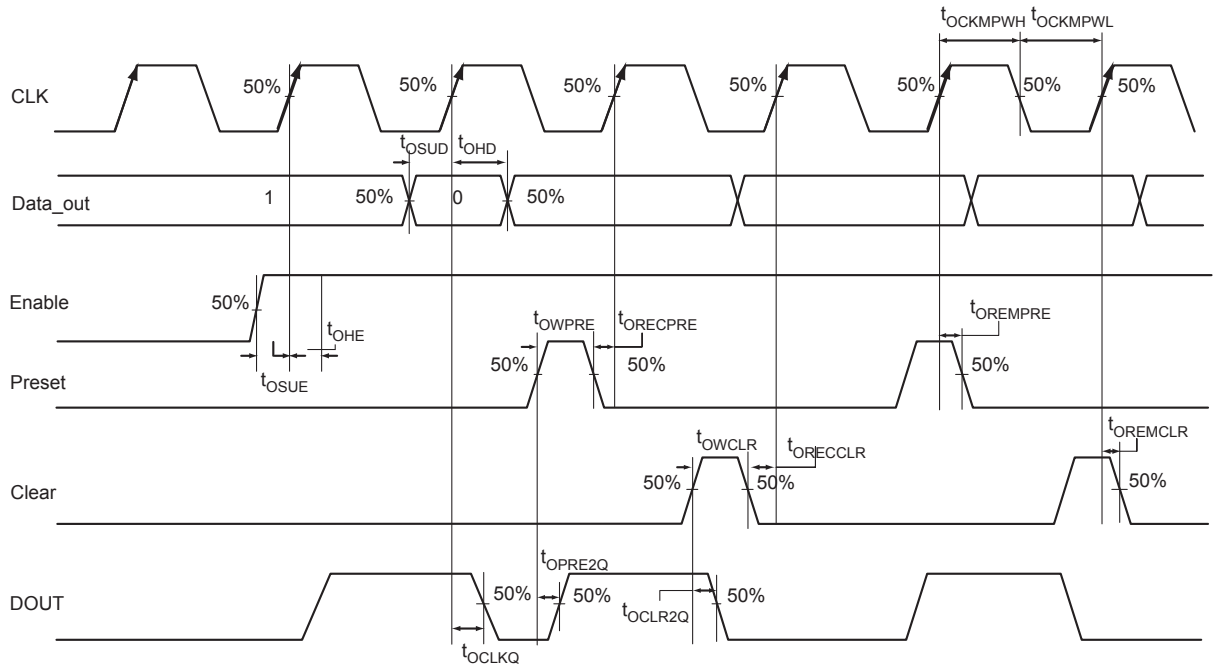



***Figure 2-138 •*** **Output Register Timing Diagram**

### Timing Characteristics

***Table 2-168 •*** **Output Data Register Propagation Delays**
**Extended Temperature Case Conditions: $T_J$ = 100°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | 0.61 | 0.69 | 0.81 | ns |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | 0.32 | 0.37 | 0.43 | ns |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | 0.45 | 0.51 | 0.60 | ns |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | 0.83 | 0.94 | 1.11 | ns |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | 0.83 | 0.94 | 1.11 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.23 | 0.26 | 0.31 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.23 | 0.26 | 0.31 | ns |
| $t_{OWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width High for the Output Data Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width Low for the Output Data Register | 0.32 | 0.37 | 0.43 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.*

because SAMPLE is defined in the IEEE1532 specification as a noninvasive instruction. If the input buffers were to be enabled by SAMPLE temporarily turning on the I/Os, then it would not truly be a noninvasive instruction. Refer to the standard or the "In-System Programming (ISP) of Microsemi's Low Power Flash Devices Using FlashPro4/3/3X" chapter of the *Fusion FPGA Fabric User's Guide* for more details.

### Boundary Scan

Fusion devices are compatible with IEEE Standard 1149.1, which defines a hardware architecture and the set of mechanisms for boundary scan testing. The basic Fusion boundary scan logic circuit is composed of the test access port (TAP) controller, test data registers, and instruction register (Figure 2-144 on page 2-229). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) and the optional IDCODE instruction (Table 2-176 on page 2-229).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI, TDO (test data input and output), TMS (test mode selector), and TRST (test reset input). TMS, TDI, and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary scan test usage. Refer to the "JTAG Pins" section on page 2-225 for pull-up/-down recommendations for TDO and TCK pins. The TAP controller is a 4-bit state machine (16 states) that operates as shown in Figure 2-144 on page 2-229. The 1s and 0s represent the values that must be present on TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

***Table 2-175* • TRST and TCK Pull-Down Recommendations**

| VJTAG | Tie-Off Resistance* |
|---|---|
| VJTAG at 3.3 V | 200 Ω to 1 kΩ |
| VJTAG at 2.5 V | 200 Ω to 1 kΩ |
| VJTAG at 1.8 V | 500 Ω to 1 kΩ |
| VJTAG at 1.5 V | 500 Ω to 1 kΩ |

*Note: *Equivalent parallel resistance if more than one device is on JTAG chain.*

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain High for five TCK cycles. The TRST pin can also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

Fusion devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (LSB, ID number, part number, and version). The boundary scan register observes and controls the state of each I/O pin. Each I/O cell has three boundary scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin.

The serial pins are used to serially connect all the boundary scan register cells in a device into a boundary scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

# Thermal Characteristics

## Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P}$$

*EQ 1*

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

*EQ 2*

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

*EQ 3*

where

$\theta_{JA}$ = Junction-to-air thermal resistance
$\theta_{JB}$ = Junction-to-board thermal resistance
$\theta_{JC}$ = Junction-to-case thermal resistance
$T_J$ = Junction temperature
$T_A$ = Ambient temperature
$T_B$ = Board temperature (measured 1.0 mm away from the package edge)
$T_C$ = Case temperature
P = Total power dissipated by the device

***Table 3-6 •*** **Package Thermal Resistance**

| Product | $\theta_{JA}$ | | | $\theta_{JC}$ | $\theta_{JB}$ | Units |
|---|---|---|---|---|---|---|
| | Still Air | 1.0 m/s | 2.5 m/s | | | |
| AFS600-FG256 | 28.9 | 25.2 | 23.5 | 6.8 | 19.9 | °C/W |
| AFS1500-FG256 | 23.3 | 19.6 | 18.0 | 4.3 | 14.2 | °C/W |
| AFS600-FG484 | 21.8 | 18.2 | 16.7 | 7.7 | 16.8 | °C/W |
| AFS1500-FG484 | 21.6 | 16.8 | 15.2 | 5.6 | 14.9 | °C/W |
| AFS1500-FG676 | TBD | TBD | TBD | TBD | TBD | °C/W |

## Methodology

### Total Power Consumption—$P_{TOTAL}$

#### Operating Mode, Standby Mode, and Sleep Mode

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{STAT}$ is the total static power consumption.

$P_{DYN}$ is the total dynamic power consumption.

### Total Static Power Consumption—$P_{STAT}$

#### Operating Mode

$P_{STAT} = PDC1 + (N_{NVM\text{-}BLOCKS} * PDC4) + PDC5+ (N_{QUADS} * P_{DC6}) + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8}) + (N_{PLLS} * PDC9)$

$N_{NVM\text{-}BLOCKS}$ is the number of NVM blocks available in the device.

$N_{QUADS}$ is the number of Analog Quads used in the design.

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$N_{PLLS}$ is the number of PLLs available in the device.

#### Standby Mode

$P_{STAT} = PDC2$

#### Sleep Mode

$P_{STAT} = PDC3$

### Total Dynamic Power Consumption—$P_{DYN}$

#### Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB}$

#### Standby Mode

$P_{DYN} = P_{XTL\text{-}OSC}$

#### Sleep Mode

$P_{DYN} = 0$ W

### Global Clock Dynamic Contribution—$P_{CLOCK}$

#### Operating Mode

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

$F_{CLK}$ is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

#### Standby Mode and Sleep Mode

$P_{CLOCK} = 0$ W

| Revision | Changes | Page |
|---|---|---|
| Revision 1 (continued) | The following information was added before Figure 2-17 • XTLOSC Macro:<br>In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating (SAR 34900). | 2-19 |
| | Table 2-11 • Fusion CCC/PLL Specification was updated. A note was added indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34815). | 2-28 |
| | A note was added to Figure 2-27 • Real-Time Counter System (not all the signals are shown for the AB macro) stating that the user is only required to instantiate the VRPSM macro if the user wishes to specify PUPO behavior of the voltage regulator to be different from the default, or employ user logic to shut the voltage regulator off (SAR 34897). | 2-31 |
| | VPUMP was incorrectly represented as VPP in several places. This was corrected to VPUMP in the "Standby and Sleep Mode Circuit Implementation" section, Table 3-8 • AFS1500 Quiescent Supply Current Characteristics, and Table 3-9 • AFS600 Quiescent Supply Current Characteristics (SAR 34922). | 2-32, 3-11, 3-13 |
| | Additional information was added to the Flash Memory Block "Write Operation" section, including an explanation of the fact that a copy-page operation takes no less than 55 cycles (SAR 34924). | 2-45 |
| | The "FlashROM" section was revised to refer to Figure 2-46 • FlashROM Timing Diagram and Table 2-25 • FlashROM Access Time, Extended Temperature Conditions: TJ = 100°C, Worst-Case VCC = 1.425 V rather than stating 20 MHz as the maximum FlashROM access clock and 10 ns as the time interval for D0 to become valid or invalid (SAR 34923). | 2-54 |
| | Figure 2-54 • One Port Write / Other Port Read Same was deleted. Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34864).<br>The port names in the "SRAM Characteristics" section, Figure 2-58 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SARs 35745, 38235). | 2-63, 2-73, 2-75 |
| | Figure 2-56 • FIFO Read and Figure 2-57 • FIFO Write were added (SAR 34839). | 2-72 |
| | In several places throughout the datasheet, GNDREF was corrected to ADCGNDREF (SAR 38698):<br>Figure 2-63 • Analog Block Macro<br>Table 2-35 • Analog Block Pin Description<br>"ADC Operation" section | 2-77, 2-78, 2-104 |
| | The following note was added below Figure 2-77 • Timing Diagram for the Temperature Monitor Strobe Signal:<br>When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a 1 µA sink into the Fusion device (SAR 34901). | 2-93 |
| | Table 2-49 • Analog Channel Specifications was modified to include calibrated and uncalibrated values for offset (AFS090 and AFS250) for the external and internal temperature monitors. The "Offset" section was revised accordingly and now references Table 2-49 • Analog Channel Specifications (SARs 34898, 34902). | 2-95, 2-117 |
| | The "Analog-to-Digital Converter Block" section was extensively revised, reorganizing the information and adding the "ADC Theory of Operation" section and "Acquisition Time or Sample Time Control" section. The "ADC Configuration Example" section was reworked and corrected (SAR 34918). | 2-96 |

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