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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-fgg484k

Instant On

Flash-based Fusion devices are Level 0 Instant On. Instant On Fusion devices greatly simplify total system design and reduce total system cost by eliminating the need for CPLDs. The Fusion Instant On clocking (PLLs) replaces off-chip clocking resources. The Fusion mix of Instant On clocking and analog resources makes these devices an excellent choice for both system supervisor and system management functions. Instant On from a single 3.3 V source enables Fusion devices to initiate, control, and monitor multiple voltage supplies while also providing system clocks. In addition, glitches and brownouts in system power will not corrupt the Fusion device flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design. Flash-based Fusion devices simplify total system design and reduce cost and design risk, while increasing system reliability.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. Another source of radiation-induced firm errors is alpha particles. For an alpha to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in Fusion flash-based FPGAs. Once it is programmed, the flash cell configuration element of Fusion FPGAs cannot be altered by high-energy neutrons and is therefore immune to errors from them.

Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Fusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With Fusion devices, there is no power-on current surge and no high current transition, both of which occur on many FPGAs.

Fusion devices also have low dynamic power consumption and support both low power standby mode and very low power sleep mode, offering further power savings.

Advanced Flash Technology

The Fusion family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows very high logic utilization (much higher than competing SRAM technologies) without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary Fusion architecture provides granularity comparable to standard-cell ASICs. The Fusion device consists of several distinct and programmable architectural features, including the following (Figure 1-1 on page 1-5):

- Embedded memories
  - Flash memory blocks
  - FlashROM
  - SRAM and FIFO

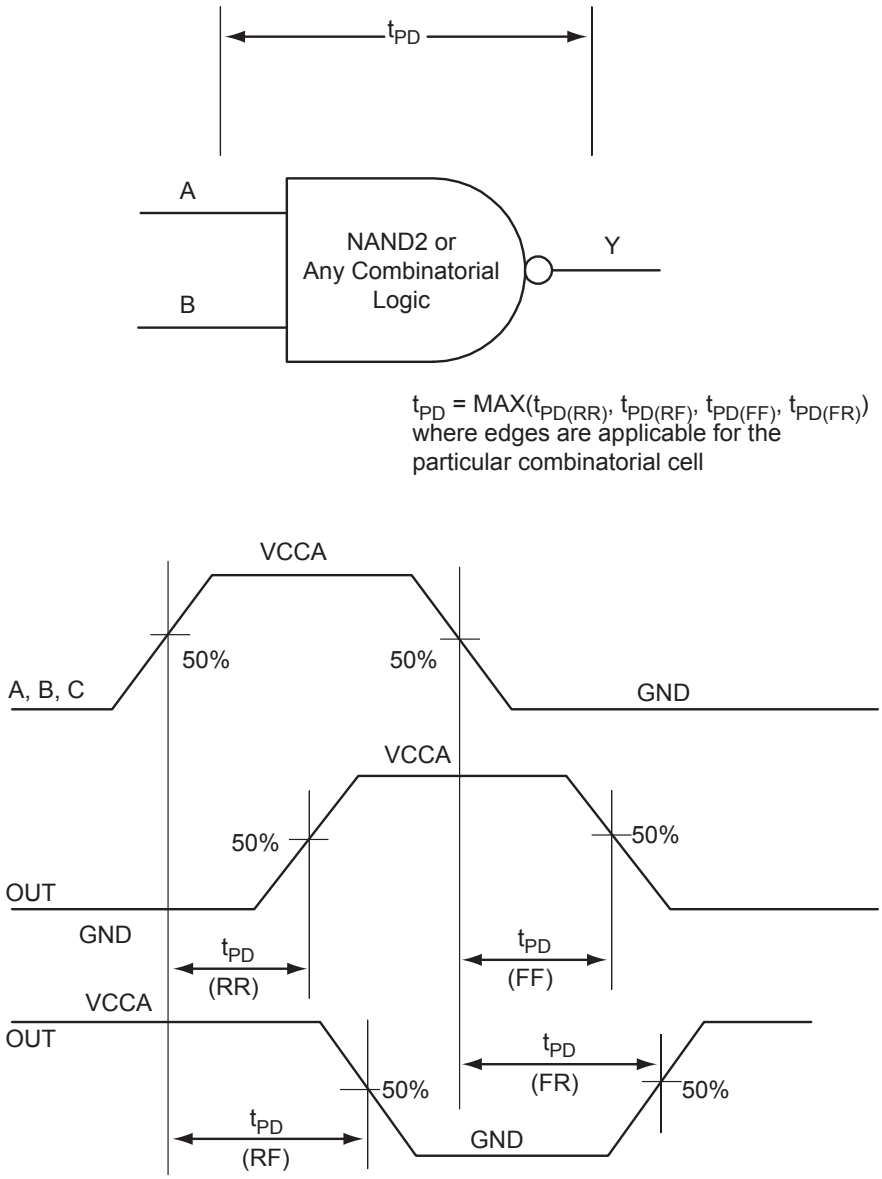


Figure 2-4 • **Combinatorial Timing Model and Waveforms**

Array Coordinates

During many place-and-route operations in the Microsemi Designer software tool, it is possible to set constraints that require array coordinates. Table 2-3 is provided as a reference. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

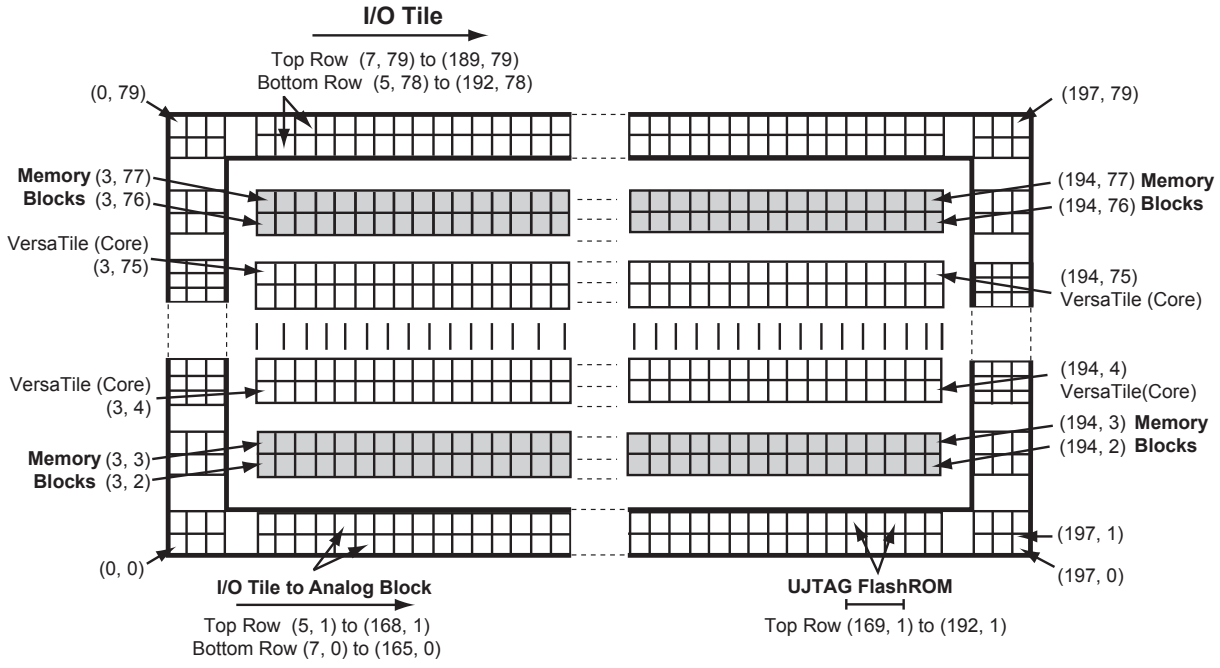
Table 2-3 provides array coordinates of core cells and memory blocks.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and edge core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-3. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-7 illustrates the array coordinates of an AFS600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for Fusion software tools.

Table 2-3 • **Array Coordinates**

Device	VersaTiles				Memory Rows		All	
	Min.		Max.		Bottom	Top	Min.	Max.
	x	y	x	y	(x, y)	(x, y)	(x, y)	(x, y)
AFS600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)
AFS1500	3	4	322	123	(3, 2)	(3, 124)	(0, 0)	(325, 129)



Note: The vertical I/O tile coordinates are not shown. West side coordinates are {(0, 2) to (2, 2)} to {(0, 77) to (2, 77)}; east side coordinates are {(195, 2) to (197, 2)} to {(195, 77) to (197, 77)}.

Figure 2-7 • **Array Coordinates for AFS600**

Global Buffers with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay (Figure 2-21). The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

The CLKDLY macro can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the Fusion family. The available INBUF macros are described in the *IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide.*

The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Libero SoC and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.

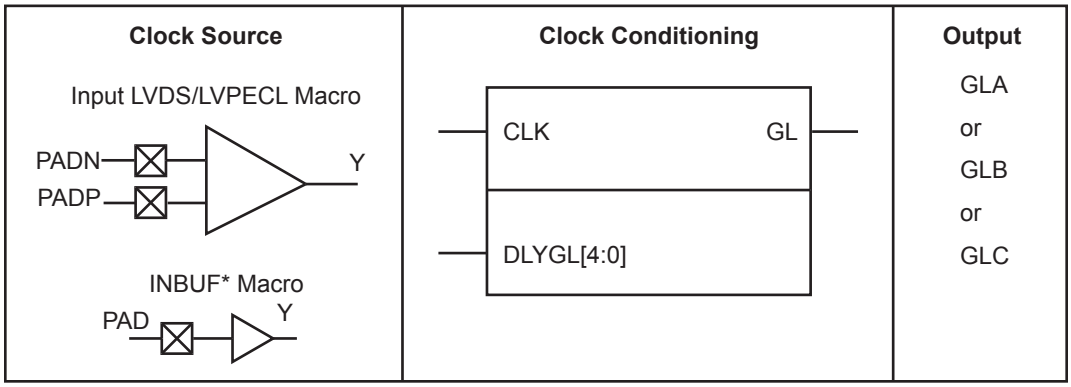


Figure 2-21 • **Fusion CCC Options: Global Buffers with Programmable Delay**

The NGMUX macro is simplified to show the two clock options that have been selected by the GLMUXCFG[1:0] bits. Figure 2-25 illustrates the NGMUX macro. During design, the two clock sources are connected to CLK0 and CLK1 and are controlled by GLMUXSEL[1:0] to determine which signal is to be passed through the MUX.

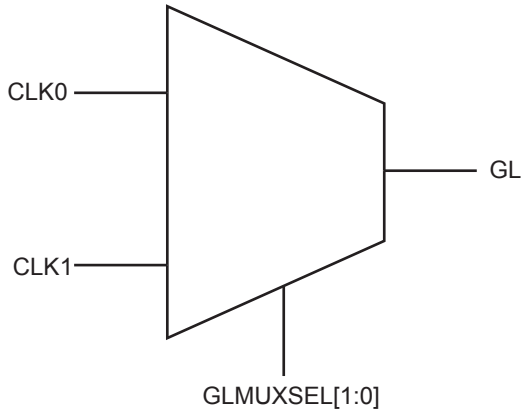


Figure 2-25 • **NGMUX Macro**

The sequence of switching between two clock sources (from CLK0 to CLK1) is as follows (Figure 2-26):

- GLMUXSEL[1:0] transitions to initiate a switch.
- GL drives one last complete CLK0 positive pulse (i.e., one rising edge followed by one falling edge).
- From that point, GL stays Low until the second rising edge of CLK1 occurs.
- At the second CLK1 rising edge, GL will begin to continuously deliver the CLK1 signal.
- Minimum t_{sw} = 0.05 ns at 25°C (typical conditions)

For examples of NGMUX operation, refer to the *Fusion FPGA Fabric User's Guide*.

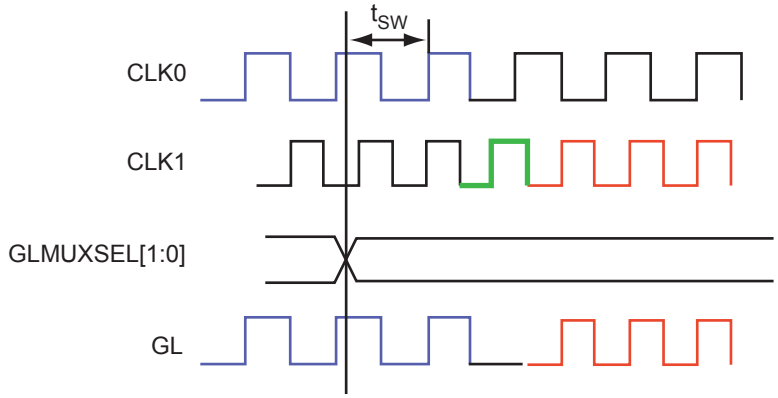


Figure 2-26 • **NGMUX Waveform**

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—1 clock edge): In the standard read mode, new data is driven onto the RD bus in the same clock cycle following RA and REN valid. The read address is registered on the read port clock active edge, and data appears at RD after the RAM access time. Setting PIPE to OFF enables this mode.
- Read Pipelined (synchronous—2 clock edges): The pipelined mode incurs an additional clock delay from the address to the data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.
- Write (synchronous—1 clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is High. The setup times of the write address, write enables, and write data are minimal with respect to the write clock. Write and read transfers are described with timing requirements in the "SRAM Characteristics" section on page 2-63 and the "FIFO Characteristics" section on page 2-72.

RAM Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism (refer to the "JTAG IEEE 1532" section on page 2-227 and the *Fusion SRAM/FIFO Blocks* application note). The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.

FIFO Flag Usage Considerations

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values, respectively. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag to assert when the write address exceeds the read address by at least a predefined value. In a 2k×8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

Timing Characteristics

Table 2-34 • FIFO, Worst Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup time	5.01	5.70	6.70	ns
t_{ENH}	REN, WEN Hold time	0.02	0.02	0.03	ns
t_{BKS}	BLK Setup time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold time	0.00	0.00	0.00	ns
t_{DS}	Input data (WD) Setup time	0.19	0.22	0.25	ns
t_{DH}	Input data (WD) Hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.43	2.77	3.25	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.92	1.05	1.23	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.77	2.02	2.37	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.68	1.92	2.25	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.38	7.27	8.55	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.75	1.99	2.34	ns
t_{RSTAF}	RESET Low to Almost-Empty/Full Flag Valid	6.32	7.20	8.46	ns
t_{RSTBQ}	RESET Low to Data out Low on RD (flow-through)	0.95	1.08	1.27	ns
	RESET Low to Data out Low on RD (pipelined)	0.95	1.08	1.27	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.34	0.39	ns
$t_{RECRSTB}$	RESET Recovery	1.55	1.76	2.07	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.22	0.25	0.29	ns
t_{CYC}	Clock Cycle time	3.33	3.79	4.46	ns
FMAX	Maximum Frequency for FIFO	300	264	224	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10 for derating values.

C_{GS} is not a fixed capacitance but, depending on the circuitry connected to its drain terminal, can vary significantly during the course of a turn-on or turn-off transient. Thus, EQ 6 on page 2-90 can only be used for a first-order estimate of the switching speed of the external MOSFET.

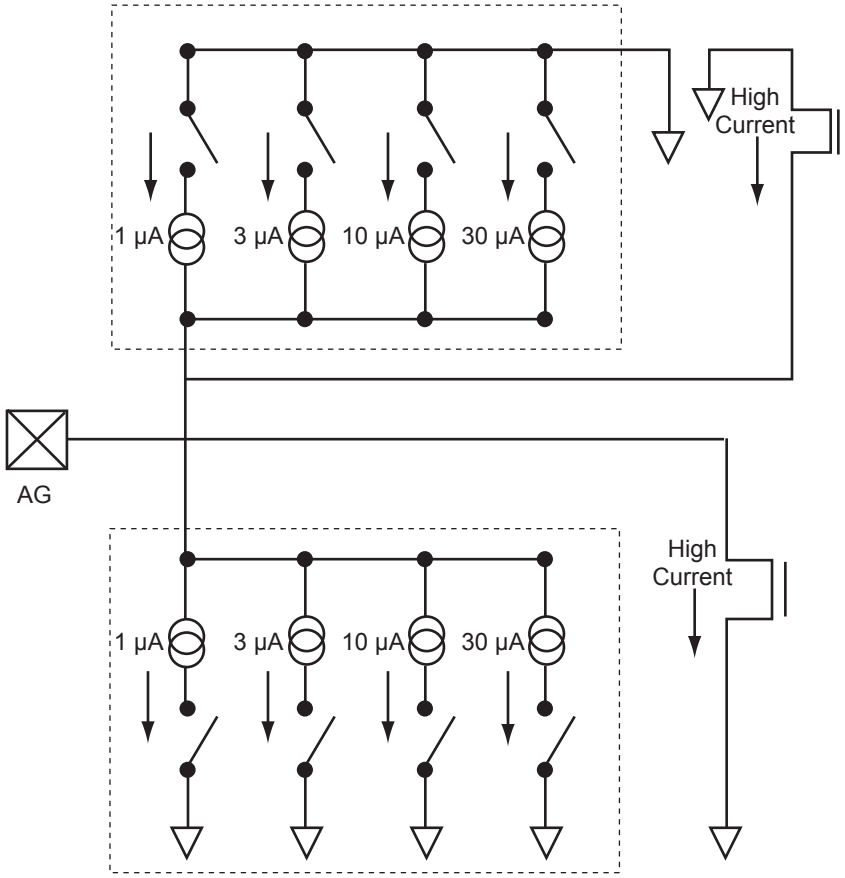


Figure 2-74 • **Gate Driver Example**

Table 2-50 • **Electrical Characteristics (continued)**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
Temperature Monitor						
	Resolution			1		ºC
	Accuracy			5	± 10	ºC
VMPWT	Strobe	Minimum Pulse Width	10			µs
Analog Input as a Digital Input						
VIND	Input voltage		–0.2		AVDD + 0.2	V
VHYSDIN	Hysteresis			0.3		V
VIHDIN	Input High			1.2		V
VILDIN	Input Low			0.9		V
VMPWDIN	Minimum pulse width		100			nS
I_{STBDIN}	Standby current				20	nA
I_{DYNDIN}	Dynamic current				20	µA
t_{INDIN}	Input delay			10		nS
Analog Output Pad (G pad)						
VG	Voltage Range		–12		12	V
IG	Minimum output current drive	High current mode at 1.0 V		25		mA
		Low current mode—1 µA		1		µA
		Low current mode—3 µA		3		µA
		Low current mode—10 µA		10		µA
		Low current mode—30 µA		30		µA
IOFFG	Maximum Off Current			100		µA

Notes:

1. *The sample rate is time-shared among active analog inputs.*
2. *The input voltage range for the temperature monitor block prescaler is 0 to 12 V.*
3. *VRSM is the maximum voltage drop across the current sense resistor.*

Table 2-96 • **I/O Short Currents IOSH/IOSL (continued)**

	Drive Strength	IOSH (mA)*	IOSL (mA)*
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Note: *T_J = 100°C*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-108 • 2.5 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	9.30	0.05	1.59	1.75	0.44	8.57	9.30	2.87	2.41	10.93	11.65	ns
	–1	0.58	7.91	0.04	1.36	1.49	0.38	7.29	7.91	2.44	2.05	9.30	9.91	ns
	–2	0.51	6.94	0.03	1.19	1.31	0.33	6.40	6.94	2.14	1.80	8.16	8.70	ns
8 mA	Std.	0.68	5.56	0.05	1.59	1.75	0.44	5.56	5.56	3.27	3.19	7.91	7.92	ns
	–1	0.58	4.73	0.04	1.36	1.49	0.38	4.73	4.73	2.78	2.72	6.73	6.73	ns
	–2	0.51	4.15	0.03	1.19	1.31	0.33	4.15	4.15	2.44	2.38	5.91	5.91	ns
12 mA	Std.	0.68	3.95	0.05	1.59	1.75	0.44	4.02	3.68	3.55	3.69	6.38	6.04	ns
	–1	0.58	3.36	0.04	1.36	1.49	0.38	3.42	3.13	3.02	3.14	5.43	5.14	ns
	–2	0.51	2.95	0.03	1.19	1.31	0.33	3.00	2.75	2.65	2.75	4.76	4.51	ns
16 mA	Std.	0.68	3.72	0.05	1.59	1.75	0.44	3.79	3.29	3.61	3.82	6.15	5.65	ns
	–1	0.58	3.16	0.04	1.36	1.49	0.38	3.22	2.80	3.07	3.25	5.23	4.80	ns
	–2	0.51	2.78	0.03	1.19	1.31	0.33	2.83	2.46	2.69	2.85	4.59	4.22	ns
24 mA	Std.	0.68	3.44	0.05	1.59	1.75	0.44	3.50	2.62	3.69	4.33	5.86	4.98	ns
	–1	0.58	2.93	0.04	1.36	1.49	0.38	2.98	2.23	3.14	3.68	4.99	4.23	ns
	–2	0.51	2.57	0.03	1.19	1.31	0.33	2.62	1.95	2.75	3.23	4.38	3.72	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Timing Characteristics

Table 2-113 • 1.8 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	16.70	0.05	1.53	2.01	0.44	16.50	16.70	2.93	1.67	18.86	19.06	ns
	–1	0.58	14.21	0.04	1.30	1.71	0.38	14.04	14.21	2.50	1.42	16.05	16.21	ns
	–2	0.51	12.47	0.03	1.14	1.50	0.33	12.32	12.47	2.19	1.25	14.09	14.23	ns
4 mA	Std.	0.68	12.01	0.05	1.53	2.01	0.44	12.24	11.34	3.43	2.92	14.59	13.70	ns
	–1	0.58	10.22	0.04	1.30	1.71	0.38	10.41	9.65	2.92	2.49	12.41	11.66	ns
	–2	0.51	8.97	0.03	1.14	1.50	0.33	9.14	8.47	2.56	2.18	10.90	10.23	ns
6 mA	Std.	0.68	9.46	0.05	1.53	2.01	0.44	9.54	8.54	3.76	3.54	11.99	10.90	ns
	–1	0.58	8.05	0.04	1.30	1.71	0.38	8.20	7.26	3.20	3.01	10.20	9.27	ns
	–2	0.51	7.06	0.03	1.14	1.50	0.33	7.20	6.38	2.81	2.64	8.96	8.14	ns
8 mA	Std.	0.68	8.81	0.05	1.53	2.01	0.44	8.97	8.00	3.84	3.71	11.33	10.36	ns
	–1	0.58	7.49	0.04	1.30	1.71	0.38	7.63	6.80	3.27	3.16	9.64	8.81	ns
	–2	0.51	6.58	0.03	1.14	1.50	0.33	6.70	5.97	2.87	2.77	8.46	7.73	ns
12 mA	Std.	0.68	8.37	0.05	1.53	2.01	0.44	8.53	7.97	3.95	4.33‘	10.89	10.33	ns
	–1	0.58	7.12	0.04	1.30	1.71	0.38	7.25	6.78	3.36	3.68	9.26	8.79	ns
	–2	0.51	6.25	0.03	1.14	1.50	0.33	6.37	5.95	2.85	3.23	8.13	7.71	ns
16 mA	Std.	0.68	8.37	0.05	1.53	2.01	0.44	8.53	7.97	3.95	4.33	10.89	10.33	ns
	–1	0.58	7.12	0.04	1.30	1.71	0.38	7.25	6.78	3.36	3.68	9.26	8.79	ns
	–2	0.51	6.25	0.03	1.14	1.50	0.33	6.37	5.95	2.95	3.23	8.13	7.71	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-116 • 1.8 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	12.51	0.05	1.53	0.44	9.63	12.51	2.92	1.75	11.99	14.87	ns
	–1	0.58	10.64	0.04	1.30	0.38	8.19	10.64	2.49	1.49	10.20	12.65	ns
	–2	0.51	9.34	0.03	1.14	0.33	7.19	9.34	2.18	1.30	8.96	11.10	ns
4 mA	Std.	0.68	7.44	0.05	1.53	0.44	6.18	7.29	3.40	2.99	8.54	9.65	ns
	–1	0.58	6.33	0.04	1.30	0.38	5.26	6.20	2.89	2.55	7.26	8.21	ns
	–2	0.51	5.55	0.03	1.14	0.33	4.62	5.45	2.54	2.23	6.38	7.21	ns
6 mA	Std.	0.68	4.77	0.05	1.53	0.44	4.41	4.69	3.72	3.57	6.77	7.05	ns
	–1	0.58	4.06	0.04	1.30	0.38	3.75	3.99	3.17	3.03	5.76	6.00	ns
	–2	0.51	3.56	0.03	1.14	0.33	3.29	3.50	2.78	2.66	5.05	5.26	ns
8 mA	Std.	0.68	4.35	0.05	1.53	0.44	4.14	4.14	3.80	3.71	6.50	6.50	ns
	–1	0.58	3.70	0.04	1.30	0.38	3.52	3.52	3.23	3.16	5.53	5.53	ns
	–2	0.51	3.25	0.03	1.14	0.33	3.09	3.09	2.83	2.77	4.85	4.85	ns
12 mA	Std.	0.68	4.00	0.05	1.53	0.44	3.80	3.21	3.90	4.30	6.15	5.57	ns
	–1	0.58	3.41	0.04	1.30	0.38	3.23	2.73	3.32	3.66	5.23	4.73	ns
	–2	0.51	2.99	0.03	1.14	0.33	2.83	2.40	2.91	3.21	4.60	4.16	ns
16 mA	Std.	0.68	4.00	0.05	1.53	0.44	3.80	3.21	3.90	4.30	6.15	5.57	ns
	–1	0.58	3.41	0.04	1.30	0.38	3.23	2.73	3.32	3.66	5.23	4.73	ns
	–2	0.51	2.99	0.03	1.14	0.33	2.83	2.40	2.91	3.21	4.60	4.16	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-145 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
17 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	17	17	87	83	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

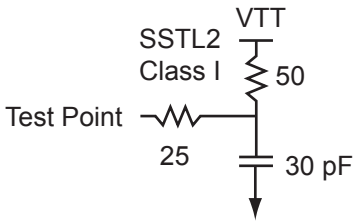


Figure 2-128 • AC Loading

Table 2-146 • SSTL2 Class I AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

Table 2-147 • SSTL 2 Class I
Extended Temperature Range Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.24	0.05	1.41	0.44	2.28	1.95			4.64	4.31	ns
–1	0.58	1.91	0.04	1.20	0.38	1.94	1.66			3.95	3.66	ns
–2	0.51	1.68	0.03	1.05	0.33	1.71	1.45			3.47	3.22	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-158 • LVDS AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

*Note: *Measuring point = V_{trip}. See Table 2-89 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-159 • LVDS
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.68	1.98	0.05	1.97	ns
–1	0.58	1.69	0.04	1.68	ns
–2	0.51	1.48	0.03	1.47	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-160 • LVDS
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.68	1.98	0.05	1.75	ns
–1	0.58	1.69	0.04	1.49	ns
–2	0.51	1.48	0.03	1.31	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations can contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The driver requires series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus, since the driver can be located anywhere on the bus. These configurations can be implemented using TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-133 on page 2-209. The input and output buffer delays are available in the LVDS section in Table 2-161 on page 2-210.

Output DDR

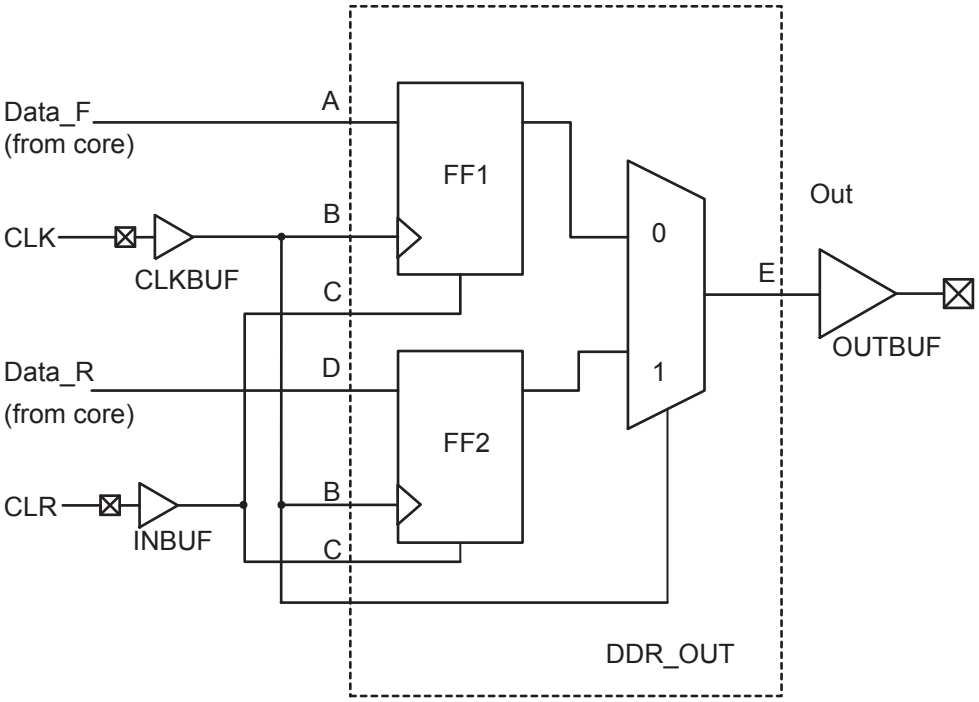


***Figure 2-142* • Output DDR Timing Model**

***Table 2-172* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

because SAMPLE is defined in the IEEE1532 specification as a noninvasive instruction. If the input buffers were to be enabled by SAMPLE temporarily turning on the I/Os, then it would not truly be a noninvasive instruction. Refer to the standard or the "In-System Programming (ISP) of Microsemi's Low Power Flash Devices Using FlashPro4/3/3X" chapter of the *Fusion FPGA Fabric User's Guide* for more details.

Boundary Scan

Fusion devices are compatible with IEEE Standard 1149.1, which defines a hardware architecture and the set of mechanisms for boundary scan testing. The basic Fusion boundary scan logic circuit is composed of the test access port (TAP) controller, test data registers, and instruction register (Figure 2-144 on page 2-229). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) and the optional IDCODE instruction (Table 2-176 on page 2-229).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI, TDO (test data input and output), TMS (test mode selector), and TRST (test reset input). TMS, TDI, and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary scan test usage. Refer to the "JTAG Pins" section on page 2-225 for pull-up/-down recommendations for TDO and TCK pins. The TAP controller is a 4-bit state machine (16 states) that operates as shown in Figure 2-144 on page 2-229. The 1s and 0s represent the values that must be present on TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

***Table 2-175* • TRST and TCK Pull-Down Recommendations**

VJTAG	Tie-Off Resistance*
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

*Note: *Equivalent parallel resistance if more than one device is on JTAG chain.*

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain High for five TCK cycles. The TRST pin can also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

Fusion devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (LSB, ID number, part number, and version). The boundary scan register observes and controls the state of each I/O pin. Each I/O cell has three boundary scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin.

The serial pins are used to serially connect all the boundary scan register cells in a device into a boundary scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

Table 3-2 • Recommended Operating Conditions[1]

Symbol	Parameter[2]	Ext. Temperature	Units
AC	Unpowered, ADC reset asserted or unconfigured	–10.5 to 11.6	V
	Analog input (+16 V to +2 V prescaler range)	–0.3 to 11.6	V
	Analog input (+1 V to +0.125 V prescaler range)	–0.3 to 3.6	V
	Analog input (–16 V to –2 V prescaler range)	–10.5 to 0.3	V
	Analog input (–1 V to –0.125 V prescaler range)	–3.6 to 0.3	V
	Analog input (direct input to ADC)	–0.3 to 3.6	V
	Analog input (positive current monitor)[8]	–0.3 to 11.6	V
	Analog input (negative current monitor)[7]	–10.5 to 0.3	V
	Digital input	–0.3 to 11.6	V
AG [4,5]	Unpowered, ADC reset asserted or unconfigured	–10.5 to 11.6	V
	Low Current Mode (1 µA, 3 µA, 10 µA, 30 µA)	–0.3 to 11.6	V
	Low Current Mode (–1 µA, –3 µA, –10 µA, –30 µA)	–10.5 to 0.3	V
	High Current Mode [5]	–10.5 to 11.6	V
AT [4]	Unpowered, ADC reset asserted or unconfigured	–0.3 to 14.5	V
	Analog input (+16 V, +4 V prescaler range)	–0.3 to 14.5	V
	Analog input (direct input to ADC)	–0.3 to 3.6	V
	Digital input	–0.3 to 14.5	V

Notes:

1. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-85 on page 2-158.*
2. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
3. *The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.*
4. *VPUMP can be left floating during normal operation (not programming mode).*
5. *The input voltage may overshoot by up to 500 mV above the Recommended Maximum (150 mV in Direct mode), provided the duration of the overshoot is less than 50% of the operating lifetime of the device.*
6. *Violating the VCC15A recommended voltage supply during an embedded flash program cycle can corrupt the page being programmed.*
7. *Negative input is not supported between –40°C and –55°C.*
8. *Positive input is not supported between –40°C and –55°C.*

FG256		
Pin Number	AFS600 Function	AFS1500 Function
K5	GND	GND
K6	IO65NDB4V0	IO96NDB4V0
K7	VCC	VCC
K8	GND	GND
K9	VCC	VCC
K10	GND	GND
K11	GDC2/IO57PPB2V0	GDC2/IO84PPB2V0
K12	GND	GND
K13	GDA0/IO54NDB2V0	GDA0/IO81NDB2V0
K14	GDA2/IO55PPB2V0	GDA2/IO82PPB2V0
K15	VCCIB2	VCCIB2
K16	GDB1/IO53PPB2V0	GDB1/IO80PPB2V0
L1	GEC1/IO63PDB4V0	GEC1/IO90PDB4V0
L2	GEC0/IO63NDB4V0	GEC0/IO90NDB4V0
L3	GEB1/IO62PDB4V0	GEB1/IO89PDB4V0
L4	GEB0/IO62NDB4V0	GEB0/IO89NDB4V0
L5	IO60NDB4V0	IO87NDB4V0
L6	GEC2/IO60PDB4V0	GEC2/IO87PDB4V0
L7	GNDA	GNDA
L8	AC2	AC2
L9	AV4	AV4
L10	AC5	AC5
L11	PTEM	PTEM
L12	TDO	TDO
L13	VJTAG	VJTAG
L14	IO57NPB2V0	IO84NPB2V0
L15	GDB2/IO56PPB2V0	GDB2/IO83PPB2V0
L16	IO55NPB2V0	IO82NPB2V0
M1	GND	GND
M2	GEA1/IO61PDB4V0	GEA1/IO88PDB4V0
M3	GEA0/IO61NDB4V0	GEA0/IO88NDB4V0
M4	VCCIB4	VCCIB4
M5	IO58NPB4V0	IO85NPB4V0
M6	AV0	AV0
M7	AC1	AC1
M8	AG3	AG3
M9	AC4	AC4

FG256		
Pin Number	AFS600 Function	AFS1500 Function
M10	AC6	AC6
M11	AG7	AG7
M12	VPUMP	VPUMP
M13	VCCIB2	VCCIB2
M14	TMS	TMS
M15	TRST	TRST
M16	GND	GND
N1	GEB2/IO59PDB4V0	GEB2/IO86PDB4V0
N2	IO59NDB4V0	IO86NDB4V0
N3	GEA2/IO58PPB4V0	GEA2/IO85PPB4V0
N4	VCC33PMP	VCC33PMP
N5	VCC15A	VCC15A
N6	AG0	AG0
N7	AC3	AC3
N8	AG5	AG5
N9	AV5	AV5
N10	AG6	AG6
N11	AC8	AC8
N12	GNDA	GNDA
N13	VCC33A	VCC33A
N14	VCCNVM	VCCNVM
N15	TCK	TCK
N16	TDI	TDI
P1	VCCNVM	VCCNVM
P2	GNDNVM	GNDNVM
P3	GNDA	GNDA
P4	AC0	AC0
P5	AG1	AG1
P6	AV1	AV1
P7	AG2	AG2
P8	AG4	AG4
P9	GNDA	GNDA
P10	AC7	AC7
P11	AV8	AV8
P12	AG8	AG8
P13	AV9	AV9
P14	ADCGNDREF	ADCGNDREF