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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	119
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs600-1fg256k

Email: info@E-XFL.COM

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Fusion Device Family Overview

FPGA logic or an on-chip soft microprocessor can access flash memory through the parallel interface. Since the flash parallel interface is implemented in the FPGA fabric, it can potentially be customized to meet special user requirements. For more information, refer to the *CoreCFI Handbook*. The flash memory parallel interface provides configurable byte-wide (×8), word-wide (×16), or dual-word-wide (×32) data port options. Through the programmable flash parallel interface, the on-chip and off-chip memories can be cascaded for wider or deeper configurations.

The flash memory has built-in security. The user can configure either the entire flash block or the small blocks to prevent unintentional or intrusive attempts to change or destroy the storage contents. Each onchip flash memory block has a dedicated controller, enabling each block to operate independently.

The flash block logic consists of the following sub-blocks:

- Flash block Contains all stored data. The flash block contains 64 sectors and each sector contains 33 pages of data.
- Page Buffer Contains the contents of the current page being modified. A page contains 8 blocks of data.
- Block Buffer Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic The flash memory stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

User Nonvolatile FlashROM

In addition to the flash blocks, Fusion devices have 1 Kbit of user-accessible, nonvolatile FlashROM onchip. The FlashROM is organized as 8×128-bit pages. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- · Version management

The FlashROM is written using the standard IEEE 1532 JTAG programming interface. Pages can be individually programmed (erased and written). On-chip AES decryption can be used selectively over public networks to securely load data such as security keys stored in the FlashROM for a user design.

The FlashROM can be programmed (erased and written) via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing.

The FlashPoint tool in the Fusion development software solutions, Libero SoC and Designer, has extensive support for flash memory blocks and FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using the Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

Fusion devices have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be written through a 4-bit port and read as a single bitstream. The SRAM blocks can be initialized from the flash memory blocks or via the device JTAG port (ROM emulation mode), using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and



Routing Architecture

The routing structure of Fusion devices is designed to provide high performance through a flexible fourlevel hierarchy of routing resources: ultra-fast local resources; efficient long-line resources; high-speed very-long-line resources; and the high-performance VersaNet networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 2-8). The exception to this is that the SET/CLR input of a VersaTile configured as a D-flip-flop is driven only by the VersaNet global network.

The efficient long-line resources provide routing for longer distances and higher-fanout connections. These resources vary in length (spanning one, two, or four VersaTiles), run both vertically and horizontally, and cover the entire Fusion device (Figure 2-9 on page 2-9). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Active buffers are inserted automatically by routing software to limit loading effects.

The high-speed very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: length ± 12 VersaTiles in the vertical direction and length ± 16 in the horizontal direction from a given core VersaTile (Figure 2-10 on page 2-10). Very long lines in Fusion devices, like those in ProASIC3 devices, have been enhanced. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or from internal logic (Figure 2-11 on page 2-11). These nets are typically used to distribute clocks, reset signals, and other high-fanout nets requiring minimum skew. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input on all VersaTiles.



Note: Input to the core cell for the D-flip-flop set and reset is only available via the VersaNet global network connection.



Global Resource Characteristics

AFS600 VersaNet Topology

Clock delays are device-specific. Figure 2-15 is an example of a global tree used for clock routing. The global tree presented in Figure 2-15 is driven by a CCC located on the west side of the AFS600 device. It is used to drive all D-flip-flops in the device.



Figure 2-15 • Example of Global Tree Use in an AFS600 Device for Clock Routing

Extended Temperature Fusion Family of Mixed Signal FPGAs

In RC network mode, the XTAL1 pin is connected to an RC circuit, as shown in Figure 2-17. The XTAL2 pin should be left floating. The RC value can be chosen based on Figure 2-18 for any desired frequency between 32 KHz and 4 MHz. The RC network mode can also accommodate an external clock source on XTAL1 instead of an RC circuit.

In Low gain, Medium gain, and High gain, an external crystal component or ceramic resonator can be added onto XTAL1 and XTAL2, as shown in Figure 2-16 on page 2-17. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.



Note: *Internal signal—does not exist in macro. Figure 2-17 • XTLOSC Macro



Figure 2-18 • Crystal Oscillator: RC Time Constant Values vs. Frequency (typical)

No-Glitch MUX (NGMUX)

Positioned downstream from the PLL/CCC blocks, the NGMUX provides a special switching sequence between two asynchronous clock domains that prevents generating any unwanted narrow clock pulses. The NGMUX is used to switch the source of a global between three different clock sources. Allowable inputs are either two PLL/CCC outputs or a PLL/CCC output and a regular net, as shown in Figure 2-24. The GLMUXCFG[1:0] configuration bits determine the source of the CLK inputs (i.e., internal signal or GLC). These are set by SmartGen during design but can also be changed by dynamically reconfiguring the PLL. The GLMUXSEL[1:0] bits control which clock source is passed through the NGMUX to the global network (GL). See Table 2-12.



Figure 2-24 • NGMUX

Table 2-12 •	NGMUX	Configuration	and Selection	Table
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GLMUXCFG[1:0]	GLMUXSEL[1:0]		Selected Input Signal	MUX Type
00	Х	0	GLA	2-to-1 GLMUX
	Х	1	GLC	
01	Х	0	GLA	2-to-1 GLMUX
	Х	1	GLINT	

Real-Time Counter System

The RTC system enables Fusion devices to support standby and sleep modes of operation to reduce power consumption in many applications.

- Sleep mode, typical 10 µA
- Standby mode (RTC running), typical 3 mA with 20 MHz

The RTC system is composed of five cores:

- RTC sub-block inside Analog Block (AB)
- Voltage Regulator and Power System Monitor (VRPSM)
- Crystal oscillator (XTLOSC); refer to the "Crystal Oscillator" section in the Fusion Clock Resources chapter of the *Fusion FPGA Fabric User's Guide* for more detail.
- Crystal clock; does not require instantiation in RTL
- 1.5 V voltage regulator; does not require instantiation in RTL

All cores are powered by 3.3 V supplies, so the RTC system is operational without a 1.5 V supply during standby mode. Figure 2-27 shows their connection.



Notes:

- 1. Signals are hardwired internally and do not exist in the macro core.
- 2. User is only required to instantiate the VRPSM macro if the user wishes to specify PUPO behavior of the voltage regulator to be different from the default, or employ user logic to shut the voltage regulator off.

Figure 2-27 • Real-Time Counter System (not all the signals are shown for the AB macro)



Modes of Operation

Standby Mode

Standby mode allows periodic power-up and power-down of the FPGA fabric. In standby mode, the real-time counter and crystal block are ON. The FPGA is not powered by disabling the 1.5 V voltage regulator. The 1.5 V voltage regulator can be enabled when the preset count is matched. Refer to the "Real-Time Counter (part of AB macro)" section for details. To enter standby mode, the RTC must be first configured and enabled. Then VRPSM is shut off by deasserting the VRPU signal. The 1.5 V voltage regulator is then disabled, and shuts off the 1.5 V output.

Sleep Mode

In sleep mode, the real-time counter and crystal blocks are OFF. The 1.5 V voltage regulator inside the VRPSM can only be enabled by the PUB or TRST pin. Refer to the "Voltage Regulator and Power System Monitor (VRPSM)" section on page 2-35 for details on power-up and power-down of the 1.5 V voltage regulator.

Standby and Sleep Mode Circuit Implementation

For extra power savings, VJTAG and VPUMP should be at the same voltage as VCC, floated or ground, during standby and sleep modes. Note that when VJTAG is not powered, the 1.5 V voltage regulator cannot be enabled through TRST.

VPUMP and VJTAG can control through an external switch. Microsemi recommends ADG839, ADG849, or ADG841 as possible switches. Figure 2-28 shows the implementation for controlling VPUMP. The IN signal of the switch can be connected to PTBASE of the Fusion device. VJTAG can be controlled in same manner.



Figure 2-28 • Implementation to Control VPUMP



Device Architecture

Read Operation

Read operations are designed to read data from the FB Array, Page Buffer, Block Buffer, or status registers. Read operations support a normal read and a read-ahead mode (done by asserting READNEXT). Also, the timing for Read operations is dependent on the setting of PIPE.

The following diagrams illustrate representative timing for Non-Pipe Mode (Figure 2-38) and Pipe Mode (Figure 2-39) reads of the flash memory block interface.



Figure 2-38 • Read Waveform (Non-Pipe Mode, 32-bit access)



Figure 2-39 • Read Waveform (Pipe Mode, 32-bit access)

Extended Temperature Fusion Family of Mixed Signal FPGAs

 VAREF		
 ADCGNDREF		
 AV0	DAVOUT0	
 AC0	DACOUT0	
 AT0	DATOUT0	
•	•	
 ÅV/9		
	DATOUTS	
	100	
•	AGU	
 ATRETURN9	AG1	
 DENAV0	•	
 DENAC0	AG9	<u> </u>
 DENAT0		
•		
 DENAV0		
 DENAC0		
 DENAT0		
 CMSTB0		
•		
 CSMTB9		
GDONU		
GDON9		
 IMS1B0		
•		
 TMSTB9		
 MODE[3:0]	BUSY	
 TVC[7:0]	CALIBRATE	
 STC[7:0]	DATAVALID	
 CHNUMBER[4:0]	SAMPLE	
 TMSTINT	RESULT[11:0]	
 ADCSTART	RTCMATCH	
VAREFSEL	RTCXTLMODE	
PWRDWN	RTCYTISE	
ADURESEI		
 PTCCLK		
SISULK		
 ACMWEN	ACMRDATA[7:0]	
 ACMRESET	[]	
 ACMWDATA		
ACMADDR		
AE	3	

Figure 2-63 • Analog Block Macro



Device Architecture

Table 2-57 details the settings available to control the prescaler values of the AV, AC, and AT pins. Note that the AT pin has a reduced number of available prescaler values.

Control Lines Bx[2:0]	Scaling Factor, Pad to ADC Input	LSB for an 8-Bit Conversion (mV) ¹	LSB for a 10-Bit Conversion (mV) ¹	LSB for a 12-Bit Conversion (mV) ¹	Full Scale Voltage in 10-Bit Mode ²	Range Name
000 ³	0.15625	64	16	4	16.368 V	16 V
001	0.3125	32	8	2	8.184 V	8 V
010 ³	0.625	16	4	1	4.092 V	4 V
011	1.25	8	2	0.5	2.046 V	2 V
100	2.5	4	1	0.25	1.023 V	1 V
101	5.0	2	0.5	0.125	0.5115 V	0.5 V
110	10.0	1	0.25	0.0625	0.25575 V	0.25 V
111	20.0	0.5	0.125	0.03125	0.127875 V	0.125 V

Table 2-57 • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

Notes:

1. LSB voltage equivalences assume VAREF = 2.56 V.

2. Full Scale voltage for n-bit mode: ((2ⁿ) - 1) x (LSB for a n-bit Conversion).

3. These are the only valid ranges for the temperature monitor block prescaler.

Table 2-58 details the settings available to control the MUX within each of the AV, AC, and AT circuits. This MUX determines whether the signal routed to the ADC is the direct analog input, prescaled signal, or output of either the Current Monitor Block or the Temperature Monitor Block.

Table 2-58 • Analog Multiplexer Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

Control Lines Bx[4]	Control Lines Bx[3]	ADC Connected To
0	0	Prescaler
0	1	Direct input
1	0	Current amplifier* temperature monitor
1	1	Not valid

Note: *Current monitor is not supported between –40°C and –55°C.

Table 2-59 details the settings available to control the Direct Analog Input switch for the AV, AC, and AT pins.

Table 2-59 •	Direct Analog Input Switch Control Truth Tal	ble—AV ($x = 0$), AC ($x = 1$), and AT ($x = 3$)
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Control Lines Bx[5]	Direct Input Switch
0	Off
1	On

Table 2-60 details the settings available to control the polarity of the signals coming to the AV, AC, and AT pins. Note that the only valid setting for the AT pin is logic 0 to support positive voltages.

Table 2-60 • Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)*

Control Lines Bx[6]	Input Signal Polarity
0 1	Positive

Table 2-60 • Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)*

Control Lines Bx[6]	Input Signal Polarity
1 ²	Negative

Notes:

1. The B3[6] signal for the AT pad should be kept at logic 0 to accept only positive voltages.

2. Negative input is not supported between -40°C and -55°C.

Table 2-61 details the settings available to either power down or enable the prescaler associated with the analog inputs AV, AC, and AT.

Table 2-61 • Prescaler Op Amp Power-Down Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

Control Lines Bx[7]	Prescaler Op Amp
0	Power-down
1	Operational

Table 2-62 details the settings available to enable the Current Monitor Block associated with the AC pin.

Table 2-62 • Current Monitor Input Switch Control Truth Table—AV (x = 0)

Control Lines B0[4]	Current Monitor Input Switch
0	Off
1 *	On

Note: Current monitor is not supported between –40°C and –55°C.

Table 2-63 details the settings available to configure the drive strength of the gate drive when not in highdrive mode.

Table 2-63 • Low-Drive Gate Driver Current Truth Table (AG)

Control Lines B2[3]	Control Lines B2[2]	Current (μA)
0	0	1
0	1	3
1	0	10
1	1	30

Table 2-64 details the settings available to set the polarity of the gate driver (either p-channel- or n-channel-type devices).

Table 2-64 • Gate Driver Polarity Truth Table (AG)

Control Lines B2[6]	Gate Driver Polarity
0	Positive
1	Negative

Table 2-65 details the settings available to turn on the Gate Driver and set whether high-drive mode is on or off.

Table 2-65 • Gate Driver Control Truth Table (AG)

Control Lines B2[7]	GDON	Gate Driver
0	0	Off
0	1	Low drive on
1	0	Off
1	1	High drive on

Table 2-66 details the settings available to turn on and off the chip internal temperature monitor.

5 V Output Tolerance

Fusion I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to $3.3 \vee LVTTL$ or $3.3 \vee LVCMOS$ mode, Fusion I/Os can directly drive signals into $5 \vee TTL$ receivers. In fact, VOL = 0.4 V and VOH = 2.4 V in both $3.3 \vee LVTTL$ and $3.3 \vee LVCMOS$ modes exceed the VIL = 0.8 V and VIH = 2 V level requirements of 5 V TTL receivers. Therefore, level '1' and level '0' will be recognized correctly by 5 V TTL receivers.

Simultaneously Switching Outputs and PCB Layout

Simultaneously switching outputs (SSOs) can produce signal integrity problems on adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCBs will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and VCCI dip noise. These two noise types are caused by rapidly changing currents through GND and VCCI package pin inductances during switching activities:

- Ground bounce noise voltage = L(GND) * di/dt
- VCCI dip noise voltage = L(VCCI) * di/dt

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to SSO bus are LVTTL/LVCMOS inputs, LVTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltages to the IC and, at the same time, maintaining signal integrity between devices.

Key issues that need to considered are as follows:

- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations

I/O Software Support

In the Fusion development software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 2-84 and Table 2-85 on page 2-158 list the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in Fusion support up to five different drive strengths.

 Table 2-84 •
 Fusion Advanced I/O Attributes vs. I/O Standard Applications

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3
LVCMOS 2.5 V	3	3	3	3	3	3
LVCMOS 2.5/5.0 V	3	3	3	3	3	3
LVCMOS 1.8 V	3	3	3	3	3	3
LVCMOS 1.5 V	3	3	3	3	3	3
PCI (3.3 V)			3		3	3
PCI-X (3.3 V)	3		3		3	3
LVDS, B-LVDS, M-LVDS			3			3
LVPECL						3

	Drive Strength	IOSH (mA)*	IOSL (mA)*
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Table 2-96 •	I/O Short Currents IOSH/IOSL	(continued))

Note: *T_J = 100°C

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

	Аррік		Auvano		anno								
Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
4 mA	Std.	0.68	12.02	0.05	1.38	0.44	11.83	12.02	2.82	2.33	14.19	14.38	ns
	-1	0.58	10.22	0.04	1.18	0.38	10.06	10.22	2.40	1.98	12.07	12.23	ns
	-2	0.51	8.97	0.03	1.03	0.33	8.83	8.97	2.11	1.74	10.59	10.74	ns
8 mA	Std.	0.68	8.39	0.05	1.38	0.44	8.55	8.24	3.22	3.05	10.91	10.60	ns
	-1	0.58	7.14	0.04	1.18	0.38	7.27	7.01	2.74	2.59	9.28	9.02	ns
	-2	0.51	6.27	0.03	1.03	0.33	6.38	6.15	2.40	2.28	8.15	7.91	ns
12 mA	Std.	0.68	6.52	0.05	1.38	0.44	6.64	6.24	3.48	3.50	8.99	8.60	ns
	-1	0.58	5.54	0.04	1.18	0.38	5.65	5.31	2.96	2.98	7.65	7.31	ns
	-2	0.51	4.87	0.03	1.03	0.33	4.96	4.66	2.60	2.62	6.72	6.42	ns
16 mA	Std.	0.68	6.08	0.05	1.38	0.44	6.19	5.83	3.54	3.63	8.55	8.18	ns
	-1	0.58	5.17	0.04	1.18	0.38	5.27	4.96	3.01	3.08	7.27	6.96	ns
	-2	0.51	4.54	0.03	1.03	0.33	4.62	4.35	2.65	2.71	6.38	6.11	ns
24 mA	Std.	0.68	5.81	0.05	1.38	0.44	5.80	5.81	3.62	4.08	8.16	8.16	ns
	–1	0.58	4.94	0.04	1.18	0.38	4.94	4.94	3.08	3.47	6.94	6.95	ns
	-2	0.51	4.34	0.03	1.03	0.33	4.33	4.34	2.70	3.05	6.09	6.10	ns

Table 2-109 • 2.5 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V Applicable to Advanced I/O Banks

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

HSTL Class I		VIL	VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
8 mA	-0.3	VREF - 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8	39	32	15	15

Table 2-139 • Minimum and Maximum DC Input and Output Levels

Notes:

1. I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. *I_{IH}* is the input leakage current per *I/O* pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



Figure 2-126 • AC Loading

Table 2-140 • HSTL Class I AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.

Timing Characteristics

Table 2-141 • HSTL Class I

Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.68	3.25	0.05	2.24	0.44	3.41	3.31			5.77	5.67	ns
-1	0.58	2.85	0.04	1.91	0.38	2.90	2.82			4.91	4.83	ns
-2	0.51	2.50	0.03	1.67	0.33	2.55	2.48			4.31	4.24	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.



Device Architecture

Output DDR



Figure 2-142 • Output DDR Timing Model

Table 2-172 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
t _{DDROCLKQ}	Clock-to-Out	B, E
t _{DDROCLR2Q}	Asynchronous Clear-to-Out	C, E
t _{DDROREMCLR}	Clear Removal	С, В
t _{DDRORECCLR}	Clear Recovery	С, В
t _{DDROSUD1}	Data Setup Data_F	А, В
t _{DDROSUD2}	Data Setup Data_R	D, B
t _{DDROHD1}	Data Hold Data_F	А, В
t _{DDROHD2} Data Hold Data_R		D, B



Pin Descriptions

Supply Pins

GND Ground

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ Ground (quiet)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND. Note: In FG256, FG484, and FG676 packages, GNDQ and GND pins are connected within the package and are labeled as GND pins in the respective package pin assignment tables.

ADCGNDREF Analog Reference Ground

Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.

GNDA Ground (analog)

Quiet ground supply voltage to the Analog Block of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation.

GNDAQ Ground (analog quiet)

Quiet ground supply voltage to the analog I/O of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation. Note: In FG256, FG484, and FG676 packages, GNDAQ and GNDA pins are connected within the package and are labeled as GNDA pins in the respective package pin assignment tables.

GNDNVM Flash Memory Ground

Ground supply used by the Fusion device's flash memory block module(s).

GNDOSC Oscillator Ground

Ground supply for both integrated RC oscillator and crystal oscillator circuit.

VCC15A Analog Power Supply (1.5 V)

1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry.

VCC33A Analog Power Supply (3.3 V)

3.3 V clean analog power supply input for use by the 3.3 V portion of the analog circuitry.

VCC33N Negative 3.3 V Output

This is the -3.3 V output from the voltage converter. A 2.2 μ F capacitor must be connected from this pin to ground.

VCC33PMP Analog Power Supply (3.3 V)

3.3 V clean analog power supply input for use by the analog charge pump. To avoid high current draw, VCC33PMP should be powered up simultaneously with or after VCC33A.

VCCNVM Flash Memory Block Power Supply (1.5 V)

1.5 V power supply input used by the Fusion device's flash memory block module(s). To avoid high current draw, VCC should be powered up before or simultaneously with VCCNVM.

VCCOSC Oscillator Power Supply (3.3 V)

Power supply for both integrated RC oscillator and crystal oscillator circuit. The internal 100 MHz oscillator, powered by the VCCOSC pin, is needed for device programming, operation of the VDDN33



DC and Power Characteristics

Table 3-1 •	Absolute	Maximum	Ratings	(continued)
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Symbol	Parameter	Limit	Units
AV	Unpowered, ADC reset asserted or unconfigured	-11.0 to 12.0	V
	Analog input (+16 V to +2 V prescaler range)	-0.4 to 12.0	V
	Analog input (+1 V to +0.125 V prescaler range)	-0.4 to 3.75	V
	Analog input (–16 V to –2 V prescaler range) ⁵	-11.0 to 0.4	V
	Analog input (–1 V to –0.125 V prescaler range) ⁵	-3.75 to 0.4	V
	Analog input (direct input to ADC)	-0.4 to 3.75	V
	Analog input (positive current monitor) ⁶	-0.4 to 12.0	V
	Analog input (negative current monitor) ⁵	-11.0 to 0.4	V
	Digital input	-0.4 to 12.0	V
AC	Unpowered, ADC reset asserted or unconfigured	-11.0 to 12.0	V
	Analog input (+16 V to +2 V prescaler range ⁾	-0.4 to 12.0	V
	Analog input (+1 V to +0.125 V prescaler range)	-0.4 to 3.75	V
	Analog input (–16 V to –2 V prescaler range) ⁵	-11.0 to 0.4	V
	Analog input (–1 V to –0.125 V prescaler range) ⁵	-3.75 to 0.4	V
	Analog input (direct input to ADC)	-0.4 to 3.75	V
	Analog input (positive current monitor) ⁶	–0.4 to 12.0	V
	Analog input (negative current monitor) ⁵	-11.0 to 0.4	V
	Digital input	-0.4 to 12.0	V
AG	Unpowered, ADC reset asserted or unconfigured	-11.0 to 12.0	V
	Low Current Mode (1 µA, 3 µA, 10 µA, 30 µA)	–0.4 to 12.0	V
	Low Current Mode (–1 µA, –3 µA, –10 µA, –30 µA)	-11.0 to 0.4	V
	High Current Mode ³	-11.0 to 12.0	V
AT	Unpowered, ADC reset asserted or unconfigured	–0.4 to 15.0	V
	Analog input (+16 V, 4 V prescaler range)	-0.4 to 15.0	V
	Analog input (direct input to ADC)	-0.4 to 3.75	V
	Digital input	–0.4 to 1650	V
T _{STG} ⁴	Storage temperature	–65 to 150	°C
T _J ⁴	Junction temperature	125	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-5.

2. Analog data not valid beyond 3.65 V.

3. The high current mode has a maximum power limit of 15 mW. Appropriate current limit resistors must be used, based on voltage on the pad.

4. For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.

5. Negative input is not supported between –40°C and –55°C.

6. Positive input is not supported between –40°C and –55°C.

Extended Temperature Fusion Family of Mixed Signal FPGAs

Standby Mode and Sleep Mode

 $P_{S-CELL} = 0 W$ $P_{C-CELL} = 0 W$ $P_{NET} = 0 W$ $P_{LOGIC} = 0 W$

I/O Input and Output Buffer Contribution—P_{I/O}

This example uses LVTTL 3.3 V I/O cells. The output buffers are 12 mA–capable, configured with high output slew and driving a 35 pF output load.

 F_{CLK} = 50 MHz Number of input pins used: N_{INPUTS} = 30 Number of output pins used: $N_{OUTPUTS}$ = 40 Estimated I/O buffer toggle rate: α_2 = 0.1 (10%) Estimated IO buffer enable rate: β_1 = 1 (100%)

Operating Mode

$$\begin{split} \mathsf{P}_{\mathsf{INPUTS}} &= \mathsf{N}_{\mathsf{INPUTS}} * (\alpha_2 \, / \, 2) * \mathsf{PAC9} * \mathsf{F}_{\mathsf{CLK}} \\ \mathsf{P}_{\mathsf{INPUTS}} &= 30 * (0.1 \, / \, 2) * 0.01739 * 50 \\ \mathsf{P}_{\mathsf{INPUTS}} &= 1.30 \text{ mW} \end{split}$$

$$\begin{split} \mathsf{P}_{\text{OUTPUTS}} &= \mathsf{N}_{\text{OUTPUTS}} * (\alpha_2 / 2) * \beta_1 * \mathsf{PAC10} * \mathsf{F}_{\text{CLK}} \\ \mathsf{P}_{\text{OUTPUTS}} &= 40 * (0.1 / 2) * 1 * 0.4747 * 50 \\ \mathsf{P}_{\text{OUTPUTS}} &= 47.47 \text{ mW} \end{split}$$

 $P_{I/O} = P_{INPUTS} + P_{OUTPUTS}$ $P_{I/O} = 1.30 \text{ mW} + 47.47 \text{ mW}$ $P_{I/O} = 48.77 \text{ mW}$

Standby Mode and Sleep Mode

P_{INPUTS} = 0 W

 $P_{OUTPUTS} = 0 W$ $P_{VO} = 0 W$

RAM Contribution—P_{MEMORY}

Frequency of Read Clock: $F_{READ-CLOCK} = 10 \text{ MHz}$ Frequency of Write Clock: $F_{WRITE-CLOCK} = 10 \text{ MHz}$ Number of RAM blocks: $N_{BLOCKS} = 20$ Estimated RAM Read Enable Rate: $\beta_2 = 0.125 (12.5\%)$ Estimated RAM Write Enable Rate: $\beta_3 = 0.125 (12.5\%)$

Operating Mode

$$\begin{split} \mathsf{P}_{\mathsf{MEMORY}} &= (\mathsf{N}_{\mathsf{BLOCKS}} * \mathsf{P}_{\mathsf{AC11}} * \beta_2 * \mathsf{F}_{\mathsf{READ-CLOCK}}) + (\mathsf{N}_{\mathsf{BLOCKS}} * \mathsf{P}_{\mathsf{AC12}} * \beta_3 * \mathsf{F}_{\mathsf{WRITE-CLOCK}}) \\ \mathsf{P}_{\mathsf{MEMORY}} &= (20 * 0.025 * 0.125 * 10) + (20 * 0.030 * 0.125 * 10) \\ \mathsf{P}_{\mathsf{MEMORY}} &= 1.38 \text{ mW} \end{split}$$

Standby Mode and Sleep Mode

P_{MEMORY} = 0 W