Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	172
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs600-1fgg484k

Related Documents

Datasheet

Core8051
www.microsemi.com/soc/ipdocs/Core8051_DS.pdf

Application Notes

Fusion FlashROM
http://www.microsemi.com/soc/documents/Fusion_FROM_AN.pdf
Fusion SRAM/FIFO Blocks
http://www.microsemi.com/soc/documents/Fusion_RAM_FIFO_AN.pdf
Using DDR in Fusion Devices
http://www.microsemi.com/soc/documents/Fusion_DDR_AN.pdf
Fusion Security
http://www.microsemi.com/soc/documents/Fusion_Security_AN.pdf
Using Fusion RAM as Multipliers
http://www.microsemi.com/soc/documents/Fusion_Multipliers_AN.pdf

Handbook

Cortex-M1 Handbook
www.microsemi.com/soc/documents/CortexM1_HB.pdf

User’s Guides

Fusion FPGA Fabric User’s Guide
http://www.microsemi.com/soc/documents/Fusion_UG.pdf
Designer User's Guide
http://www.microsemi.com/soc/documents/designer_UG.pdf
Fusion FPGA Fabric User’s Guide
http://www.microsemi.com/soc/documents/Fusion_UG.pdf
IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide
http://www.microsemi.com/soc/documents/pa3_libguide_ug.pdf
SmartGen, FlashROM, Flash Memory System Builder, and Analog System Builder User's Guide
http://www.microsemi.com/soc/documents/genguide_ug.pdf

White Papers

Fusion Technology
http://www.microsemi.com/soc/documents/Fusion_Tech_WP.pdf

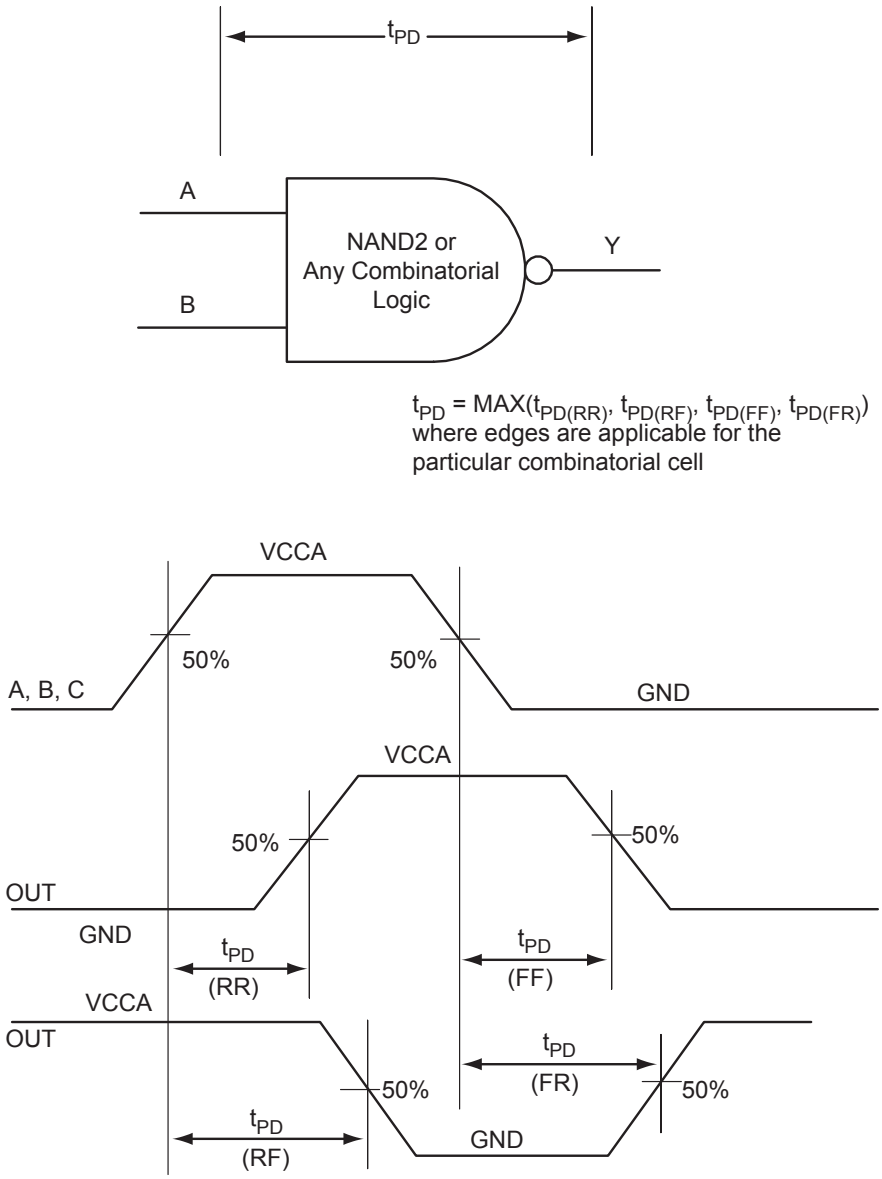
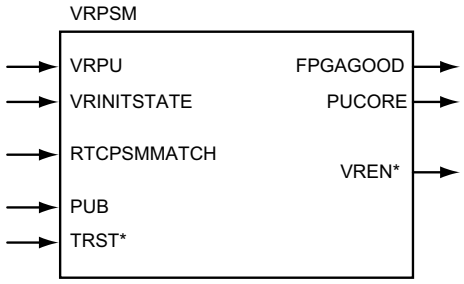


Figure 2-4 • **Combinatorial Timing Model and Waveforms**



*Note: *Signals are hardwired internally and do not exist in the macro core.*

Figure 2-30 • **VRPSM Macro**

Table 2-16 • **VRPSM Signal Descriptions**

Signal Name	Width	Dir.	Function
VRPU	1	In	Voltage Regulator Power-Up 0 – Voltage regulator disabled. PUB must be floated or pulled up, and the TRST pin must be grounded to disable the voltage regulator. 1 – Voltage regulator enabled
VRINITSTATE	1	In	Voltage Regulator Initial State Defines the voltage regulator status upon power-up of the 3.3 V. The signal is configured by Libero SoC when the VRPSM macro is generated. Tie off to 1 – Voltage regulator enables when 3.3 V is powered. Tie off to 0 – Voltage regulator disables when 3.3 V is powered.
RTCPSMMATCH	1	In	RTC Power System Management Match Connect from RTCPSMATCH signal from RTC in AB 0 transition to 1 turns on the voltage regulator
PUB	1	In	External pin, built-in weak pull-up Power-Up bar 0 – Enables voltage regulator at all times
TRST*	1	In	External pin, JTAG Test Reset 1 – Enables voltage regulator at all times
FPGAGOOD	1	Out	Indicator that the FPGA is powered and functional No need to connect if it is not used. 1 – Indicates that the FPGA is powered up and functional. 0 – Not possible to read by FPGA since it has already powered off.
PUCORE	1	Out	Power-Up Core Inverted signal of PUB. No need to connect if it is not used.
VREN*	1	Out	Voltage Regulator Enable Connected to 1.5 V voltage regulator in Fusion device internally. 0 – Voltage regulator disables 1 – Voltage regulator enables

*Note: *Signals are hardwired internally and do not exist in the macro core.*

Data operations are performed in widths of 1 to 4 bytes. A write to a location in a page that is not already in the Page Buffer will cause the page to be read from the FB Array and stored in the Page Buffer. The block that was addressed during the write will be put into the Block Buffer, and the data written by WD will overwrite the data in the Block Buffer. After the data is written to the Block Buffer, the Block Buffer is then written to the Page Buffer to keep both buffers in sync. Subsequent writes to the same block will overwrite the Block Buffer and the Page Buffer. A write to another block in the page will cause the addressed block to be loaded from the Page Buffer, and the write will be performed as described previously.

The data width can be selected dynamically via the DATAWIDTH input bus. The truth table for the data width settings is detailed in Table 2-20. The minimum resolvable address is one 8-bit byte. For data widths greater than 8 bits, the corresponding address bits are ignored—when DATAWIDTH = 0 (2 bytes), ADDR[0] is ignored, and when DATAWIDTH = '10' or '11' (4 bytes), ADDR[1:0] are ignored. Data pins are LSB-oriented and unused WD data pins must be grounded.

Table 2-20 • **Data Width Settings**

DATAWIDTH[1:0]	Data Width
00	1 byte [7:0]
01	2 byte [15:0]
10, 11	4 bytes [31:0]

Flash Memory Block Protection

Page Loss Protection

When the PAGELOSSPROTECT pin is set to logic 1, it prevents writes to any page other than the current page in the Page Buffer until the page is either discarded or programmed.

A write to another page while the current page is Page Loss Protected will return a STATUS of '11'.

Overwrite Protection

Any page that is Overwrite Protected will result in the STATUS being set to '01' when an attempt is made to either write, program, or erase it. To set the Overwrite Protection state for a page, set the OVERWRITEPROTECT pin when a Program operation is undertaken. To clear the Overwrite Protect state for a given page, an Unprotect Page operation must be performed on the page, and then the page must be programmed with the OVERWRITEPROTECT pin cleared to save the new page.

LOCKREQUEST

The LOCKREQUEST signal is used to give the user interface control over simultaneous access of the FB from both the User and JTAG interfaces. When LOCKREQUEST is asserted, the JTAG interface will hold off any access attempts until LOCKREQUEST is deasserted.

Flash Memory Block Operations

FB Operation Priority

The FB provides for priority of operations when multiple actions are requested simultaneously. Table 2-21 shows the priority order (priority 0 is the highest).

Table 2-21 • **FB Operation Priority**

Operation	Priority
System Initialization	0
FB Reset	1
Read	2
Write	3
Erase Page	4
Program	5
Unprotect Page	6
Discard Page	7

Timing Characteristics

Table 2-30 • RAM4K9, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.26	0.29	0.34	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.15	0.17	0.20	ns
t_{ENH}	REN, WEN hold time	0.10	0.11	0.13	ns
t_{BKS}	BLK setup time	0.24	0.27	0.32	ns
t_{BKH}	BLK hold time	0.02	0.02	0.03	ns
t_{DS}	Input data (DIN) setup time	0.19	0.22	0.25	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.84	2.10	2.47	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.43	2.77	3.25	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.92	1.05	1.23	ns
t_{C2CWWH} [1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.23	0.26	0.30	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.34	0.38	0.45	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.37	0.42	0.49	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	0.95	1.08	1.27	ns
	RESET Low to Data Out Low on DOUT (pipelined)	0.95	1.08	1.27	ns
$t_{REMRSTB}$	RESET removal	0.29	0.34	0.39	ns
$t_{RECRSTB}$	RESET recovery	1.55	1.76	2.07	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.22	0.25	0.29	ns
t_{CYC}	Clock cycle time	3.33	3.79	4.46	ns
FMAX	Maximum frequency	300	264	224	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.*

FIFO Flag Usage Considerations

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values, respectively. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag to assert when the write address exceeds the read address by at least a predefined value. In a 2k×8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

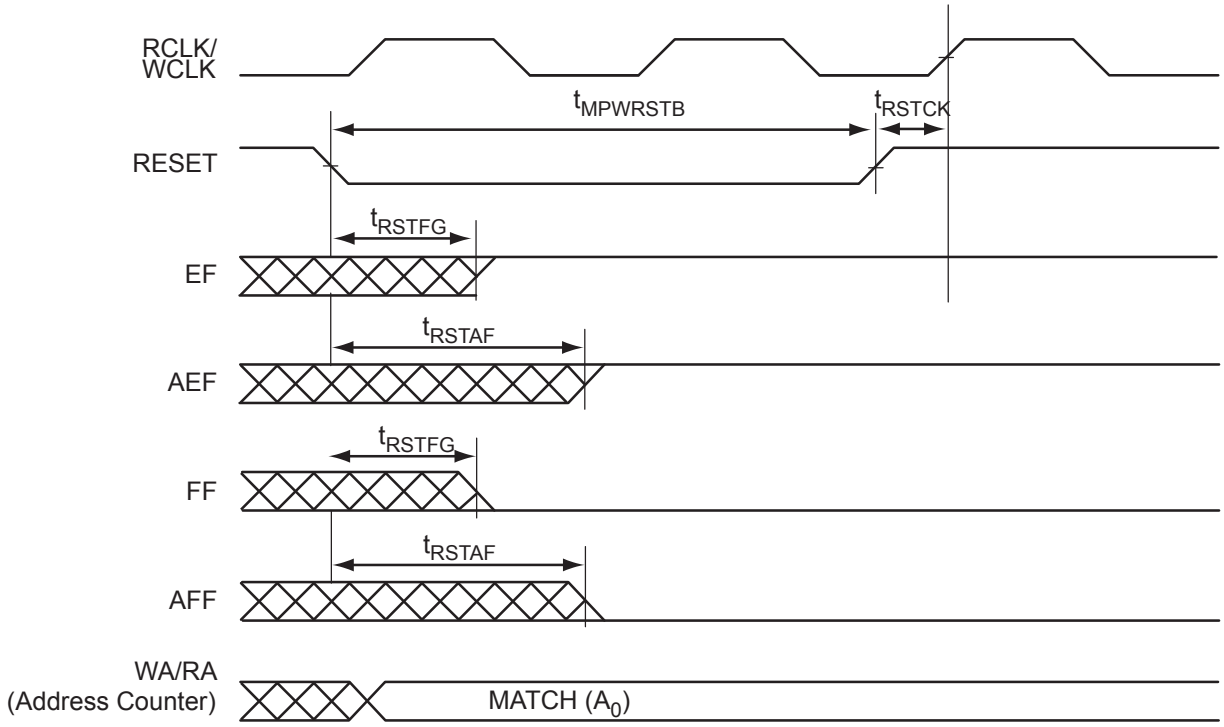


Figure 2-58 • **FIFO Reset**

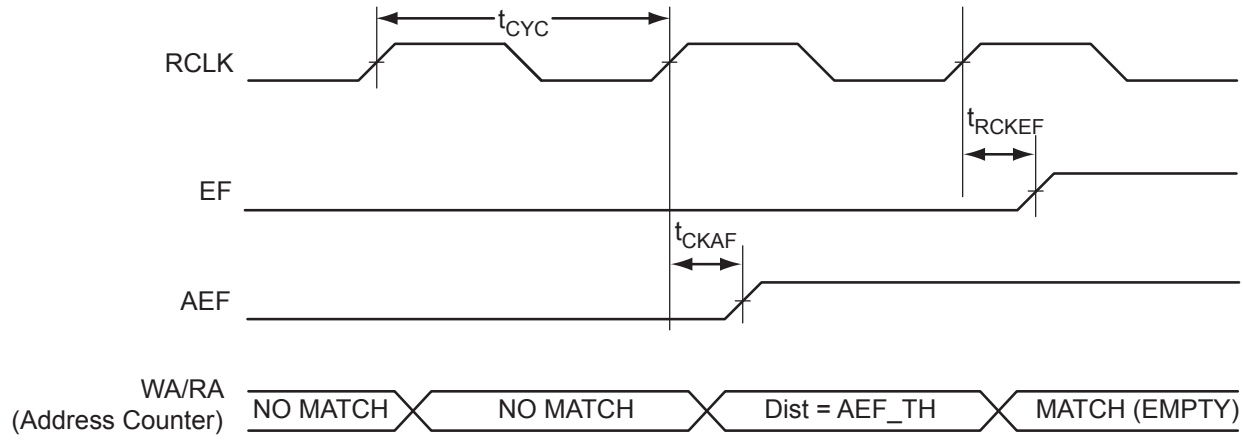


Figure 2-59 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

The third part of the Analog Quad is called the Gate Driver Block, and its output pin is named AG. This section is used to drive an external FET. There are two modes available: a High Current Drive mode and a Current Source Control mode. Both negative and positive voltage polarities are available, and in the current source control mode, four different current levels are available.

The fourth section of the Analog Quad is called the Temperature Monitor Block, and its input pin name is AT. This block is similar to the Voltage Monitor Block, except that it has an additional function: it can be used to monitor the temperature of an external diode-connected transistor. It has a modified prescaler and is limited to positive voltages only.

The Analog Quad can be configured during design time by Libero SoC; however, the ACM can be used to change the parameters of any of these I/Os during runtime. This type of change is referred to as a context switch. The Analog Quad is a modular structure that is replicated to generate the analog I/O resources. Each Fusion device supports between 5 and 10 Analog Quads.

The analog pads are numbered to clearly identify both the type of pad (voltage, current, gate driver, or temperature pad) and its corresponding Analog Quad (AV0, AC0, AG0, AT0, AV1, …, AC9, AG9, and AT9). There are three types of input pads (AVx, ACx, and ATx) and one type of analog output pad (AGx). Since there can be up to 10 Analog Quads on a device, there can be a maximum of 30 analog input pads and 10 analog output pads.

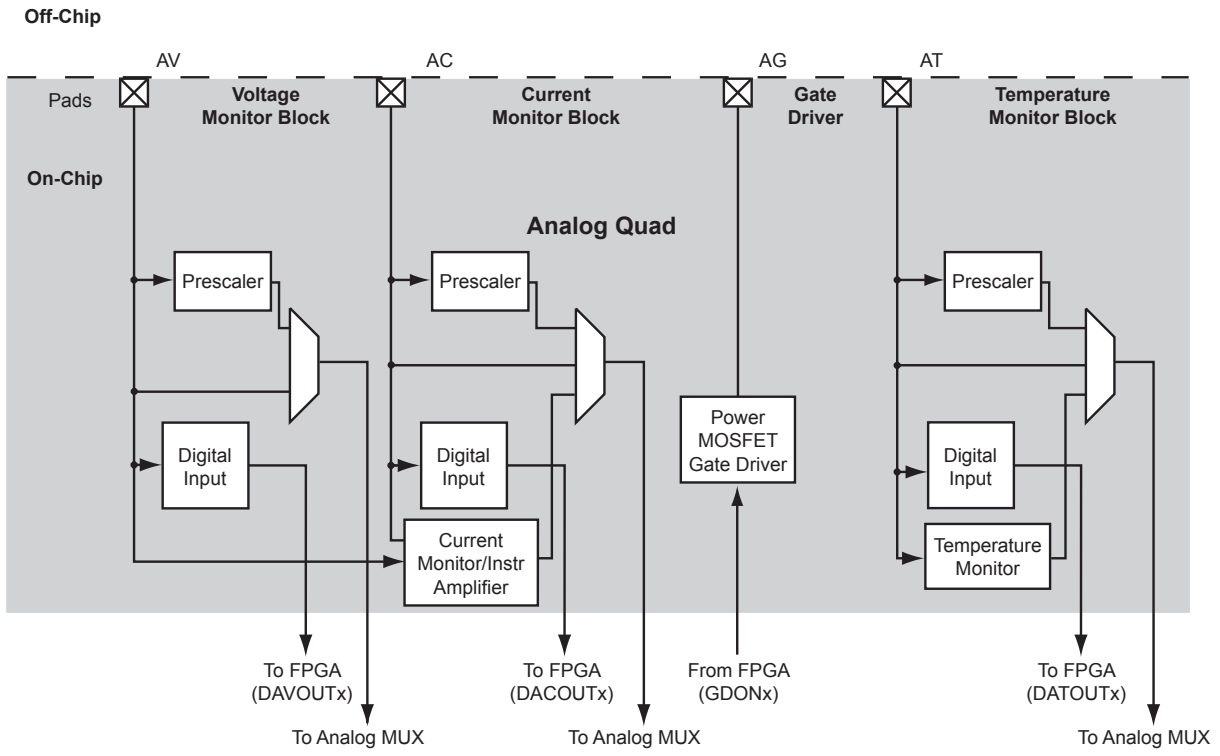


Figure 2-64 • **Analog Quad**

Direct Digital Input

The AV, AC, and AT pads can also be configured as high-voltage digital inputs (Figure 2-68). As these pads are 12 V–tolerant, the digital input can also be up to 12 V. However, the frequency at which these pads can operate is limited to 10 MHz.

To enable one of these analog input pads to operate as a digital input, its corresponding Digital Input Enable (DENA*xy*) pin on the Analog Block must be pulled High, where *x* is either V, C, or T (for AV, AC, or AT pads, respectively) and *y* is in the range 0 to 9, corresponding to the appropriate Analog Quad.

When the pad is configured as a digital input, the signal will come out of the Analog Block macro on the appropriate DA*x*OUT*y* pin, where *x* represents the pad type (V for AV pad, C for AC pad, or T for AT pad) and *y* represents the appropriate Analog Quad number. Example: If the AT pad in Analog Quad 5 is configured as a digital input, it will come out on the DATOUT5 pin of the Analog Block macro.

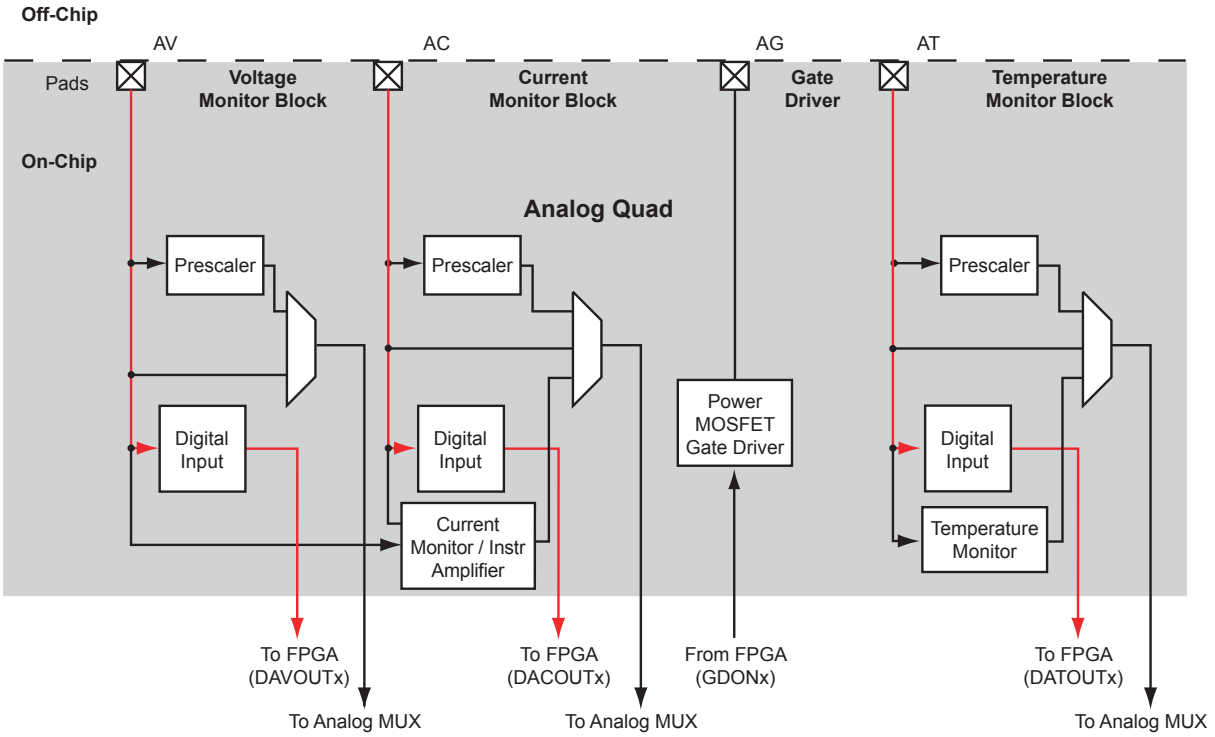


Figure 2-68 • **Analog Quad Direct Digital Input Configuration**

Typical Performance Characteristics

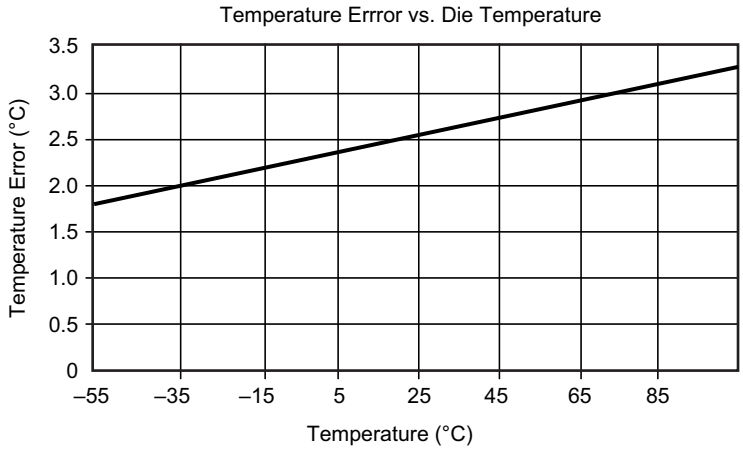


Figure 2-93 • **Temperature Error**

Table 2-48 • **Temperature vs. Average Fitted Error**

Temperature (°C)	Averaged Fitted Error
100	3.2469
90	3.1559
80	3.0649
70	2.9739
60	2.8829
50	2.7919
40	2.7009
30	2.6099
20	2.5189
10	2.4279
0	2.3369
–10	2.2459
–20	2.1549
–30	2.0639
–40	1.9729
–55	1.8364

Table 2-50 • **Electrical Characteristics**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
ADC						
VREFADC	Reference voltage	Internal reference		2.560		V
		External reference	2.527		VCC33A + 0.05	V
t_{CONV}	Conversion time	8-bit mode	1.67			µs
		10-bit mode	1.82			µs
		12-bit mode	2.00			µs
	Sample rate1	8-bit mode			600	ksps
		10-bit mode			550	ksps
		12-bit mode			500	ksps
All Analog Inputs (direct input)						
VINAD	Input voltage		–0.2		≤ VREF	V
CINAD	Input capacitance	Channel not selected		7		pF
		Channel selected, not sampling		8		pF
		Channel selected and sampling		18		pF
TUE	Total unadjusted error (external reference)	10-bit mode Input impedance 2 kΩ		2		LSB
All Analog Inputs (using prescaler)						
VINAP	Input voltage[2]		–12		12	V
	Accuracy	Positive DC inputs		1		%
		Negative DC inputs		2		%
	Offset			2 ± 0.2% of range		mV
	Bandwidth		100			kHz
	Impedance (2, 4, 8, and 12 V ranges)			1		MΩ
	Scaling factor	Pre-Scaler Modes (Table 2-35 on page 2-80)				
	Settling time	To 0.1% of final value			10	µs
Current Monitor						
VRSM	Maximum Differential Input				VREFADC/10	mV
	Resolution		1			mV
	Common Mode Range		–12		12	V
	Gain			10		
CMRR	Common mode rejection ratio	DC – 1 kHz		60		dB
		1 kHz – 10 kHz		50		dB
		> 10 kHz		30		dB
	Pole			100		kHz
VMPWC	Strobe	Minimum Pulse Width	10			µs

Notes:

1. *The sample rate is time-shared among active analog inputs.*
2. *The input voltage range for the temperature monitor block prescaler is 0 to 12 V.*
3. *VRSM is the maximum voltage drop across the current sense resistor.*

Table 2-57 details the settings available to control the prescaler values of the AV, AC, and AT pins. Note that the AT pin has a reduced number of available prescaler values.

Table 2-57 • **Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[2:0]	Scaling Factor, Pad to ADC Input	LSB for an 8-Bit Conversion (mV)[1]	LSB for a 10-Bit Conversion (mV)[1]	LSB for a 12-Bit Conversion (mV)[1]	Full Scale Voltage in 10-Bit Mode[2]	Range Name
000[3]	0.15625	64	16	4	16.368 V	16 V
001	0.3125	32	8	2	8.184 V	8 V
010[3]	0.625	16	4	1	4.092 V	4 V
011	1.25	8	2	0.5	2.046 V	2 V
100	2.5	4	1	0.25	1.023 V	1 V
101	5.0	2	0.5	0.125	0.5115 V	0.5 V
110	10.0	1	0.25	0.0625	0.25575 V	0.25 V
111	20.0	0.5	0.125	0.03125	0.127875 V	0.125 V

Notes:

1. *LSB voltage equivalences assume VAREF = 2.56 V.*
2. *Full Scale voltage for n-bit mode: ((2^n) - 1) x (LSB for a n-bit Conversion).*
3. *These are the only valid ranges for the temperature monitor block prescaler.*

Table 2-58 details the settings available to control the MUX within each of the AV, AC, and AT circuits. This MUX determines whether the signal routed to the ADC is the direct analog input, prescaled signal, or output of either the Current Monitor Block or the Temperature Monitor Block.

Table 2-58 • **Analog Multiplexer Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[4]	Control Lines Bx[3]	ADC Connected To
0	0	Prescaler
0	1	Direct input
1	0	Current amplifier* temperature monitor
1	1	Not valid

*Note: *Current monitor is not supported between –40°C and –55°C.*

Table 2-59 details the settings available to control the Direct Analog Input switch for the AV, AC, and AT pins.

Table 2-59 • **Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[5]	Direct Input Switch
0	Off
1	On

Table 2-60 details the settings available to control the polarity of the signals coming to the AV, AC, and AT pins. Note that the only valid setting for the AT pin is logic 0 to support positive voltages.

Table 2-60 • **Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)***

Control Lines Bx[6]	Input Signal Polarity
0 [1]	Positive

Temporary overshoots are allowed according to Table 3-4 on page 3-5.

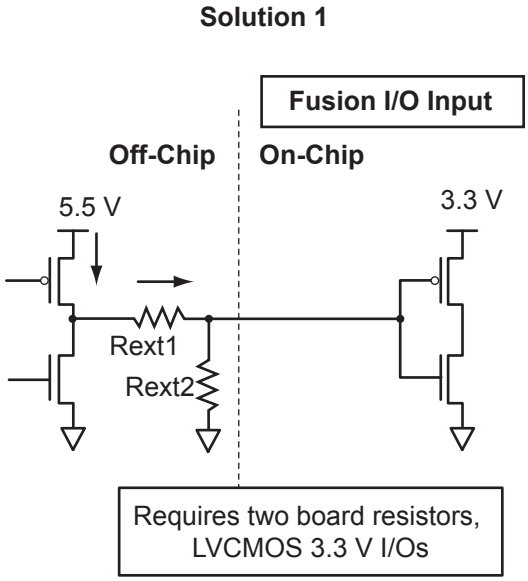


Figure 2-102 • **Solution 1**

Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-5. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and Zener, as shown in Figure 2-103. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

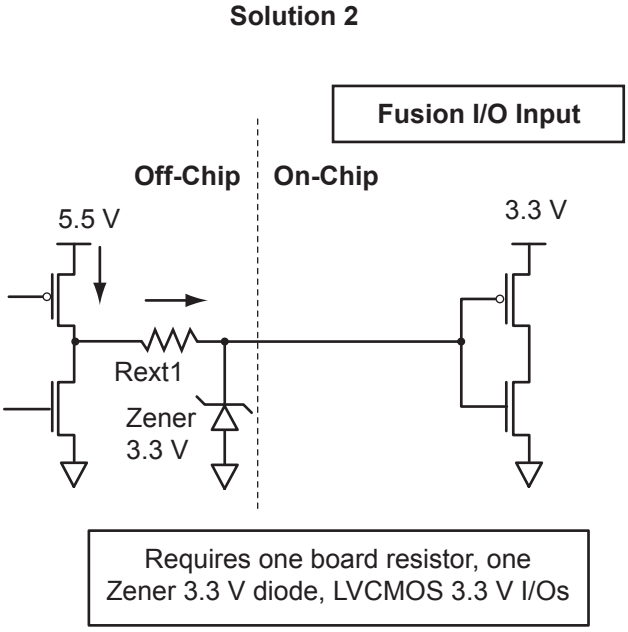


Figure 2-103 • **Solution 2**

Table 2-104 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	10.81	0.05	1.27	0.44	11.01	9.38	2.79	2.59	13.37	11.74	ns
	–1	0.58	9.20	0.04	1.08	0.38	9.37	7.98	2.37	2.20	11.38	9.99	ns
	–2	0.51	8.08	0.03	0.95	0.33	8.23	7.01	2.08	1.93	9.99	8.77	ns
8 mA	Std.	0.68	7.67	0.05	1.27	0.44	7.81	6.63	3.14	3.21	10.17	8.98	ns
	–1	0.58	6.53	0.04	1.08	0.38	6.65	5.64	2.67	2.73	8.65	7.64	ns
	–2	0.51	5.73	0.03	0.95	0.33	5.83	4.95	2.35	2.39	7.60	6.71	ns
12 mA	Std.	0.68	5.89	0.05	1.27	0.44	5.99	5.14	3.38	3.60	8.35	7.49	ns
	–1	0.58	5.01	0.04	1.08	0.38	5.10	4.37	2.88	3.06	7.10	6.38	ns
	–2	0.51	4.39	0.03	0.95	0.33	4.48	3.84	2.52	2.69	6.24	5.60	ns
16 mA	Std.	0.68	5.49	0.05	1.27	0.44	5.59	4.81	3.43	3.70	7.95	7.17	ns
	–1	0.58	4.67	0.04	1.08	0.38	4.76	4.09	2.92	3.15	6.76	6.10	ns
	–2	0.51	4.10	0.03	0.95	0.33	4.18	3.59	2.56	2.77	5.94	5.36	ns
24 mA	Std.	0.68	5.11	0.05	1.27	0.44	5.21	4.79	3.50	4.10	7.57	7.15	ns
	–1	0.58	4.35	0.04	1.08	0.38	4.43	4.08	2.98	3.48	6.44	6.08	ns
	–2	0.51	3.82	0.03	0.95	0.33	3.89	3.58	2.61	3.06	5.65	5.34	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-154 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
24 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	24	24	109	103	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

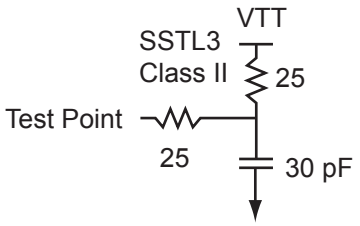


Figure 2-131 • AC Loading

Table 2-155 • SSTL3 Class II AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

*Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

Table 2-156 • SSTL3- Class II
Extended Temperature Range Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.18	0.05	1.32	0.44	2.22	1.76			4.58	4.12	ns
–1	0.58	1.85	0.04	1.12	0.38	1.89	1.50			3.89	3.51	ns
–2	0.51	1.63	0.03	0.99	0.33	1.66	1.32			3.42	3.08	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

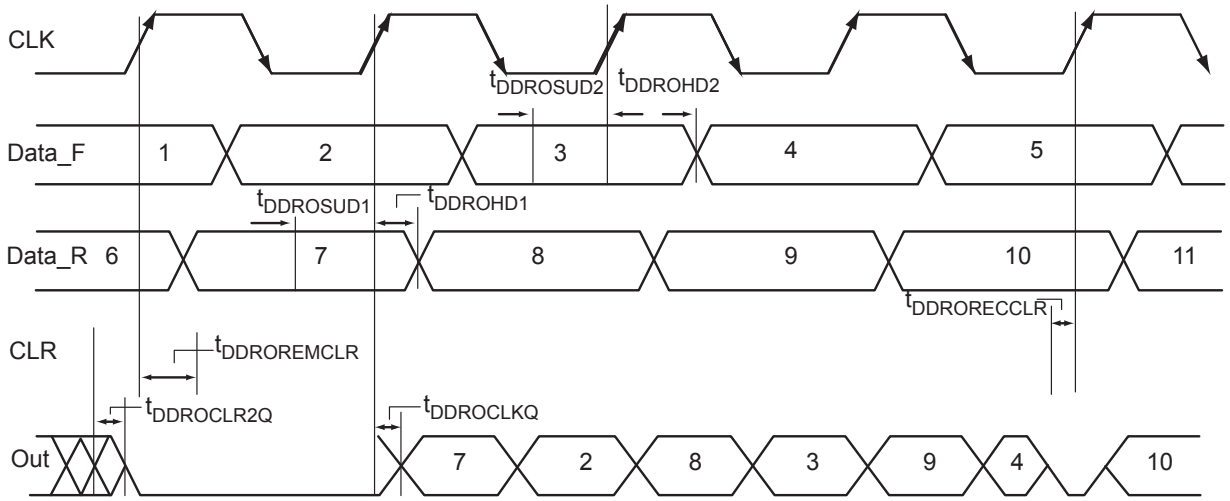


***Figure 2-143* • Output DDR Timing Diagram**

Timing Characteristics

***Table 2-173* • Output DDR Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.72	0.82	0.97	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.39	0.44	0.52	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.39	0.43	0.52	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.83	0.94	1.11	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	0.26	0.31	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.36	0.41	0.48	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.37	0.43	ns
FDDOMAX	Maximum Frequency for the Output DDR	1,404	1,232	1,048	MHz

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

IEEE 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/Os" section on page 2-133 for more details.

Timing Characteristics

***Table 2-177* • JTAG 1532**
Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.50	0.58	0.68	ns
t_{DIHD}	Test Data Input Hold Time	1.00	1.15	1.35	ns
t_{TMSSU}	Test Mode Select Setup Time	0.50	0.58	0.68	ns
t_{TMDHD}	Test Mode Select Hold Time	1.00	1.15	1.35	ns
t_{TCK2Q}	Clock to Q (data out)	6.00	5.75	6.77	ns
t_{RSTB2Q}	Reset to Q (data out)	20.00	23.00	27.06	ns
FTCKMAX	TCK Maximum Frequency	25.00	23.00	20.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.20	0.23	0.27	ns
$t_{TRSTMPW}$	ResetB minimum pulse	TBD	TBD	TBD	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse		TBD	TBD	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Methodology

Total Power Consumption—P_{TOTAL}

Operating Mode, Standby Mode, and Sleep Mode

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

Operating Mode

$P_{STAT} = PDC1 + (N_{NVM\text{-}BLOCKS} * PDC4) + PDC5+ (N_{QUADS} * P_{DC6}) + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8}) + (N_{PLLS} * PDC9)$

$N_{NVM\text{-}BLOCKS}$ is the number of NVM blocks available in the device.

N_{QUADS} is the number of Analog Quads used in the design.

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = PDC2$

Sleep Mode

$P_{STAT} = PDC3$

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB}$

Standby Mode

$P_{DYN} = P_{XTL\text{-}OSC}$

Sleep Mode

$P_{DYN} = 0$ W

Global Clock Dynamic Contribution—P_{CLOCK}

Operating Mode

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

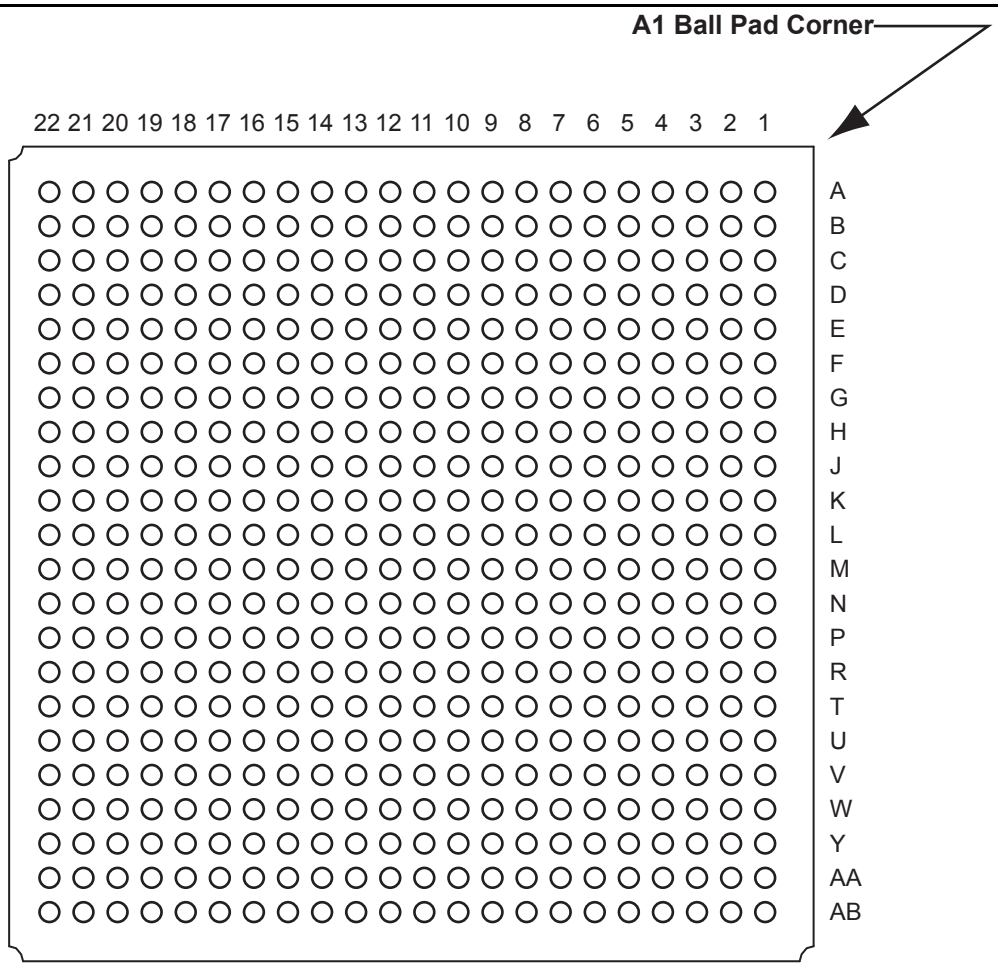
F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Sleep Mode

$P_{CLOCK} = 0$ W

FG484



Note

For Package Manufacturing and Environmental information, visit the Resource Center at www.microsemi.com/soc/products/solutions/package/default.aspx.

FG484		
Pin Number	AFS600 Function	AFS1500 Function
V3	VCCIB4	VCCIB4
V4	GEA1/IO61PDB4V0	GEA1/IO88PDB4V0
V5	GEA0/IO61NDB4V0	GEA0/IO88NDB4V0
V6	GND	GND
V7	VCC33PMP	VCC33PMP
V8	NC	NC
V9	VCC33A	VCC33A
V10	AG4	AG4
V11	AT4	AT4
V12	ATRTN2	ATRTN2
V13	AT5	AT5
V14	VCC33A	VCC33A
V15	NC	NC
V16	VCC33A	VCC33A
V17	GND	GND
V18	TMS	TMS
V19	VJTAG	VJTAG
V20	VCCIB2	VCCIB2
V21	TRST	TRST
V22	TDO	TDO
W1	NC	IO93PDB4V0
W2	GND	GND
W3	NC	IO93NDB4V0
W4	GEB2/IO59PDB4V0	GEB2/IO86PDB4V0
W5	IO59NDB4V0	IO86NDB4V0
W6	AV0	AV0
W7	GNDA	GNDA
W8	AV1	AV1
W9	AV2	AV2
W10	GNDA	GNDA
W11	AV3	AV3
W12	AV6	AV6
W13	GNDA	GNDA
W14	AV7	AV7
W15	AV8	AV8

FG484		
Pin Number	AFS600 Function	AFS1500 Function
W16	GNDA	GNDA
W17	AV9	AV9
W18	VCCIB2	VCCIB2
W19	NC	IO68PPB2V0
W20	TCK	TCK
W21	GND	GND
W22	NC	IO76PPB2V0
Y1	GEC2/IO60PDB4V0	GEC2/IO87PDB4V0
Y2	IO60NDB4V0	IO87NDB4V0
Y3	GEA2/IO58PDB4V0	GEA2/IO85PDB4V0
Y4	IO58NDB4V0	IO85NDB4V0
Y5	NCAP	NCAP
Y6	AC0	AC0
Y7	VCC33A	VCC33A
Y8	AC1	AC1
Y9	AC2	AC2
Y10	VCC33A	VCC33A
Y11	AC3	AC3
Y12	AC6	AC6
Y13	VCC33A	VCC33A
Y14	AC7	AC7
Y15	AC8	AC8
Y16	VCC33A	VCC33A
Y17	AC9	AC9
Y18	ADCGNDREF	ADCGNDREF
Y19	PTBASE	PTBASE
Y20	GNDNVM	GNDNVM
Y21	VCCNVM	VCCNVM
Y22	VPUMP	VPUMP