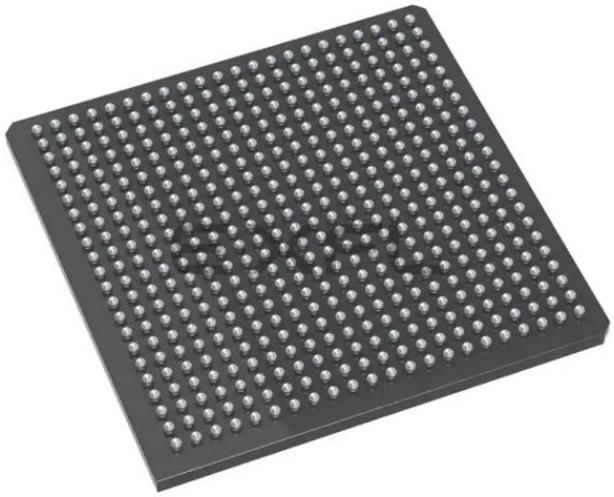

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	172
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs600-fg484k

Modes of Operation

Standby Mode

Standby mode allows periodic power-up and power-down of the FPGA fabric. In standby mode, the real-time counter and crystal block are ON. The FPGA is not powered by disabling the 1.5 V voltage regulator. The 1.5 V voltage regulator can be enabled when the preset count is matched. Refer to the "Real-Time Counter (part of AB macro)" section for details. To enter standby mode, the RTC must be first configured and enabled. Then VRPSM is shut off by deasserting the VRPU signal. The 1.5 V voltage regulator is then disabled, and shuts off the 1.5 V output.

Sleep Mode

In sleep mode, the real-time counter and crystal blocks are OFF. The 1.5 V voltage regulator inside the VRPSM can only be enabled by the PUB or TRST pin. Refer to the "Voltage Regulator and Power System Monitor (VRPSM)" section on page 2-35 for details on power-up and power-down of the 1.5 V voltage regulator.

Standby and Sleep Mode Circuit Implementation

For extra power savings, VJTAG and VPUMP should be at the same voltage as VCC, floated or ground, during standby and sleep modes. Note that when VJTAG is not powered, the 1.5 V voltage regulator cannot be enabled through TRST.

VPUMP and VJTAG can control through an external switch. Microsemi recommends ADG839, ADG849, or ADG841 as possible switches. Figure 2-28 shows the implementation for controlling VPUMP. The IN signal of the switch can be connected to PTBASE of the Fusion device. VJTAG can be controlled in same manner.

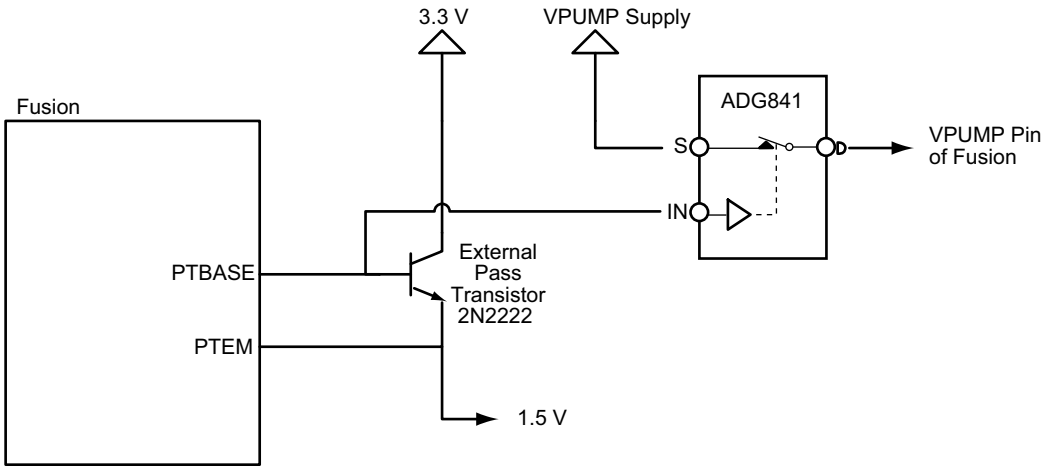


Figure 2-28 • **Implementation to Control VPUMP**

FlashROM

Fusion devices have 1 kbit of on-chip nonvolatile flash memory that can be read from the FPGA core fabric. The FlashROM is arranged in eight banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read-back of the FlashROM from the FPGA core (Figure 2-45).

The FlashROM can only be programmed via the IEEE 1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the eight 128-bit banks can be selectively reprogrammed. The FlashROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FlashROM supports a synchronous read and can be read on byte boundaries. The upper three bits of the FlashROM address from the FPGA core define the bank that is being accessed. The lower four bits of the FlashROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

The maximum FlashROM access clock is given in Table 2-25 on page 2-55. Figure 2-46 on page 2-55 shows the timing behavior of the FlashROM access cycle—the address has to be set up on the rising edge of the clock for DOUT to be valid on the next falling edge of the clock.

If the address is unchanged for two cycles:

If the address is unchanged for two cycles:

- D0 becomes invalid t_{CK2Q} ns after the second rising edge of the clock.
- D0 becomes valid again t_{CK2Q} ns after the second falling edge.

If the address unchanged for three cycles:

- D0 becomes invalid t_{CK2Q} ns after the second rising edge of the clock.
- D0 becomes valid again t_{CK2Q} ns after the second falling edge.
- D0 becomes invalid t_{CK2Q} ns after the third rising edge of the clock.
- D0 becomes valid again t_{CK2Q} ns after the third falling edge.

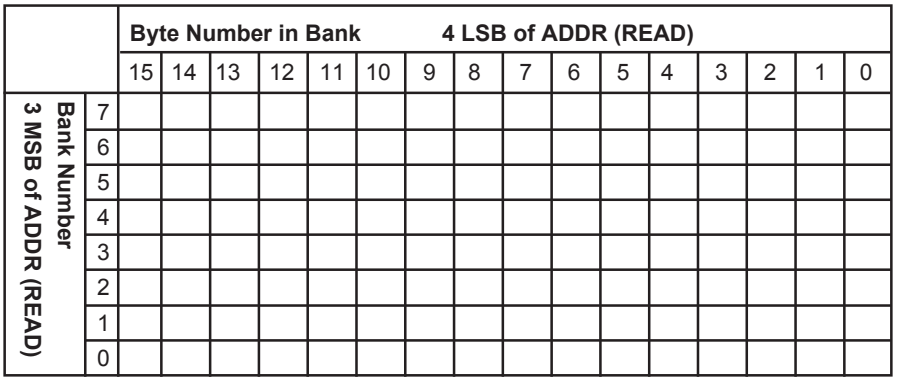
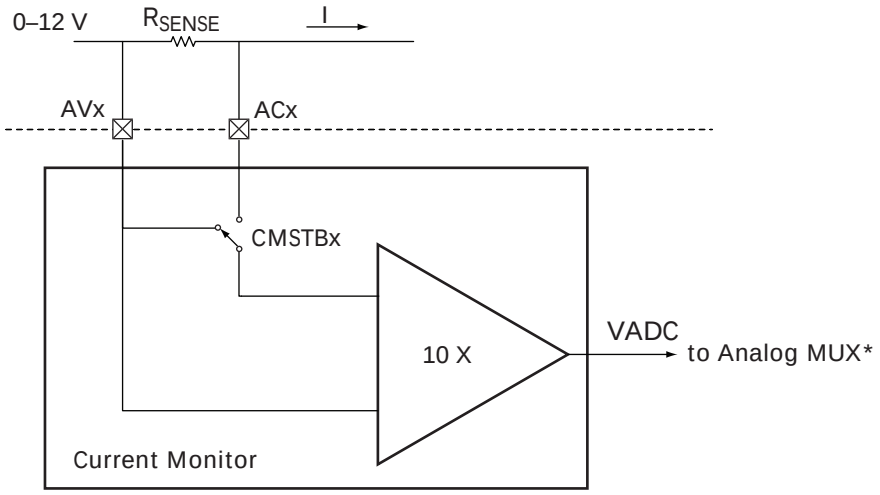


Figure 2-45 • **FlashROM Architecture**



*Note: *Refer to Table 2-39 on page 2-105 for the MUX channel number.*

Figure 2-71 • **Positive Current Monitor**

Care must be taken when choosing the right resistor for current measurement application. Note that because of the 10× amplification, the maximum measurable difference between the AV and AC pads is V_{AREF} / 10. A larger AV-to-AC voltage drop will result in ADC saturation; that is, the digital code put out by the ADC will stay fixed at the full scale value. Therefore, the user must select the external sense resistor appropriately. Table 2-36 on page 2-89 shows recommended resistor values for different current measurement ranges. When choosing resistor values for a system, there is a trade-off between measurement accuracy and power consumption. Choosing a large resistor will increase the voltage drop and hence increase accuracy of the measurement; however the larger voltage drop dissipates more power ($P = I^2 \times R$).

The Current Monitor is a unipolar system, meaning that the differential voltage swing must be from 0 V to VAREF/10. Therefore, the Current Monitor only supports differential voltage where |VAV-VAC| is greater than 0 V. This results in the requirement that the potential of the AV pad must be larger than the potential of the AC pad. This is straightforward for positive voltage systems. For a negative voltage system, it means that the AV pad must be "more negative" than the AC pad. This is shown in Figure 2-72 on page 2-89.

In this case, both the AV pad and the AC pad are configured for negative operations and the output of the differential amplifier still falls between 0 V and VAREF as required.

ADC Description

The Fusion ADC is a 12-bit SAR ADC. It offers a wide variety of features for different use models. Figure 2-79 shows a block diagram of the Fusion ADC.

- Configurable resolution: 8-bit, 10-bit, and 12-bit mode
- DNL: 0.6 LSB for 10-bit mode
- INL: 0.4 LSB for 10-bit mode
- No missing code
- Internal VAREF = 2.56 V
- Maximum Sample Rate = 600 Ksps
- Power-up calibration and dynamic calibration after every sample to compensate for temperature drift over time

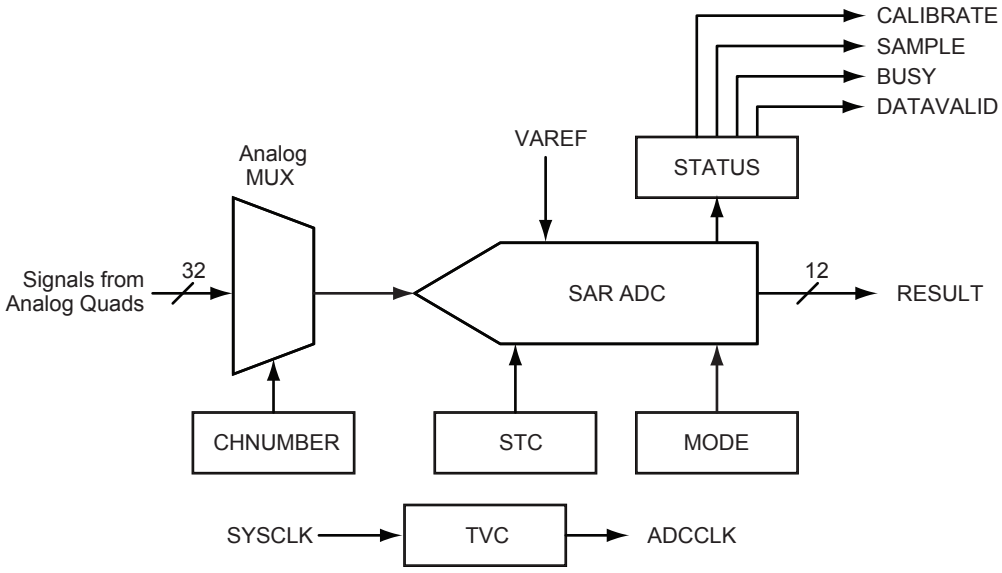


Figure 2-79 • **ADC Simplified Block Diagram**

ADC Theory of Operation

An analog-to-digital converter is used to capture discrete samples of a continuous analog voltage and provide a discrete binary representation of the signal. Analog-to-digital converters are generally characterized in three ways:

- Input voltage range
- Resolution
- Bandwidth or conversion rate

The input voltage range of an ADC is determined by its reference voltage (VREF). Fusion devices include an internal 2.56 V reference, or the user can supply an external reference of up to 3.3 V. The following examples use the internal 2.56 V reference, so the full-scale input range of the ADC is 0 to 2.56 V.

The resolution (LSB) of the ADC is a function of the number of binary bits in the converter. The ADC approximates the value of the input voltage using 2n steps, where n is the number of bits in the converter. Each step therefore represents VREF÷ 2n volts. In the case of the Fusion ADC configured for 12-bit operation, the LSB is 2.56 V / 4096 = 0.625 mV.

Finally, bandwidth is an indication of the maximum number of conversions the ADC can perform each second. The bandwidth of an ADC is constrained by its architecture and several key performance characteristics.

Table 2-39 • **Analog MUX Channels (continued)**

Analog MUX Channel	Signal	Analog Quad Number
16	AV5	Analog Quad 5
17	AC5	
18	AT5	
19	AV6	Analog Quad 6
20	AC6	
21	AT6	
22	AV7	Analog Quad 7
23	AC7	
24	AT7	
25	AV8	Analog Quad 8
26	AC8	
27	AT8	
28	AV9	Analog Quad 9
29	AC9	
30	AT9	
31	Internal temperature monitor	

The ADC can be powered down independently of the FPGA core, as an additional control or for power-saving considerations, via the PWRDWN pin of the Analog Block. The PWRDWN pin controls only the comparators in the ADC.

ADC Modes

The Fusion ADC can be configured to operate in 8-, 10-, or 12-bit modes, power-down after conversion, and dynamic calibration. This is controlled by MODE[3:0], as defined in Table 2-40.

The output of the ADC is the RESULT[11:0] signal. In 8-bit mode, the Most Significant 8 Bits RESULT[11:4] are used as the ADC value and the Least Significant 4 Bits RESULT[3:0] are logical '0's. In 10-bit mode, RESULT[11:2] are used the ADC value and RESULT[1:0] are logical 0s.

Table 2-40 • **Mode Bits Function**

Name	Bits	Function
MODE	3	0 – Internal calibration after every conversion; two ADCCLK cycles are used after the conversion. 1 – No calibration after every conversion
MODE	2	0 – Power-down after conversion 1 – No Power-down after conversion
MODE	1:0	00 – 10-bit 01 – 12-bit 10 – 8-bit 11 – Unused

Integrated Voltage Reference

The Fusion device has an integrated on-chip 2.56 V reference voltage for the ADC. The value of this reference voltage was chosen to make the prescaling and postscaling factors for the prescaler blocks change in a binary fashion. However, if desired, an external reference voltage of up to 3.3 V can be

along with the use of the active bipolar prescaler, current monitor, or temperature monitor, the minimum sample time(s) for each must be obeyed. EQ 19 can be used to determine the appropriate value of STC.

You can calculate the minimum actual acquisition time by using EQ 16:

$$VOUT = VIN(1 - e^{-t/RC})$$

EQ 16

For 0.5 LSB gain error, VOUT should be replaced with (VIN –(0.5 × LSB Value)):

$$(VIN - 0.5 \times LSB\ Value) = VIN(1 - e^{-t/RC})$$

EQ 17

where VIN is the ADC reference voltage (VREF)

Solving EQ 17:

$$t = RC \times \ln (VIN / (0.5 \times LSB\ Value))$$

EQ 18

where $R = Z_{INAD} + R_{SOURCE}$ and $C = C_{INAD}$.

Calculate the value of STC by using EQ 19.

$$t_{SAMPLE} = (2 + STC) \times (1 / ADCCLK) \text{ or } t_{SAMPLE} = (2 + STC) \times (ADC\ Clock\ Period)$$

EQ 19

where ADCCLK = ADC clock frequency in MHz.

t_{SAMPLE} = 0.449 µs from bit resolution in Table 2-43.

ADC Clock frequency = 10 MHz or a 100 ns period.

STC = (t_{SAMPLE} / (1 / 10 MHz)) – 2 = 4.49 – 2 = 2.49.

You must round up to 3 to accommodate the minimum sample time.

***Table 2-43* • Acquisition Time Example with VAREF = 2.56 V**

VIN = 2.56V, R = 4K (R_{SOURCE} ~ 0), C = 18 pF		
Resolution	**LSB Value (mV)**	**Min. Sample/Hold Time for 0.5 LSB (µs)**
8	10	0.449
10	2.5	0.549
12	0.625	0.649

***Table 2-44* • Acquisition Time Example with VAREF = 3.3 V**

VIN = 3.3V, R = 4K (R_{SOURCE} ~ 0), C = 18 pF		
Resolution	**LSB Value (mV)**	**Min. Sample/Hold time for 0.5 LSB (µs)**
8	12.891	0.449
10	3.223	0.549
12	0.806	0.649

Sample Phase

A conversion is performed in three phases. In the first phase, the analog input voltage is sampled on the input capacitor. This phase is called sample phase. During the sample phase, the output signals BUSY and SAMPLE change from '0' to '1', indicating the ADC is busy and sampling the analog signal. The sample time can be controlled by input signals STC[7:0]. The sample time can be calculated by EQ 20. When controlling the sample time for the ADC along with the use of Prescaler or Current Monitor or Temperature Monitor, the minimum sample time for each must be obeyed. Refer to Table 2-45 on page 2-109 and the "Acquisition Time or Sample Time Control" section on page 2-107

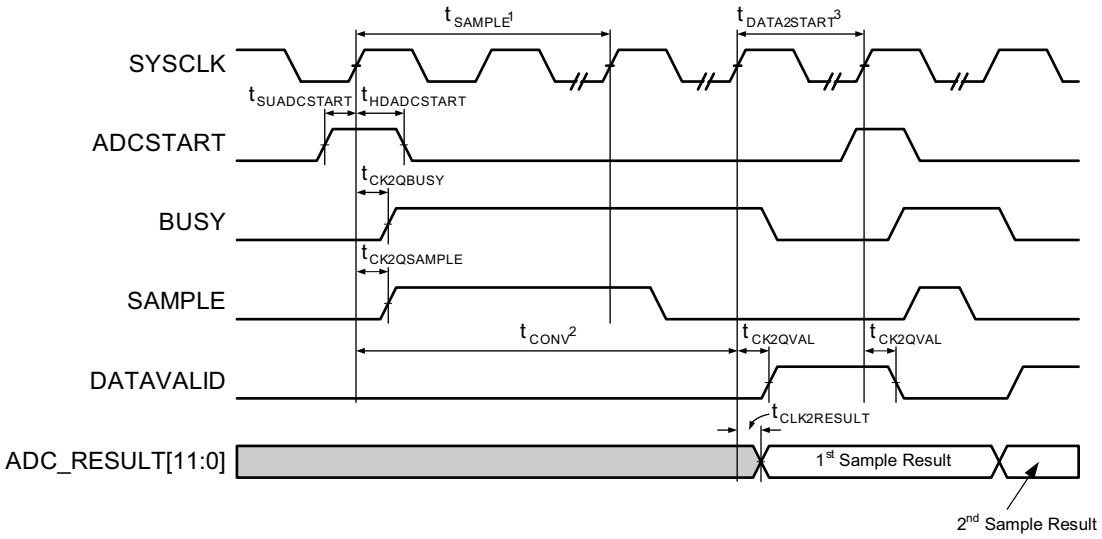
$$t_{sample} = (2 + STC) \times t_{ADCCLK}$$

EQ 20

STC: Sample Time Control value (0–255)

t_{SAMPLE} is the sample time

Standard Conversion

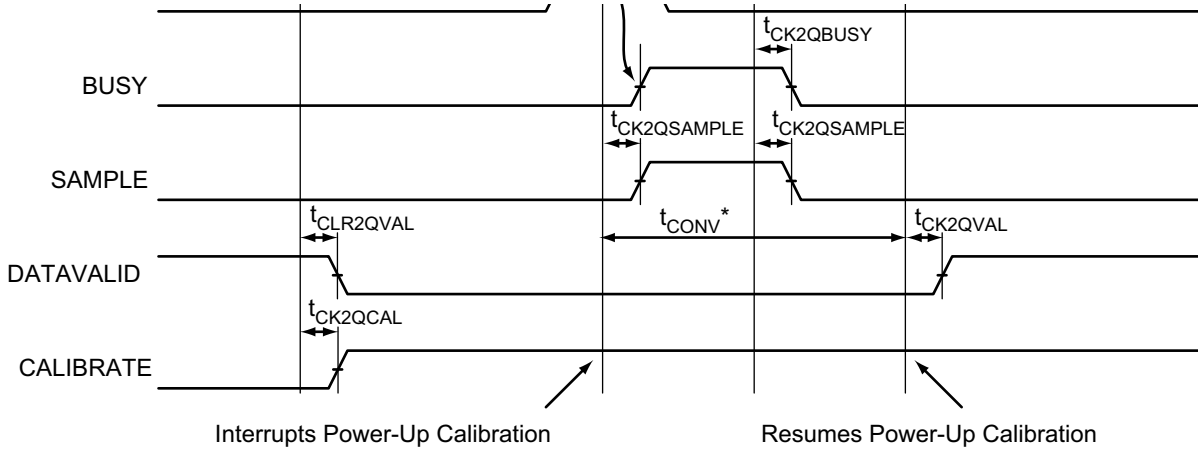


Notes:

1. *Refer to EQ 20 on page 2-108 for the calculation on the sample time, t_{SAMPLE}.*
2. *See EQ 23 on page 2-109 for calculation on the conversion time, t_{CONV}.*
3. *Minimum time to issue an ADCSTART after DATAVALID is 1 SYSCLK period*

Figure 2-90 • **Standard Conversion Status Signal Timing Diagram**

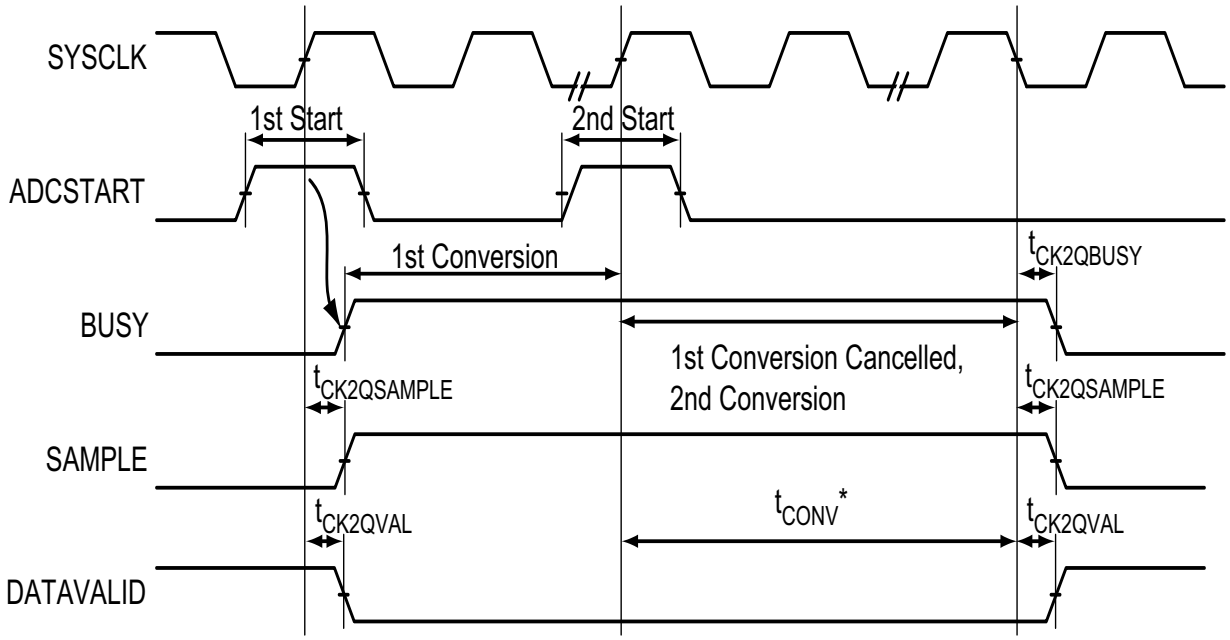
Intra-Conversion



*Note: *t_{CONV} represents the conversion time of the second conversion. See EQ 23 on page 2-109 for calculation of the conversion time, t_{CONV}.*

Figure 2-91 • **Intra-Conversion Timing Diagram**

Injected Conversion



*Note: * See EQ 23 on page 2-109 for calculation on the conversion time, t_{CONV}.*

Figure 2-92 • **Injected-Conversion Timing Diagram**

Table 2-52 • Calibrated Analog Channel Accuracy [1,2,3]
Worst-Case Extended Temperature Conditions, T_J = 100°C

		Condition	Total Channel Error (LSB)		
Analog Pad	**Prescaler Range (V)**	**Input Voltage[4] (V)**	**Negative Max.**	**Median**	**Positive Max.**
Positive Range			**ADC in 10-Bit Mode**		
AV, AC	16	0.300 to 12.0	–6	1	6
	8	0.250 to 8.00	–6	0	6
	4	0.200 to 4.00	–7	–1	7
	2	0.150 to 2.00	–7	0	7
	1	0.050 to 1.00	–6	–1	6
AT	16	0.300 to 16.0	–5	0	5
	4	0.100 to 4.00	–7	–1	7
Negative Range			**ADC in 10-Bit Mode**		
AV, AC	16	–0.400 to –10.5	–7	1	9
	8	–0.350 to –8.00	–7	–1	7
	4	–0.300 to –4.00	–7	–2	9
	2	–0.250 to –2.00	–7	–2	7
	1	–0.050 to –1.00	–16	–1	20

Notes:

1. *Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Overall accuracy remains the same.*
2. *Requires enabling Analog Calibration using SmartGen Analog System Builder. For further details, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User's Guide.
3. *Calibrated with two-point calibration methodology, using 20% and 80% full-scale points.*
4. *The lower limit of the input voltage is determined by the prescaler input offset.*

For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.

Table 2-66 • **Internal Temperature Monitor Control Truth Table**

Control Lines B2[0]	PDTMB	Chip Internal Temperature Monitor
0	0	Off
1	1	On

User I/O Characteristics

Timing Model

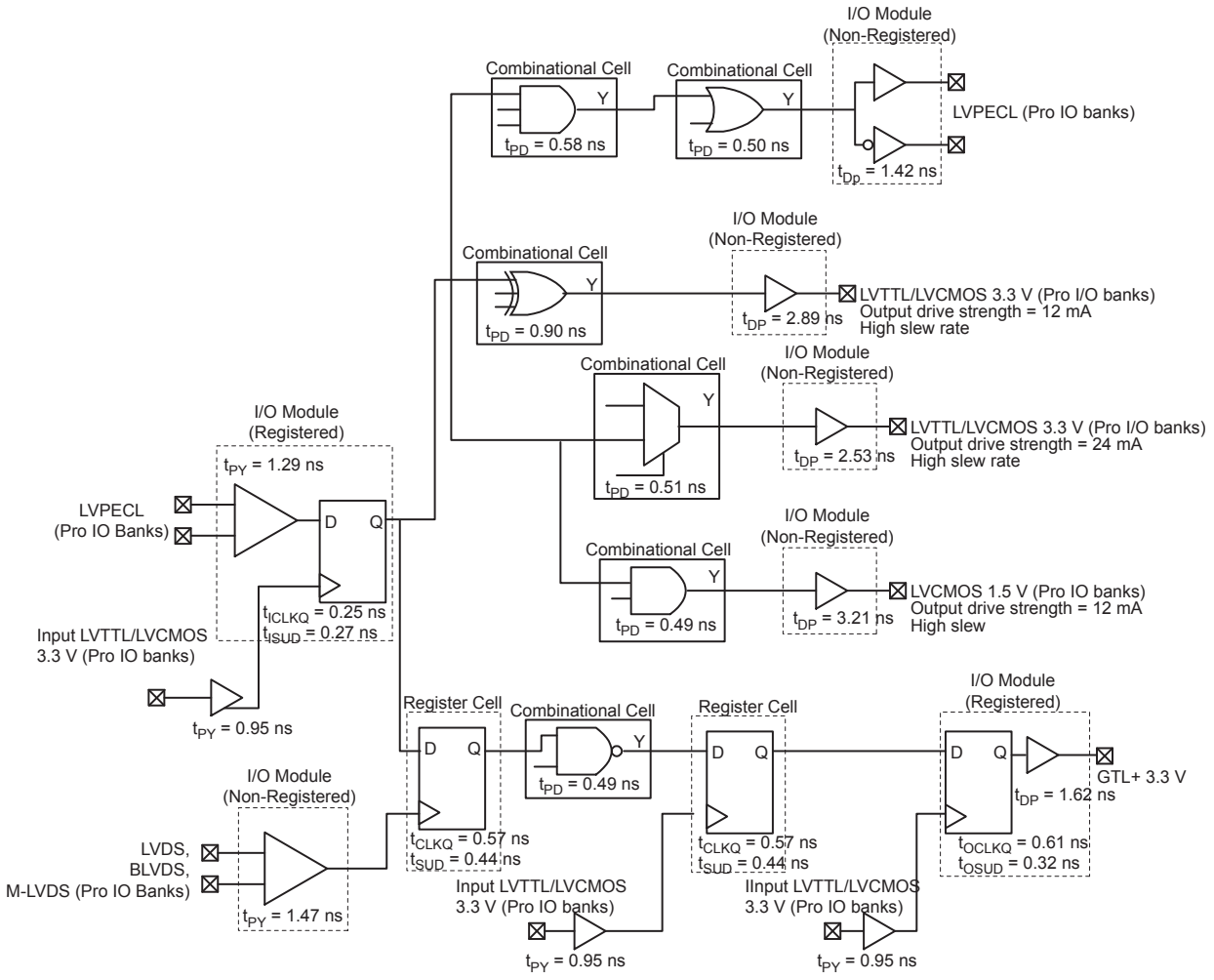


Figure 2-113 • **Timing Model**
Operating Conditions: –2 Speed, Extended Temperature Range (T_J = 100°C),
Worst-Case VCC = 1.425 V

Table 2-91 • Summary of I/O Timing Characteristics – Software Default Settings, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI as Per Configuration Applicable to Pro I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTL/ 3.3 V LVCMOS	12 mA	High	35	–	0.51	2.89	0.03	0.95	1.23	0.33	2.94	2.26	2.58	2.85	4.70	4.02	ns
2.5 V LVCMOS	12 mA	High	35	–	0.51	2.95	0.03	1.19	1.31	0.33	3.00	2.75	2.65	2.75	4.76	4.51	ns
1.8 V LVCMOS	12 mA	High	35	–	0.51	2.99	0.03	1.14	1.50	0.33	2.83	2.40	2.91	3.21	4.60	4.16	ns
1.5 V LVCMOS	12 mA	High	35	–	0.51	3.21	0.03	1.13	1.69	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns
3.3 V PCI	Per PCI spec	High	10	25 [2]	0.51	2.21	0.03	0.83	1.32	0.33	2.25	1.57	2.58	2.85	4.01	3.33	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 [2]	0.51	2.21	0.03	0.81	1.24	0.33	2.25	1.57	2.58	2.85	4.01	3.33	ns
3.3 V GTL	20 mA	High	10	25	0.51	1.63	0.03	2.31	–	0.33	1.60	1.63			3.36	3.40	ns
2.5 V GTL	20 mA	High	10	25	0.51	1.68	0.03	1.93	–	0.33	1.70	1.68			3.46	3.44	ns
3.3 V GTL+	35 mA	High	10	25	0.51	1.62	0.03	1.25	–	0.33	1.65	1.62			3.41	3.38	ns
2.5 V GTL+	33mA	High	10	25	0.51	1.74	0.03	1.19	–	0.33	1.77	1.65			3.53	3.41	ns
HSTL (I)	8 mA	High	20	50	0.51	2.50	0.03	1.67	–	0.33	2.55	2.48			4.31	4.24	ns
HSTL (II)	15 mA	High	20	25	0.51	2.38	0.03	1.67	–	0.33	2.43	2.14			4.19	3.90	ns
SSTL2 (I)	17 mA	High	30	50	0.51	1.68	0.03	1.05	–	0.33	1.71	1.45			3.47	3.22	ns
SSTL2 (II)	21 mA	High	30	25	0.51	1.71	0.03	1.05	–	0.33	1.74	1.39			3.50	3.15	ns
SSTL3 (I)	16 mA	High	30	50	0.51	1.82	0.03	0.99	–	0.33	1.85	1.45			3.61	3.21	ns
SSTL3 (II)	24 mA	High	30	25	0.51	1.63	0.03	0.99	–	0.33	1.66	1.32			3.42	3.08	ns
LVDS	24 mA	High	–	–	0.51	1.48	0.03	1.47	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.51	1.42	0.03	1.29	–	–	–	–	–	–	–	–	ns

Notes:

1. *For the derating values at specific junction temperature and voltage-supply levels, refer to Table 3-7 on page 3-10.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-100 on page 2-140 for connectivity. This resistor is not required during normal operation.*

Timing Characteristics

Table 2-102 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	11.61	0.05	1.27	1.65	0.44	11.82	9.55	2.84	2.58	14.18	11.90	ns
	–1	0.58	9.87	0.04	1.08	1.40	0.38	10.06	8.12	2.41	2.19	12.06	10.13	ns
	–2	0.51	8.67	0.03	0.95	1.23	0.33	8.83	7.13	2.12	1.92	10.59	8.89	ns
8 mA	Std.	0.68	8.29	0.05	1.27	1.65	0.44	8.45	6.79	3.20	3.23	10.80	9.15	ns
	–1	0.58	7.05	0.04	1.08	1.40	0.38	7.18	5.78	2.72	2.75	9.19	7.78	ns
	–2	0.51	6.19	0.03	0.95	1.23	0.33	6.31	5.07	2.39	2.41	8.07	6.83	ns
12 mA	Std.	0.68	6.35	0.05	1.27	1.65	0.44	6.47	5.29	3.45	3.66	8.83	7.65	ns
	–1	0.58	5.41	0.04	1.08	1.40	0.38	5.51	4.50	2.94	3.11	7.51	6.51	ns
	–2	0.51	4.75	0.03	0.95	1.23	0.33	4.83	3.95	2.58	2.73	6.59	5.71	ns
16 mA	Std.	0.68	5.93	0.05	1.27	1.65	0.44	6.04	4.98	3.50	3.77	8.39	7.34	ns
	–1	0.58	5.04	0.04	1.08	1.40	0.38	5.13	4.24	2.98	3.21	7.14	6.24	ns
	–2	0.51	4.42	0.03	0.95	1.23	0.33	4.51	3.72	2.62	2.82	6.27	5.48	ns
24 mA	Std.	0.68	5.53	0.05	1.27	1.65	0.44	5.63	4.95	3.57	4.18	7.99	7.31	ns
	–1	0.58	4.70	0.04	1.08	1.40	0.38	4.79	4.21	3.04	3.55	6.80	6.22	ns
	–2	0.51	4.13	0.03	0.95	1.23	0.33	4.21	3.70	2.67	3.12	5.97	5.46	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Voltage Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-127 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[4]	IIH[5]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
20 mA[3]	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20	181	268	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*
4. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL*
5. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

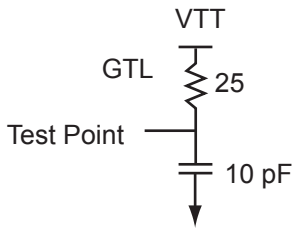


Figure 2-122 • AC Loading

Table 2-128 • 3.3 V GTL AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

*Note: *Measuring point* = Vtrip. *See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

Table 2-129 • 3.3 V GTL
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 3.0 V, VREF = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.19	0.05	3.09	0.44	2.15	2.19			4.51	4.55	ns
–1	0.58	1.86	0.04	2.63	0.38	1.83	1.86			3.83	3.87	ns
–2	0.51	1.63	0.03	2.31	0.33	1.60	1.63			3.36	3.40	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-133 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL+	VIL		VIH		V_{OL}	VOH	IOL	IOH	IOSL	IOSH	IIL[3]	IIH[4]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[2]	µA[2]
35 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35	181	268	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

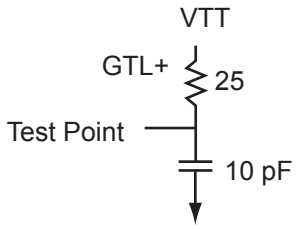


Figure 2-124 • AC Loading

Table 2-134 • 3.3 V GTL+ AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = V_{trip}. See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

Table 2-135 • 3.3 V GTL+
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 3.0 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.17	0.05	1.68	0.44	2.21	2.17			4.57	4.53	ns
–1	0.58	1.84	0.04	1.43	0.38	1.88	1.84			3.88	3.85	ns
–2	0.51	1.62	0.03	1.25	0.33	1.65	1.62			3.41	3.38	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

3 – DC and Power Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in Table 3-2 on page 3-3.

Table 3-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limit	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage [1]	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
VCC33A	+3.3 V power supply	–0.3 to 3.75 [2]	V
VCC33PMP	+3.3 V power supply	–0.3 to 3.75 [2]	V
VAREF	Voltage reference for ADC	–0.3 to 3.75	V
VCC15A	Digital power supply for the analog system	–0.3 to 1.65	V
VCCNVM	Embedded flash power supply	–0.3 to 1.65	V
VCCOSC	Oscillator power supply	–0.3 to 3.75	V

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-5.*
2. *Analog data not valid beyond 3.65 V.*
3. *The high current mode has a maximum power limit of 15 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
4. *For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.*
5. *Negative input is not supported between –40°C and –55°C.*
6. *Positive input is not supported between –40°C and –55°C.*

Table 3-1 • **Absolute Maximum Ratings (continued)**

Symbol	Parameter	Limit	Units
AV	Unpowered, ADC reset asserted or unconfigured	–11.0 to 12.0	V
	Analog input (+16 V to +2 V prescaler range)	–0.4 to 12.0	V
	Analog input (+1 V to +0.125 V prescaler range)	–0.4 to 3.75	V
	Analog input (–16 V to –2 V prescaler range)[5]	–11.0 to 0.4	V
	Analog input (–1 V to –0.125 V prescaler range)[5]	–3.75 to 0.4	V
	Analog input (direct input to ADC)	–0.4 to 3.75	V
	Analog input (positive current monitor)[6]	–0.4 to 12.0	V
	Analog input (negative current monitor)[5]	–11.0 to 0.4	V
	Digital input	–0.4 to 12.0	V
AC	Unpowered, ADC reset asserted or unconfigured	–11.0 to 12.0	V
	Analog input (+16 V to +2 V prescaler range)	–0.4 to 12.0	V
	Analog input (+1 V to +0.125 V prescaler range)	–0.4 to 3.75	V
	Analog input (–16 V to –2 V prescaler range)[5]	–11.0 to 0.4	V
	Analog input (–1 V to –0.125 V prescaler range)[5]	–3.75 to 0.4	V
	Analog input (direct input to ADC)	–0.4 to 3.75	V
	Analog input (positive current monitor)[6]	–0.4 to 12.0	V
	Analog input (negative current monitor)[5]	–11.0 to 0.4	V
	Digital input	–0.4 to 12.0	V
AG	Unpowered, ADC reset asserted or unconfigured	–11.0 to 12.0	V
	Low Current Mode (1 µA, 3 µA, 10 µA, 30 µA)	–0.4 to 12.0	V
	Low Current Mode (–1 µA, –3 µA, –10 µA, –30 µA)	–11.0 to 0.4	V
	High Current Mode [3]	–11.0 to 12.0	V
AT	Unpowered, ADC reset asserted or unconfigured	–0.4 to 15.0	V
	Analog input (+16 V, 4 V prescaler range)	–0.4 to 15.0	V
	Analog input (direct input to ADC)	–0.4 to 3.75	V
	Digital input	–0.4 to 1650	V
T_{STG} [4]	Storage temperature	–65 to 150	°C
T_J [4]	Junction temperature	125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-5.*
2. *Analog data not valid beyond 3.65 V.*
3. *The high current mode has a maximum power limit of 15 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
4. *For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.*
5. *Negative input is not supported between –40°C and –55°C.*
6. *Positive input is not supported between –40°C and –55°C.*

Table 3-3 • **Input Resistance of Analog Pads**

Pads	Pad Configuration	Prescaler Range	Input Resistance to Ground
AV	Analog Input (direct input to ADC)	–	2 kΩ (typical)
		–	> 10 MΩ
	Analog Input (positive prescaler)	+16 V to +2 V	1 MΩ (typical)
		+1 V to +0.125 V	> 10 MΩ
	Analog Input (negative prescaler)	–16 V to –2 V	1 MΩ (typical)
		–1 V to –0.125 V	> 10 MΩ
	Digital input	+16 V to +2 V	1 MΩ (typical)
	Current monitor	+16 V to +2 V	1 MΩ (typical)
		–16 V to –2 V	1 MΩ (typical)
AT	Analog Input (direct input to ADC)	–	1 MΩ (typical)
	Analog Input (positive prescaler)	+16 V, +4 V	1 MΩ (typical)
	Digital input	+16 V, +4 V	1 MΩ (typical)
	Temperature monitor	+16 V, +4 V	> 10 MΩ

Table 3-4 • **Overshoot and Undershoot Limits (as measured on quiet I/Os)[1]**

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3.0 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at a junction temperature of 85°C.*
2. *The duration is allowed at one cycle out of six clock cycle. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*

Table 3-5 • **FPGA Programming, Storage, and Operating Limits**

Product Grade	Storage Temperature	Element	Grade Programming Cycles	Retention
Extended Temperature (K)	Min. T_J = –55°C	FPGA/FlashROM	500	20 years
	Min. T_J = 100°C	Embedded flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years

FG484		
Pin Number	AFS600 Function	AFS1500 Function
B5	IO05NDB0V0	IO04NDB0V0
B6	IO05PDB0V0	IO04PDB0V0
B7	GND	GND
B8	IO10NDB0V1	IO09NDB0V1
B9	IO13PDB0V1	IO11PDB0V1
B10	GND	GND
B11	IO17NDB1V0	IO24NDB1V0
B12	IO18NDB1V0	IO26NDB1V0
B13	GND	GND
B14	IO21NDB1V0	IO31NDB1V1
B15	IO21PDB1V0	IO31PDB1V1
B16	GND	GND
B17	GBC1/IO26PDB1V1	GBC1/IO40PDB1V2
B18	GBA1/IO28PDB1V1	GBA1/IO42PDB1V2
B19	GND	GND
B20	VCCPLB	VCCPLB
B21	GND	GND
B22	VCC	NC
C1	IO82PDB4V0	IO121PDB4V0
C2	NC	IO122PSB4V0
C3	IO00NDB0V0	IO00NDB0V0
C4	IO00PDB0V0	IO00PDB0V0
C5	VCCIB0	VCCIB0
C6	IO06NDB0V0	IO05NDB0V1
C7	IO06PDB0V0	IO05PDB0V1
C8	VCCIB0	VCCIB0
C9	IO13NDB0V1	IO11NDB0V1
C10	IO11PDB0V1	IO14PDB0V2
C11	VCCIB0	VCCIB0
C12	VCCIB1	VCCIB1
C13	IO20NDB1V0	IO29NDB1V1
C14	IO20PDB1V0	IO29PDB1V1
C15	VCCIB1	VCCIB1
C16	IO25NDB1V1	IO37NDB1V2
C17	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2

FG484		
Pin Number	AFS600 Function	AFS1500 Function
C18	VCCIB1	VCCIB1
C19	VCOMPLB	VCOMPLB
C20	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0
C21	NC	IO48PSB2V0
C22	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0
D1	IO82NDB4V0	IO121NDB4V0
D2	GND	GND
D3	IO83NDB4V0	IO123NDB4V0
D4	GAC2/IO83PDB4V0	GAC2/IO123PDB4V0
D5	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0
D6	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0
D7	GAC1/IO03PDB0V0	GAC1/IO03PDB0V0
D8	IO09NDB0V1	IO10NDB0V1
D9	IO09PDB0V1	IO10PDB0V1
D10	IO11NDB0V1	IO14NDB0V2
D11	IO16NDB1V0	IO23NDB1V0
D12	IO16PDB1V0	IO23PDB1V0
D13	NC	IO32NPB1V1
D14	IO23NDB1V1	IO34NDB1V1
D15	IO23PDB1V1	IO34PDB1V1
D16	IO25PDB1V1	IO37PDB1V2
D17	GBB1/IO27PDB1V1	GBB1/IO41PDB1V2
D18	VCCIB2	VCCIB2
D19	NC	IO47PPB2V0
D20	IO30NDB2V0	IO44NDB2V0
D21	GND	GND
D22	IO31NDB2V0	IO45NDB2V0
E1	IO81NDB4V0	IO120NDB4V0
E2	IO81PDB4V0	IO120PDB4V0
E3	VCCIB4	VCCIB4
E4	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0
E5	IO85NDB4V0	IO125NDB4V0
E6	GND	GND
E7	VCCIB0	VCCIB0
E8	NC	IO08NDB0V1