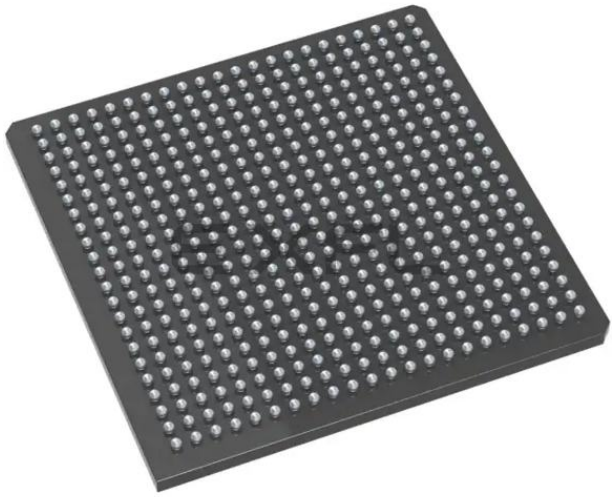


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-1fg484k

Array Coordinates

During many place-and-route operations in the Microsemi Designer software tool, it is possible to set constraints that require array coordinates. Table 2-3 is provided as a reference. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

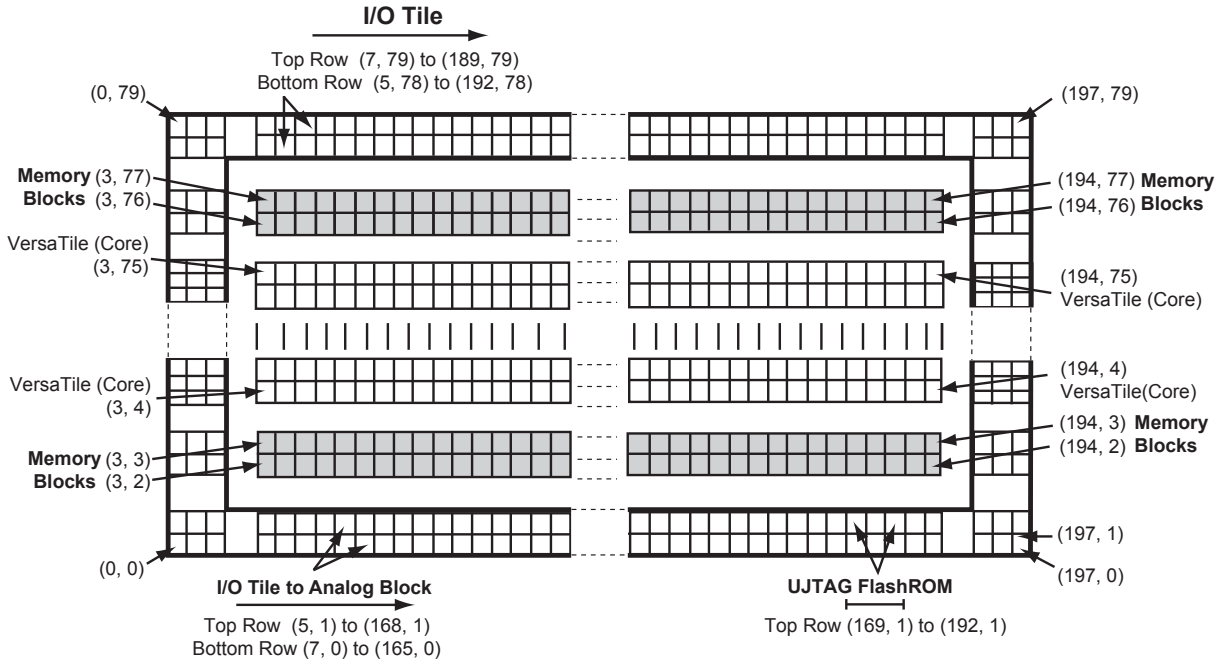
Table 2-3 provides array coordinates of core cells and memory blocks.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and edge core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-3. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-7 illustrates the array coordinates of an AFS600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for Fusion software tools.

Table 2-3 • **Array Coordinates**

Device	VersaTiles				Memory Rows		All	
	Min.		Max.		Bottom	Top	Min.	Max.
	x	y	x	y	(x, y)	(x, y)	(x, y)	(x, y)
AFS600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)
AFS1500	3	4	322	123	(3, 2)	(3, 124)	(0, 0)	(325, 129)



Note: The vertical I/O tile coordinates are not shown. West side coordinates are {(0, 2) to (2, 2)} to {(0, 77) to (2, 77)}; east side coordinates are {(195, 2) to (197, 2)} to {(195, 77) to (197, 77)}.

Figure 2-7 • **Array Coordinates for AFS600**

Global Resource Characteristics

AFS600 VersaNet Topology

Clock delays are device-specific. Figure 2-15 is an example of a global tree used for clock routing. The global tree presented in Figure 2-15 is driven by a CCC located on the west side of the AFS600 device. It is used to drive all D-flip-flops in the device.

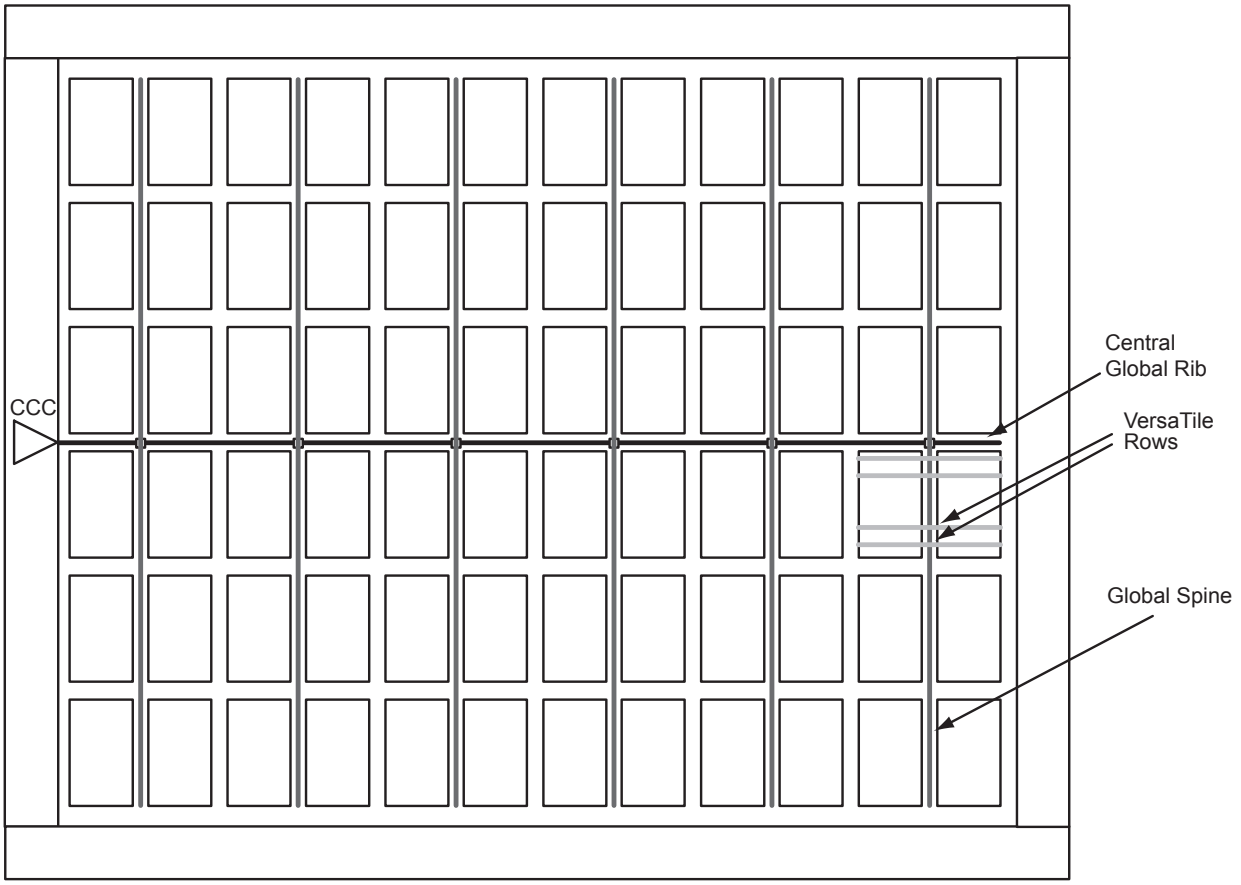


Figure 2-15 • **Example of Global Tree Use in an AFS600 Device for Clock Routing**

Real-Time Counter System

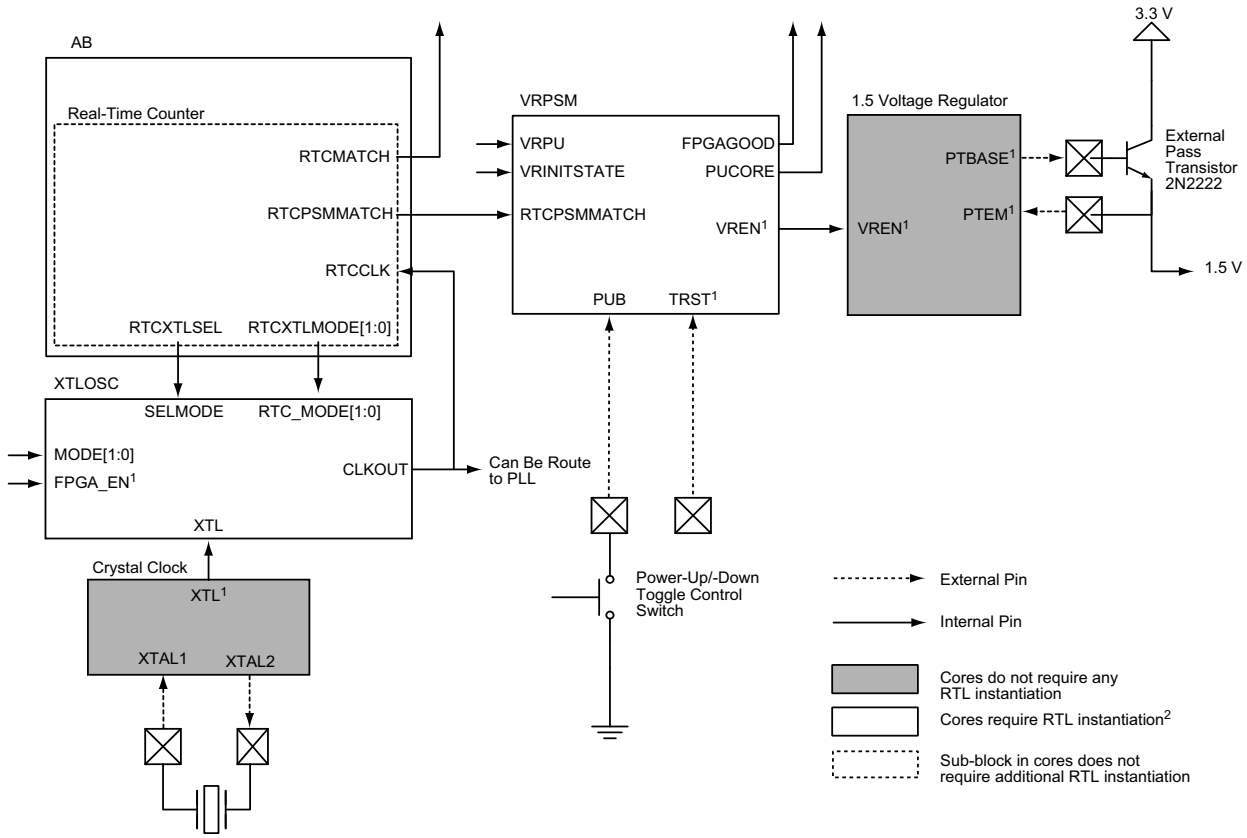
The RTC system enables Fusion devices to support standby and sleep modes of operation to reduce power consumption in many applications.

- Sleep mode, typical 10 µA
- Standby mode (RTC running), typical 3 mA with 20 MHz

The RTC system is composed of five cores:

- RTC sub-block inside Analog Block (AB)
- Voltage Regulator and Power System Monitor (VRPSM)
- Crystal oscillator (XTLOSC); refer to the "Crystal Oscillator" section in the Fusion Clock Resources chapter of the *Fusion FPGA Fabric User's Guide* for more detail.
- Crystal clock; does not require instantiation in RTL
- 1.5 V voltage regulator; does not require instantiation in RTL

All cores are powered by 3.3 V supplies, so the RTC system is operational without a 1.5 V supply during standby mode. Figure 2-27 shows their connection.



Notes:

1. *Signals are hardwired internally and do not exist in the macro core.*
2. *User is only required to instantiate the VRPSM macro if the user wishes to specify PUPO behavior of the voltage regulator to be different from the default, or employ user logic to shut the voltage regulator off.*

Figure 2-27 • **Real-Time Counter System (not all the signals are shown for the AB macro)**

The following error indications are possible for Read operations:

1. STATUS = '01' when a single-bit data error was detected and corrected within the block addressed.
2. STATUS = '10' when a double-bit error was detected in the block addressed (note that the error is uncorrected).

In addition to data reads, users can read the status of any page in the FB by asserting PAGESTATUS along with REN. The format of the data returned by a page status read is shown in Table 2-22, and the definition of the page status bits is shown in Table 2-23.

Table 2-22 • **Page Status Read Data Format**

31	8	7	4	3	2	1	0
Write Count		Reserved		Over Threshold	Read Protected	Write Protected	Overwrite Protected

Table 2-23 • **Page Status Bit Definition**

Page Status Bit(s)	Definition
31–8	The number of times the page addressed has been programmed/erased
7–4	Reserved; read as 0
3	Over Threshold indicator (see the "Program Operation" section on page 2-46)
2	Read Protected; read protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value.
1	Write Protected; write protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value.
0	Overwrite Protected; designates that the user has set the OVERWRITEPROTECT bit on the interface while doing a Program operation. The page cannot be written without first performing an Unprotect Page operation.

Flash Memory Block Characteristics

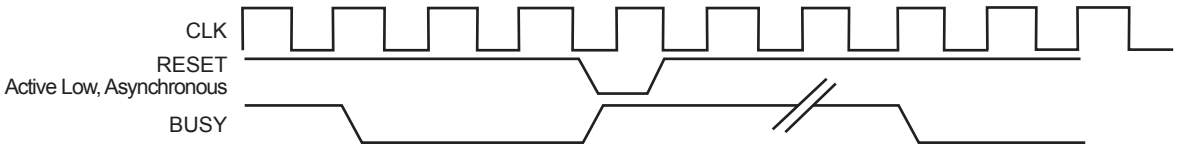


Figure 2-44 • **Reset Timing Diagram**

Table 2-24 • **Flash Memory Block Timing, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V**

Parameter	Description	–2	–1	Std.	Units
t_{CLK2RD}	Clock-to-Q in 5-cycle read mode of the Read Data	8.24	9.39	11.04	ns
	Clock-to-Q in 6-cycle read mode of the Read Data	5.10	5.81	6.83	ns
$t_{CLK2BUSY}$	Clock-to-Q in 5-cycle read mode of BUSY	5.19	5.91	6.95	ns
	Clock-to-Q in 6-cycle read mode of BUSY	4.59	5.23	6.15	ns
$t_{CLK2STATUS}$	Clock-to-Status in 5-cycle read mode	11.59	13.21	15.53	ns
	Clock-to-Status in 6-cycle read mode	4.62	5.26	6.19	ns
t_{DSUNVM}	Data Input Setup time for the Control Logic	1.98	2.26	2.65	ns
t_{DHNVM}	Data Input Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{ASUNVM}	Address Input Setup time for the Control Logic	2.84	3.24	3.81	ns
t_{AHNVM}	Address Input Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUDWNVM}$	Data Width Setup time for the Control Logic	1.91	2.17	2.56	ns
$t_{HDDWNVM}$	Data Width Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SURENNVM}$	Read Enable Setup time for the Control Logic	3.97	4.53	5.32	ns
$t_{HDRENNVM}$	Read Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUWENNVM}$	Write Enable Setup time for the Control Logic	2.44	2.78	3.27	ns
$t_{HDWENNVM}$	Write Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUPROGNVM}$	Program Setup time for the Control Logic	2.23	2.54	2.98	ns
$t_{HDPROGNVM}$	Program Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUSPAREPAGE}$	SparePage Setup time for the Control Logic	3.86	4.40	5.17	ns
$t_{HDSPAREPAGE}$	SparePage Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUAUXBLK}$	Auxiliary Block Setup Time for the Control Logic	3.85	4.39	5.16	ns
$t_{HDAUXBLK}$	Auxiliary Block Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SURDNEXT}$	ReadNext Setup Time for the Control Logic	2.23	2.54	2.99	ns
$t_{HDRDNEXT}$	ReadNext Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUERASEPG}$	Erase Page Setup Time for the Control Logic	3.87	4.41	5.19	ns
$t_{HDERASEPG}$	Erase Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUUNPROTECTPG}$	Unprotect Page Setup Time for the Control Logic	2.07	2.36	2.77	ns
$t_{HDUNPROTECTPG}$	Unprotect Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUDISCARDPG}$	Discard Page Setup Time for the Control Logic	1.94	2.21	2.60	ns
$t_{HDDISCARDPG}$	Discard Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUOVERWRPRO}$	Overwrite Protect Setup Time for the Control Logic	1.69	1.92	2.26	ns
$t_{HDOVERWRPRO}$	Overwrite Protect Hold Time for the Control Logic	0.00	0.00	0.00	ns

Timing Characteristics

Table 2-30 • RAM4K9, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.26	0.29	0.34	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.15	0.17	0.20	ns
t_{ENH}	REN, WEN hold time	0.10	0.11	0.13	ns
t_{BKS}	BLK setup time	0.24	0.27	0.32	ns
t_{BKH}	BLK hold time	0.02	0.02	0.03	ns
t_{DS}	Input data (DIN) setup time	0.19	0.22	0.25	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.84	2.10	2.47	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.43	2.77	3.25	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.92	1.05	1.23	ns
t_{C2CWWH} [1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.23	0.26	0.30	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.34	0.38	0.45	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.37	0.42	0.49	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	0.95	1.08	1.27	ns
	RESET Low to Data Out Low on DOUT (pipelined)	0.95	1.08	1.27	ns
$t_{REMRSTB}$	RESET removal	0.29	0.34	0.39	ns
$t_{RECRSTB}$	RESET recovery	1.55	1.76	2.07	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.22	0.25	0.29	ns
t_{CYC}	Clock cycle time	3.33	3.79	4.46	ns
FMAX	Maximum frequency	300	264	224	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.*

Voltage Monitor

The Fusion Analog Quad offers a robust set of voltage-monitoring capabilities unique in the FPGA industry. The Analog Quad comprises three analog input pads—Analog Voltage (AV), Analog Current (AC), and Analog Temperature (AT)—and a single gate driver output pad, Analog Gate (AG). There are many common characteristics among the analog input pads. Each analog input can be configured to connect directly to the input MUX of the ADC. When configured in this manner (Figure 2-65), there will be no prescaling of the input signal. Care must be taken in this mode not to drive the ADC into saturation by applying an input voltage greater than the reference voltage. The internal reference voltage of the ADC is 2.56 V. Optionally, an external reference can be supplied by the user. The external reference can be a maximum of 3.3 V DC.

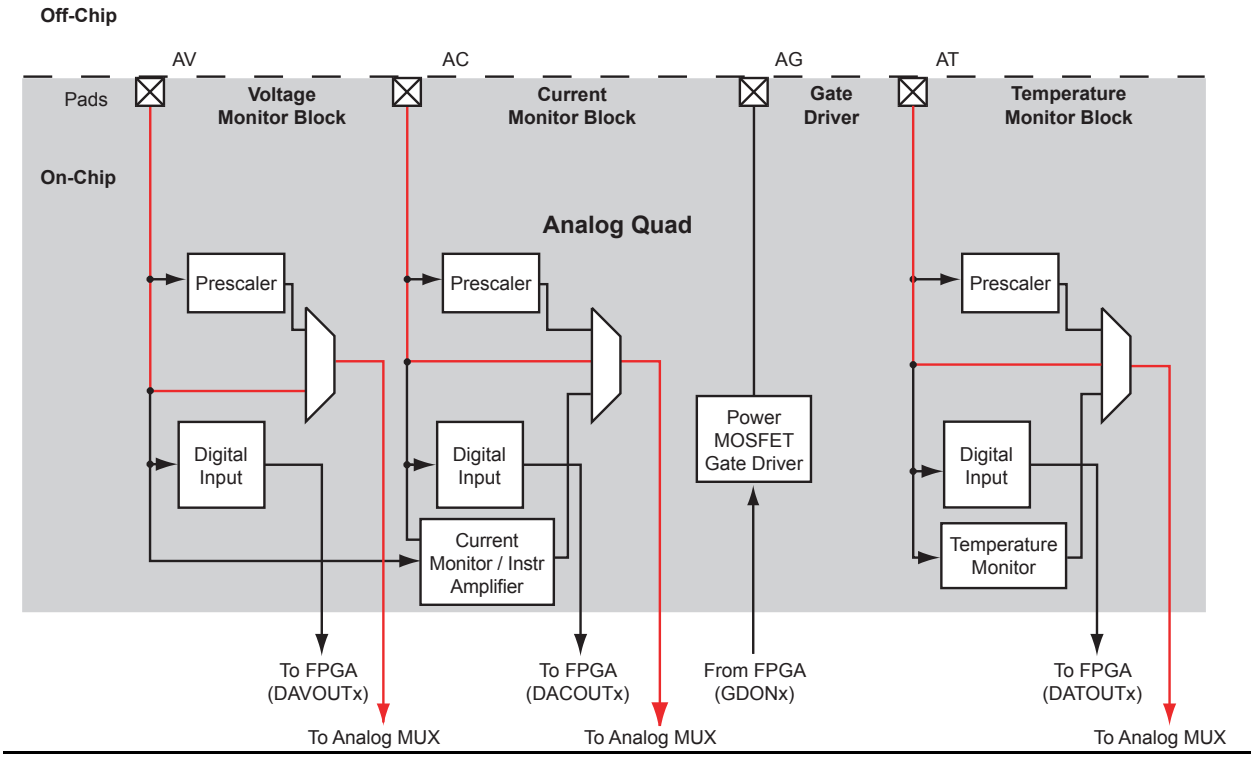


Figure 2-65 • **Analog Quad Direct Connect**

The Analog Quad offers a wide variety of prescaling options to enable the ADC to resolve the input signals. Figure 2-66 shows the path through the Analog Quad for a signal that is to be prescaled prior to conversion. The ADC internal reference voltage and the prescaler factors were selected to make both prescaling and postscaling of the signals easy binary calculations (refer to Table 2-57 on page 2-130 for details). When an analog input pad is configured with a prescaler, there will be a 1 MΩ resistor to ground. This occurs even when the device is in power-down mode. In low power standby or sleep mode (VCC is OFF, VCC33A is ON, VCCI is ON) or when the resource is not used, analog inputs are pulled down to ground through a 1 MΩ resistor. The gate driver output is floating (or tristated), and there is no extra current on VCC33A.

These scaling factors hold true whether the particular pad is configured to accept a positive or negative voltage. Note that whereas the AV and AC pads support the same prescaling factors, the AT pad supports a reduced set of prescaling factors and supports positive voltages only.

Typical scaling factors are given in Table 2-57 on page 2-130, and the gain error (which contributes to the minimum and maximum) is in Table 2-49 on page 2-117.

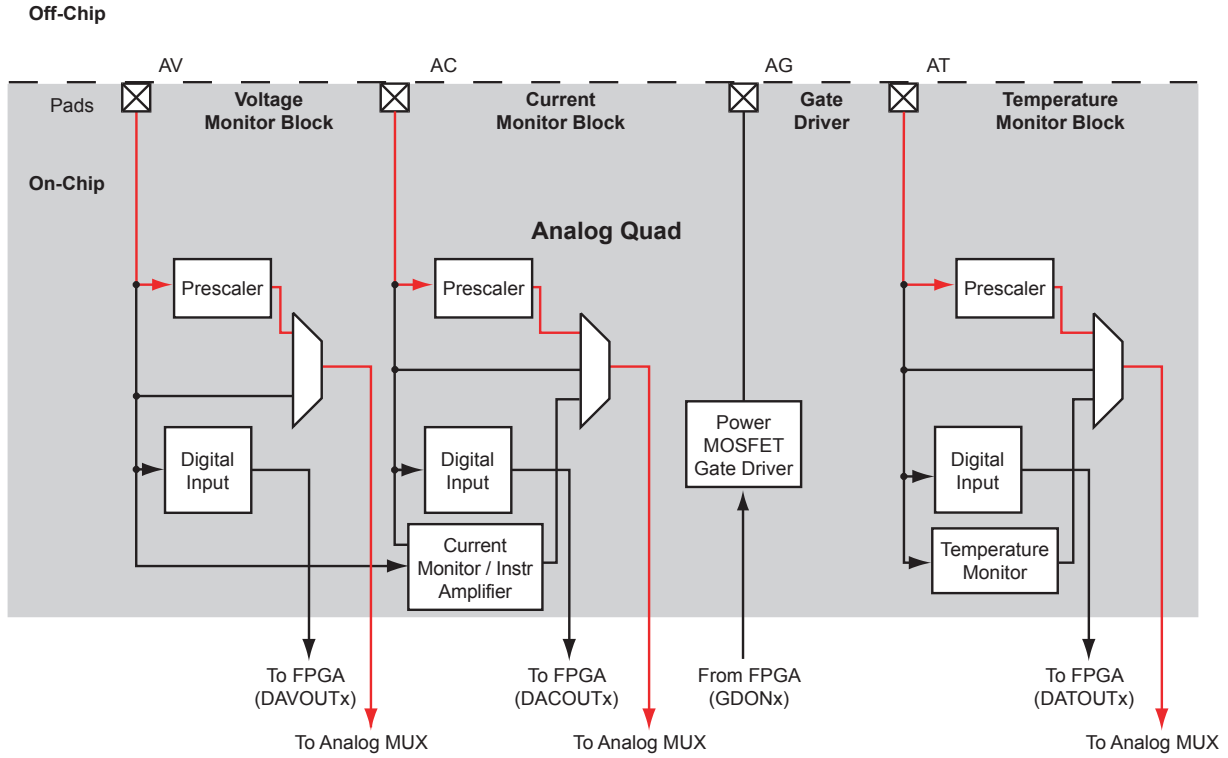


Figure 2-66 • **Analog Quad Prescaler Input Configuration**

For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.

Table 2-66 • **Internal Temperature Monitor Control Truth Table**

Control Lines B2[0]	PDTMB	Chip Internal Temperature Monitor
0	0	Off
1	1	On

For Fusion devices requiring Level 3 and/or Level 4 compliance, the board drivers connected to Fusion I/Os need to have 10 kΩ (or lower) output drive resistance at hot insertion, and 1 kΩ (or lower) output drive resistance at hot removal. This is the resistance of the transmitter sending a signal to the Fusion I/O, and no additional resistance is needed on the board. If that cannot be assured, three levels of staging can be used to meet Level 3 and/or Level 4 compliance. Cards with two levels of staging should have the following sequence:

1. Grounds
2. Powers, I/Os, other pins

Cold-Sparing Support

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

Pro I/O banks fully support cold-sparing.

For Pro I/O banks, standards such as PCI that require I/O clamp diodes, can also achieve cold-sparing compliance, since clamp diodes get disconnected internally when the supplies are at 0 V.

For Advanced I/O banks, since the I/O clamp diode is always active, cold-sparing can be accomplished either by employing a bus switch to isolate the device I/Os from the rest of the system or by driving each advanced I/O pin to 0 V.

If a resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitor is in parallel with the resistor). The RC time constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins are discharged to ground every time there is an interruption of power to the device.

I/O cold-sparing may add additional current if the pin is configured with either a pull-up or pull-down resistor and driven in the opposite direction. A small static current is induced on each I/O pin when the pin is driven to a voltage opposite to the weak pull resistor. The current is equal to the voltage drop across the input pin divided by the pull resistor. Refer to Table 2-93 on page 2-169, Table 2-94 on page 2-169, and Table 2-95 on page 2-171 for the specific pull resistor value for the corresponding I/O standard.

For example, assuming an LVTTL 3.3 V input pin is configured with a weak Pull-up resistor, a current will flow through the pull-up resistor if the input pin is driven low. For an LVTTL 3.3 V, pull-up resistor is ~45 kΩ and the resulting current is equal to 3.3 V / 45 kΩ = 73 µA for the I/O pin. This is true also when a weak pull-down is chosen and the input pin is driven high. Avoiding this current can be done by driving the input low when a weak pull-down resistor is used, and driving it high when a weak pull-up resistor is used.

In Active and Static modes, this current draw can occur in the following cases:

- Input buffers with pull-up, driven Low
- Input buffers with pull-down, driven High
- Bidirectional buffers with pull-up, driven Low
- Bidirectional buffers with pull-down, driven High
- Output buffers with pull-up, driven Low
- Output buffers with pull-down, driven High
- Tristate buffers with pull-up, driven Low
- Tristate buffers with pull-down, driven High

Electrostatic Discharge (ESD) Protection

Fusion devices are tested per JEDEC Standard JESD22-A114-B.

Fusion devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

Detailed I/O DC Characteristics

Table 2-93 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
CIN	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
CINCLK	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-94 • I/O Output Buffer Maximum Resistances [1]

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (ohms) [2]	$R_{PULL\text{-}UP}$ (ohms) [3]
Applicable to Pro I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	20 mA	11	–
2.5 V GTL	20 mA	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: www.microsemi.com/soc/techdocs/models/ibis.html.*
2. *R(PULL-DOWN-MAX) = VOLspec / IOLspec*
3. *R(PULL-UP-MAX) = (VCCImax – VOHspec) / IOHspec*

Timing Characteristics

Table 2-107 • 2.5 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	12.66	0.05	1.59	1.75	0.44	12.89	12.24	2.87	2.32	15.25	14.60	ns
	–1	0.58	10.77	0.04	1.36	1.49	0.38	10.97	10.42	2.44	1.97	12.97	12.42	ns
	–2	0.51	9.45	0.03	1.19	1.31	0.33	9.63	9.14	2.14	1.73	11.39	10.90	ns
8 mA	Std.	0.68	9.21	0.05	1.59	1.75	0.44	9.38	8.45	3.27	3.09	11.74	10.81	ns
	–1	0.58	7.83	0.04	1.36	1.49	0.38	7.98	7.19	2.78	2.63	9.98	9.19	ns
	–2	0.51	6.88	0.03	1.19	1.31	0.33	7.00	6.31	2.44	2.31	8.76	8.07	ns
12 mA	Std.	0.68	7.14	0.05	1.59	1.75	0.44	7.28	6.44	3.55	3.58	9.63	8.80	ns
	–1	0.58	6.08	0.04	1.36	1.49	0.38	6.19	5.48	3.02	3.04	8.20	7.48	ns
	–2	0.51	5.33	0.03	1.19	1.31	0.33	5.43	4.81	2.65	2.67	7.19	6.57	ns
16 mA	Std.	0.68	6.65	0.05	1.59	1.75	0.44	6.77	6.04	3.61	3.71	9.13	8.40	ns
	–1	0.58	5.66	0.04	1.36	1.49	0.38	5.76	5.14	3.07	3.16	7.77	7.14	ns
	–2	0.51	4.97	0.03	1.19	1.31	0.33	5.06	4.51	2.69	2.77	6.82	6.27	ns
24 mA	Std.	0.68	6.25	0.05	1.59	1.75	0.44	6.37	6.02	3.69	4.22	8.73	8.37	ns
	–1	0.58	5.32	0.04	1.36	1.49	0.38	5.42	5.12	3.14	3.59	7.43	7.12	ns
	–2	0.51	4.67	0.03	1.19	1.31	0.33	4.76	4.49	2.75	3.15	6.52	6.25	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-136 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
33 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33	124	169	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

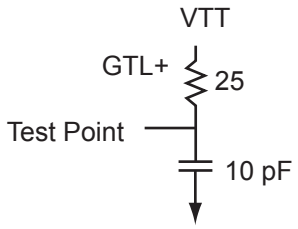


Figure 2-125 • AC Loading

Table 2-137 • 2.5 V GTL+ AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

Table 2-138 • 2.5 V GTL+
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.33	0.05	1.60	0.44	2.37	2.21			4.73	4.57	ns
–1	0.58	1.98	0.04	1.36	0.38	2.02	1.88			4.02	3.89	ns
–2	0.51	1.74	0.03	1.19	0.33	1.77	1.65			3.53	3.41	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-142 • Minimum and Maximum DC Input and Output Levels

HSTL Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max mA[3]	µA[4]	µA[4]
15 mA[3]	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15	55	66	15	15

Note:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Output drive strength is below JEDEC specification.*

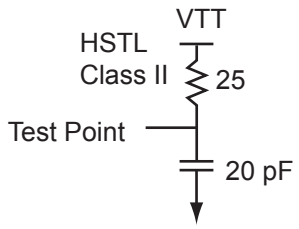


Figure 2-127 • AC Loading

Table 2-143 • HSTL Class II AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

*Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

Table 2-144 • HSTL Class II
Extended Temperature Range Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	3.19	0.05	2.24	0.44	3.25	2.86			5.61	5.22	ns
–1	0.58	2.71	0.04	1.91	0.38	2.76	2.43			4.77	4.44	ns
–2	0.51	2.38	0.03	1.67	0.33	2.43	2.14			4.19	3.90	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-161 • LVPECL Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-162 • LVPECL AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)
1.64	1.94	Cross point	–
*Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.*			

Timing Characteristics

Table 2-163 • LVPECL
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.68	1.90	0.05	1.72	ns
–1	0.58	1.61	0.04	1.47	ns
–2	0.51	1.42	0.03	1.29	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-164 • LVPECL
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.68	1.90	0.05	1.48	ns
–1	0.58	1.61	0.04	1.26	ns
–2	0.51	1.42	0.03	1.11	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

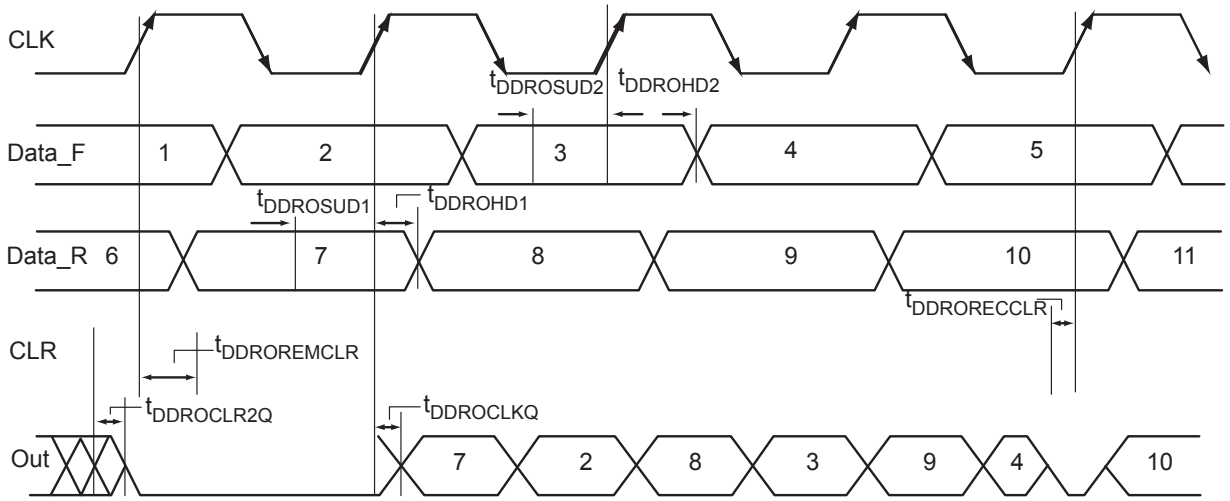


***Figure 2-143* • Output DDR Timing Diagram**

Timing Characteristics

***Table 2-173* • Output DDR Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.72	0.82	0.97	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.39	0.44	0.52	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.39	0.43	0.52	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.83	0.94	1.11	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	0.26	0.31	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.36	0.41	0.48	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.37	0.43	ns
FDDOMAX	Maximum Frequency for the Output DDR	1,404	1,232	1,048	MHz

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

3 – DC and Power Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in Table 3-2 on page 3-3.

Table 3-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limit	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage [1]	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
VCC33A	+3.3 V power supply	–0.3 to 3.75 [2]	V
VCC33PMP	+3.3 V power supply	–0.3 to 3.75 [2]	V
VAREF	Voltage reference for ADC	–0.3 to 3.75	V
VCC15A	Digital power supply for the analog system	–0.3 to 1.65	V
VCCNVM	Embedded flash power supply	–0.3 to 1.65	V
VCCOSC	Oscillator power supply	–0.3 to 3.75	V

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-5.*
2. *Analog data not valid beyond 3.65 V.*
3. *The high current mode has a maximum power limit of 15 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
4. *For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.*
5. *Negative input is not supported between –40°C and –55°C.*
6. *Positive input is not supported between –40°C and –55°C.*

Table 3-1 • **Absolute Maximum Ratings (continued)**

Symbol	Parameter	Limit	Units
AV	Unpowered, ADC reset asserted or unconfigured	–11.0 to 12.0	V
	Analog input (+16 V to +2 V prescaler range)	–0.4 to 12.0	V
	Analog input (+1 V to +0.125 V prescaler range)	–0.4 to 3.75	V
	Analog input (–16 V to –2 V prescaler range)[5]	–11.0 to 0.4	V
	Analog input (–1 V to –0.125 V prescaler range)[5]	–3.75 to 0.4	V
	Analog input (direct input to ADC)	–0.4 to 3.75	V
	Analog input (positive current monitor)[6]	–0.4 to 12.0	V
	Analog input (negative current monitor)[5]	–11.0 to 0.4	V
	Digital input	–0.4 to 12.0	V
AC	Unpowered, ADC reset asserted or unconfigured	–11.0 to 12.0	V
	Analog input (+16 V to +2 V prescaler range)	–0.4 to 12.0	V
	Analog input (+1 V to +0.125 V prescaler range)	–0.4 to 3.75	V
	Analog input (–16 V to –2 V prescaler range)[5]	–11.0 to 0.4	V
	Analog input (–1 V to –0.125 V prescaler range)[5]	–3.75 to 0.4	V
	Analog input (direct input to ADC)	–0.4 to 3.75	V
	Analog input (positive current monitor)[6]	–0.4 to 12.0	V
	Analog input (negative current monitor)[5]	–11.0 to 0.4	V
	Digital input	–0.4 to 12.0	V
AG	Unpowered, ADC reset asserted or unconfigured	–11.0 to 12.0	V
	Low Current Mode (1 µA, 3 µA, 10 µA, 30 µA)	–0.4 to 12.0	V
	Low Current Mode (–1 µA, –3 µA, –10 µA, –30 µA)	–11.0 to 0.4	V
	High Current Mode [3]	–11.0 to 12.0	V
AT	Unpowered, ADC reset asserted or unconfigured	–0.4 to 15.0	V
	Analog input (+16 V, 4 V prescaler range)	–0.4 to 15.0	V
	Analog input (direct input to ADC)	–0.4 to 3.75	V
	Digital input	–0.4 to 1650	V
T_{STG} [4]	Storage temperature	–65 to 150	°C
T_J [4]	Junction temperature	125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-5.*
2. *Analog data not valid beyond 3.65 V.*
3. *The high current mode has a maximum power limit of 15 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
4. *For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.*
5. *Negative input is not supported between –40°C and –55°C.*
6. *Positive input is not supported between –40°C and –55°C.*

FG256		
Pin Number	AFS600 Function	AFS1500 Function
A1	GND	GND
A2	VCCIB0	VCCIB0
A3	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
A4	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0
A5	GND	GND
A6	IO10PDB0V1	IO07PDB0V1
A7	IO12PDB0V1	IO13PDB0V2
A8	IO12NDB0V1	IO13NDB0V2
A9	IO22NDB1V0	IO24NDB1V0
A10	IO22PDB1V0	IO24PDB1V0
A11	IO24NDB1V1	IO29NDB1V1
A12	GND	GND
A13	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2
A14	IO29NDB1V1	IO43NDB1V2
A15	VCCIB1	VCCIB1
A16	GND	GND
B1	V_{COMPLA}	VCOMPLA
B2	VCCPLA	VCCPLA
B3	IO00NDB0V0	IO00NDB0V0
B4	IO00PDB0V0	IO00PDB0V0
B5	GAB1/IO02PPB0V0	GAB1/IO02PPB0V0
B6	IO10NDB0V1	IO07NDB0V1
B7	VCCIB0	VCCIB0
B8	IO18NDB1V0	IO22NDB1V0
B9	IO18PDB1V0	IO22PDB1V0
B10	VCCIB1	VCCIB1
B11	IO24PDB1V1	IO29PDB1V1
B12	GBC0/IO26NPB1V1	GBC0/IO40NPB1V2
B13	GBA1/IO28PDB1V1	GBA1/IO42PDB1V2
B14	IO29PDB1V1	IO43PDB1V2
B15	VCCPLB	VCCPLB
B16	VCOMPLB	VCOMPLB
C1	VCCIB4	VCCIB4
C2	GND	GND
C3	VCCIB4	VCCIB4
C4	VCCIB0	VCCIB0
C5	VCCIB0	VCCIB0

FG256		
Pin Number	AFS600 Function	AFS1500 Function
C6	GAC1/IO03PDB0V0	GAC1/IO03PDB0V0
C7	IO06NDB0V0	IO09NDB0V1
C8	IO16PDB1V0	IO23PDB1V0
C9	IO16NDB1V0	IO23NDB1V0
C10	IO25NDB1V1	IO31NDB1V1
C11	IO25PDB1V1	IO31PDB1V1
C12	VCCIB1	VCCIB1
C13	GBC1/IO26PPB1V1	GBC1/IO40PPB1V2
C14	VCCIB2	VCCIB2
C15	GND	GND
C16	VCCIB2	VCCIB2
D1	IO84NDB4V0	IO124NDB4V0
D2	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0
D3	IO85NDB4V0	IO125NDB4V0
D4	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0
D5	GAB0/IO02NPB0V0	GAB0/IO02NPB0V0
D6	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0
D7	IO06PDB0V0	IO09PDB0V1
D8	IO14NDB0V1	IO15NDB0V2
D9	IO14PDB0V1	IO15PDB0V2
D10	IO23PDB1V1	IO37PDB1V2
D11	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2
D12	VCCIB1	VCCIB1
D13	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0
D14	IO30NDB2V0	IO44NDB2V0
D15	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0
D16	IO31NDB2V0	IO45NDB2V0
E1	GND	GND
E2	IO81NDB4V0	IO118NDB4V0
E3	IO81PDB4V0	IO118PDB4V0
E4	VCCIB4	VCCIB4
E5	IO83NPB4V0	IO123NPB4V0
E6	IO04NPB0V0	IO05NPB0V1
E7	GND	GND
E8	IO08PDB0V1	IO11PDB0V1
E9	IO20NDB1V0	IO27NDB1V1
E10	GND	GND

FG484		
Pin Number	AFS600 Function	AFS1500 Function
V3	VCCIB4	VCCIB4
V4	GEA1/IO61PDB4V0	GEA1/IO88PDB4V0
V5	GEA0/IO61NDB4V0	GEA0/IO88NDB4V0
V6	GND	GND
V7	VCC33PMP	VCC33PMP
V8	NC	NC
V9	VCC33A	VCC33A
V10	AG4	AG4
V11	AT4	AT4
V12	ATRTN2	ATRTN2
V13	AT5	AT5
V14	VCC33A	VCC33A
V15	NC	NC
V16	VCC33A	VCC33A
V17	GND	GND
V18	TMS	TMS
V19	VJTAG	VJTAG
V20	VCCIB2	VCCIB2
V21	TRST	TRST
V22	TDO	TDO
W1	NC	IO93PDB4V0
W2	GND	GND
W3	NC	IO93NDB4V0
W4	GEB2/IO59PDB4V0	GEB2/IO86PDB4V0
W5	IO59NDB4V0	IO86NDB4V0
W6	AV0	AV0
W7	GNDA	GNDA
W8	AV1	AV1
W9	AV2	AV2
W10	GNDA	GNDA
W11	AV3	AV3
W12	AV6	AV6
W13	GNDA	GNDA
W14	AV7	AV7
W15	AV8	AV8

FG484		
Pin Number	AFS600 Function	AFS1500 Function
W16	GNDA	GNDA
W17	AV9	AV9
W18	VCCIB2	VCCIB2
W19	NC	IO68PPB2V0
W20	TCK	TCK
W21	GND	GND
W22	NC	IO76PPB2V0
Y1	GEC2/IO60PDB4V0	GEC2/IO87PDB4V0
Y2	IO60NDB4V0	IO87NDB4V0
Y3	GEA2/IO58PDB4V0	GEA2/IO85PDB4V0
Y4	IO58NDB4V0	IO85NDB4V0
Y5	NCAP	NCAP
Y6	AC0	AC0
Y7	VCC33A	VCC33A
Y8	AC1	AC1
Y9	AC2	AC2
Y10	VCC33A	VCC33A
Y11	AC3	AC3
Y12	AC6	AC6
Y13	VCC33A	VCC33A
Y14	AC7	AC7
Y15	AC8	AC8
Y16	VCC33A	VCC33A
Y17	AC9	AC9
Y18	ADCGNDREF	ADCGNDREF
Y19	PTBASE	PTBASE
Y20	GNDNVM	GNDNVM
Y21	VCCNVM	VCCNVM
Y22	VPUMP	VPUMP