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Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-1fgg484k

Fusion Device Architecture Overview

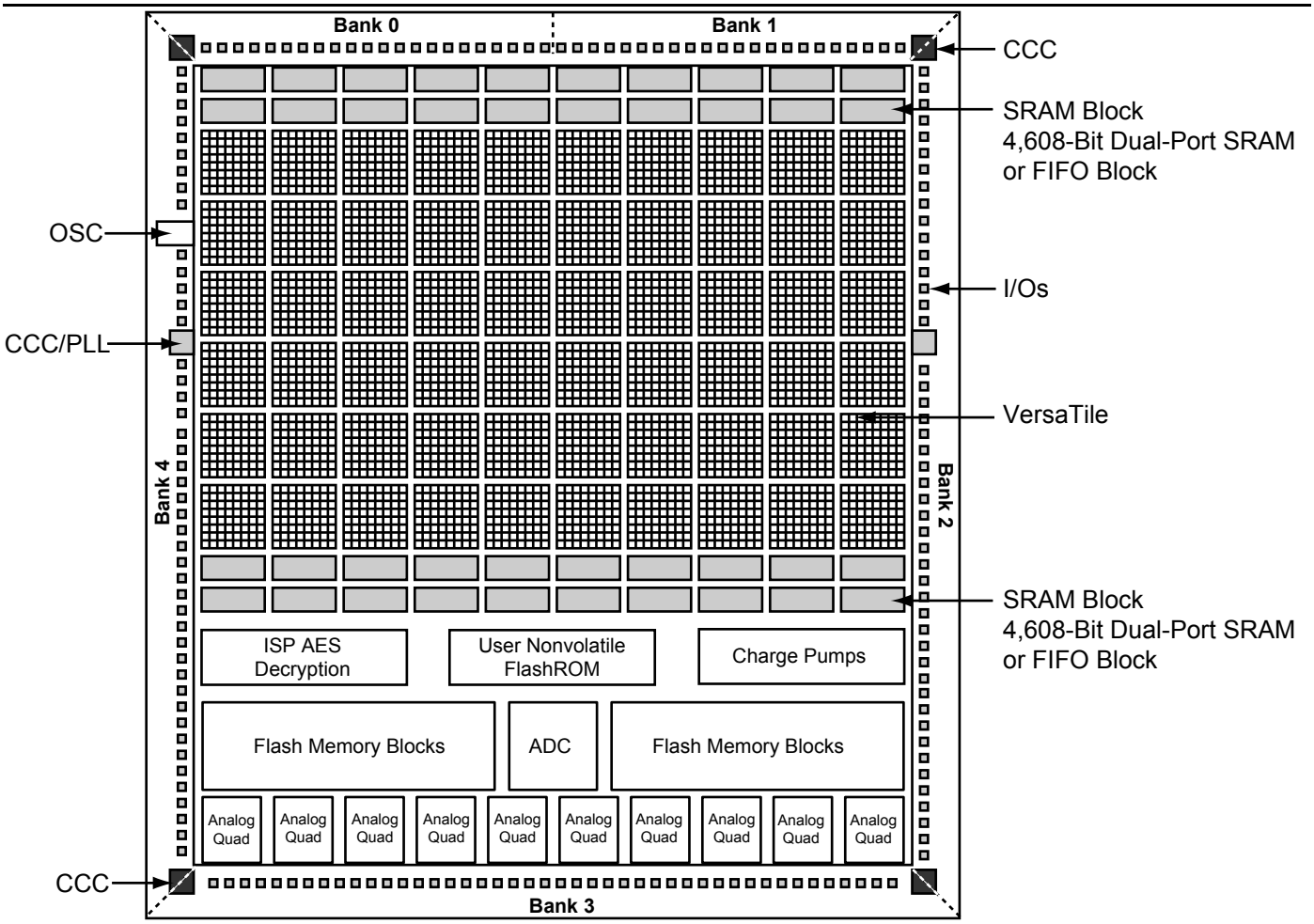


Figure 1 • **Fusion Device Architecture Overview (AFS600)**

Package I/Os: Single-/Double-Ended (Analog)

Fusion Devices	**AFS600**	**AFS1500**
ARM Cortex-M1 Devices	**M1AFS600**	**M1AFS1500**
FG256	119/58 (40)	119/58 (40)
FG484	172/86 (40)	223/109 (40)

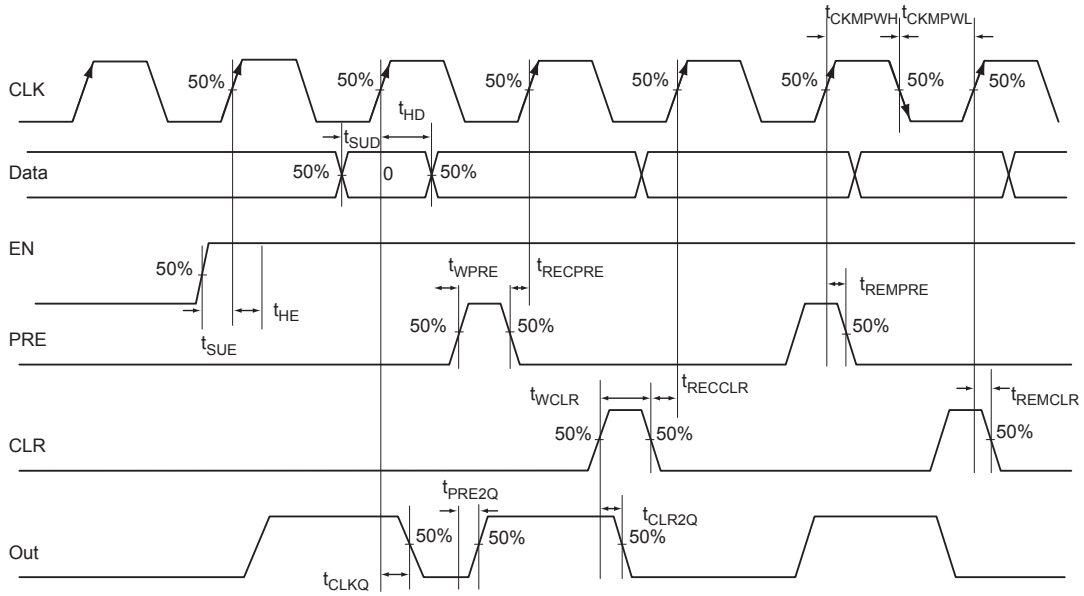


Figure 2-6 • **Sequential Timing Model and Waveforms**

Sequential Timing Characteristics

Table 2-2 • **Register Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.57	0.65	0.76	ns
t_{SUD}	Data Setup Time for the Core Register	0.44	0.50	0.59	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.47	0.53	0.63	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.41	0.47	0.55	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.41	0.47	0.55	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.23	0.26	0.31	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	0.26	0.31	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	0.37	0.43	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	0.41	0.48	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

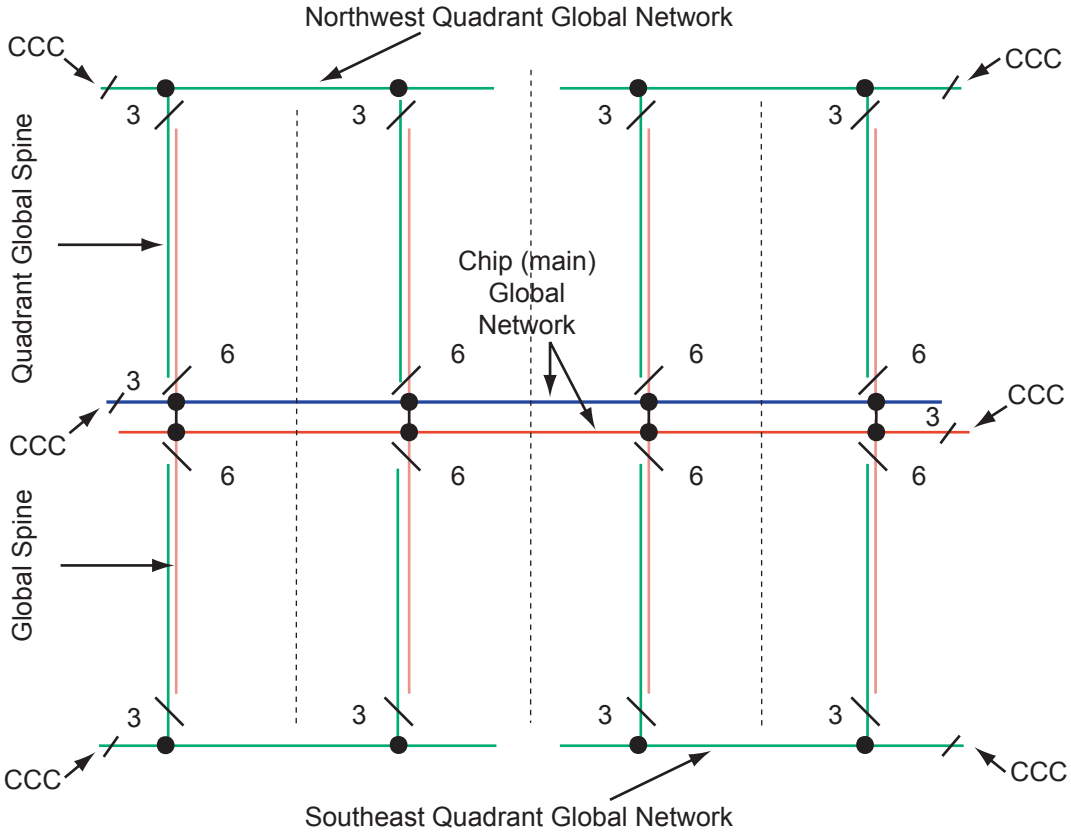


Figure 2-12 • **Global Network Architecture**

Table 2-4 • **Globals/Spines/Rows by Device**

	AFS600	AFS1500
Global VersaNets (trees)*	9	9
VersaNet Spines/Tree	12	20
Total Spines	108	180
VersaTiles in Each Top or Bottom Spine	1,152	1,920
Total VersaTiles	13,824	38,400

*Note: *There are six chip (main) globals and three globals per quadrant.*

Clocking Resources

The Fusion family has a robust collection of clocking peripherals, as shown in the block diagram in Figure 2-16. These on-chip resources enable the creation, manipulation, and distribution of many clock signals. The Fusion integrated RC oscillator produces a 100 MHz clock source with no external components. For systems requiring more precise clock signals, the Fusion family supports an on-chip crystal oscillator circuit. The integrated PLLs in each Fusion device can use the RC oscillator, crystal oscillator, or another on-chip clock signal as a source. These PLLs offer a variety of capabilities to modify the clock source (multiply, divide, synchronize, advance, or delay). Utilizing the CCC found in the popular ProASIC3 family, Fusion incorporates six CCC blocks. The CCCs allow access to Fusion global and local clock distribution nets, as described in the "Global Resources (VersaNets)" section on page 2-11.

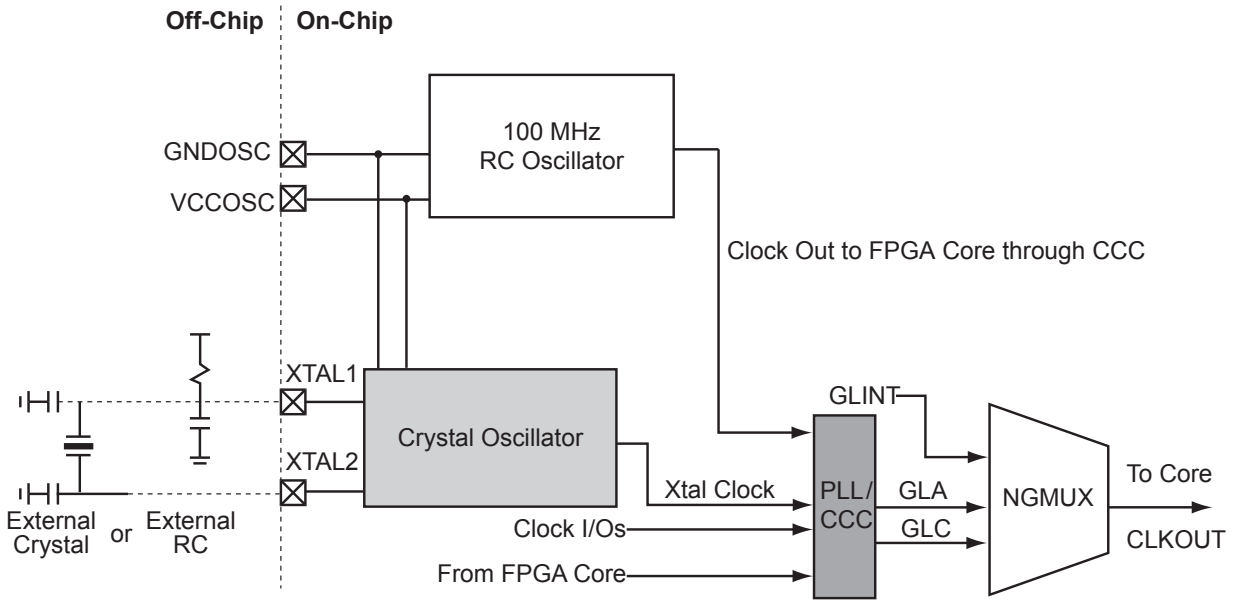
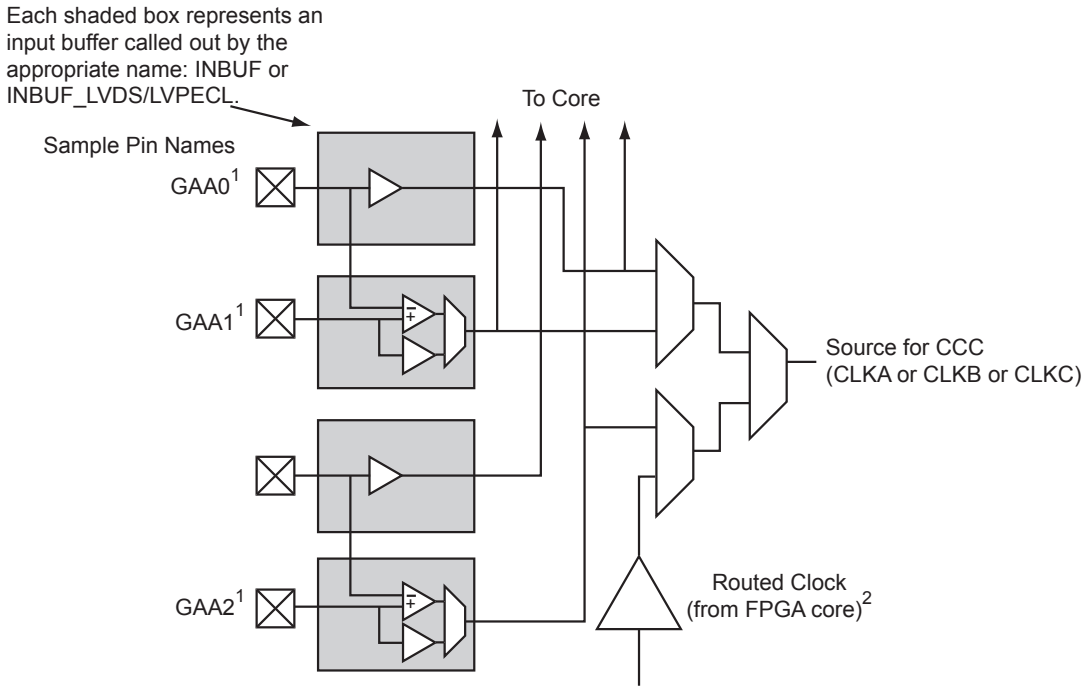


Figure 2-16 • **Fusion Clocking Options**

Global Input Selections

Each global buffer, as well as the PLL reference clock, can be driven from one of the following (Figure 2-22):

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core



Notes:

1. *Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric. Refer to the "User I/O Naming Convention" section on page 2-159 for more information.*
2. *Instantiate the routed clock source input as follows:*
   a) Connect the output of a logic element to the clock input of the PLL, CLKDLY, or CLKINT macro.
   b) Do not place a clock source I/O (INBUF or INBUF_LVPECL/LVDS) in a relevant global pin location.
3. *LVDS-based clock sources are available in the east and west banks on all Fusion devices.*

Figure 2-22 • **Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT**

RAM4K9 Description

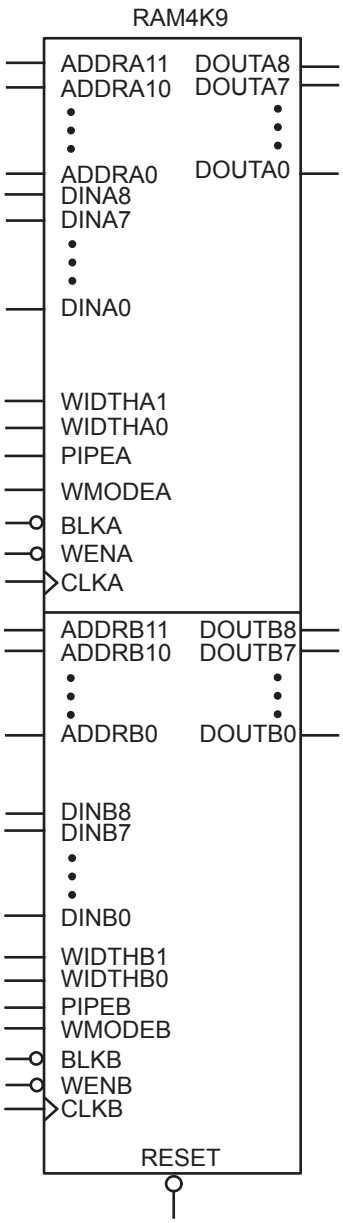


Figure 2-48 • **RAM4K9**

Timing Characteristics

Table 2-34 • FIFO, Worst Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup time	5.01	5.70	6.70	ns
t_{ENH}	REN, WEN Hold time	0.02	0.02	0.03	ns
t_{BKS}	BLK Setup time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold time	0.00	0.00	0.00	ns
t_{DS}	Input data (WD) Setup time	0.19	0.22	0.25	ns
t_{DH}	Input data (WD) Hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.43	2.77	3.25	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.92	1.05	1.23	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.77	2.02	2.37	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.68	1.92	2.25	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.38	7.27	8.55	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.75	1.99	2.34	ns
t_{RSTAF}	RESET Low to Almost-Empty/Full Flag Valid	6.32	7.20	8.46	ns
t_{RSTBQ}	RESET Low to Data out Low on RD (flow-through)	0.95	1.08	1.27	ns
	RESET Low to Data out Low on RD (pipelined)	0.95	1.08	1.27	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.34	0.39	ns
$t_{RECRSTB}$	RESET Recovery	1.55	1.76	2.07	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.22	0.25	0.29	ns
t_{CYC}	Clock Cycle time	3.33	3.79	4.46	ns
FMAX	Maximum Frequency for FIFO	300	264	224	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10 for derating values.

Gate Driver

The Fusion Analog Quad includes a Gate Driver connected to the Quad's AG pin (Figure 2-73). Designed to work with external p- or n-channel MOSFETs, the Gate driver is a configurable current sink or source and requires an external pull-up or pull-down resistor. The AG supports 4 selectable gate drive levels: 1 µA, 3 µA, 10 µA, and 30 µA (Figure 2-74 on page 2-91). The AG also supports a High Current Drive mode in which it can sink 20 mA; in this mode the switching rate is approximately 1.3 MHz with 100 ns turn-on time and 600 ns turn-off time. Modeled on an open-drain-style output, it does not output a voltage level without an appropriate pull-up or pull-down resistor. If 1 V is forced on the drain, the current sinking/sourcing will exceed the ability of the transistor, and the device could be damaged.

The AG pad is turned on via the corresponding GDON*x* pin in the Analog Block macro, where *x* is the number of the corresponding Analog Quad for the AG pad to be enabled (GDON0 to GDON9).

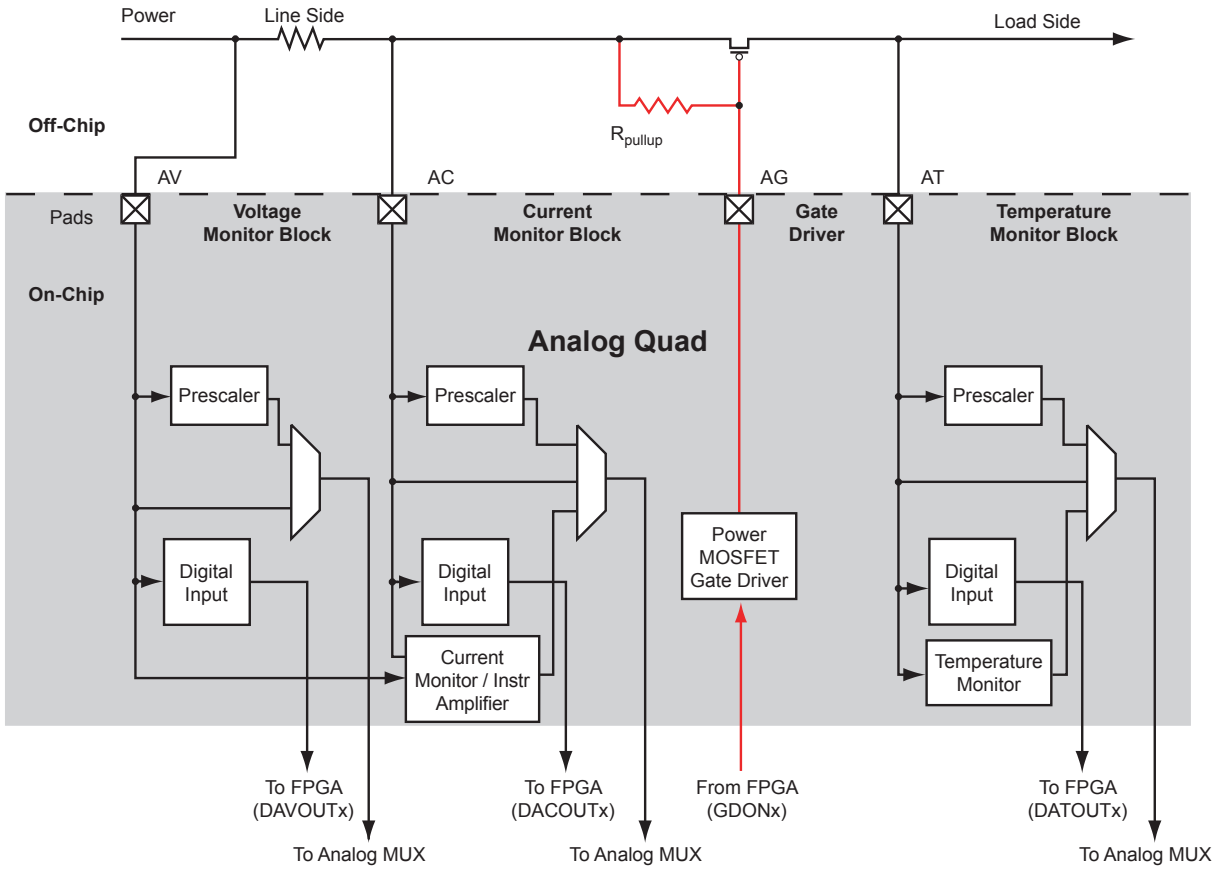


Figure 2-73 • **Gate Driver**

The gate-to-source voltage (V_{gs}) of the external MOSFET is limited to the programmable drive current times the external pull-up or pull-down resistor value (EQ 5).

$$V_{gs} \leq I_g \times (R_{pullup} \text{ or } R_{pulldown})$$

EQ 5

The rate at which the gate voltage of the external MOSFET slews is determined by the current, I_g, sourced or sunk by the AG pin and the gate-to-source capacitance, C_{GS}, of the external MOSFET. As an approximation, the slew rate is given by EQ 6.

$$dv/dt = I_g / C_{GS}$$

EQ 6

Table 2-52 • Calibrated Analog Channel Accuracy [1,2,3]
Worst-Case Extended Temperature Conditions, T_J = 100°C

		Condition	Total Channel Error (LSB)		
Analog Pad	**Prescaler Range (V)**	**Input Voltage[4] (V)**	**Negative Max.**	**Median**	**Positive Max.**
Positive Range			**ADC in 10-Bit Mode**		
AV, AC	16	0.300 to 12.0	–6	1	6
	8	0.250 to 8.00	–6	0	6
	4	0.200 to 4.00	–7	–1	7
	2	0.150 to 2.00	–7	0	7
	1	0.050 to 1.00	–6	–1	6
AT	16	0.300 to 16.0	–5	0	5
	4	0.100 to 4.00	–7	–1	7
Negative Range			**ADC in 10-Bit Mode**		
AV, AC	16	–0.400 to –10.5	–7	1	9
	8	–0.350 to –8.00	–7	–1	7
	4	–0.300 to –4.00	–7	–2	9
	2	–0.250 to –2.00	–7	–2	7
	1	–0.050 to –1.00	–16	–1	20

Notes:

1. *Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Overall accuracy remains the same.*
2. *Requires enabling Analog Calibration using SmartGen Analog System Builder. For further details, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User's Guide.
3. *Calibrated with two-point calibration methodology, using 20% and 80% full-scale points.*
4. *The lower limit of the input voltage is determined by the prescaler input offset.*

Table 2-81 • **Fusion Pro I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)
LVTTL/LVCMOS 3.3 V	Refer to the following tables for more information: Table 2-79 on page 2-153 Table 2-80 on page 2-153	Refer to the following tables for more information: Table 2-79 on page 2-153 Table 2-80 on page 2-153	Off	None	35 pF	–	Off	0	Off
LVCMOS 2.5 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 2.5/5.0 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.8 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.5 V			Off	None	35 pF	–	Off	0	Off
PCI (3.3 V)			Off	None	10 pF	–	Off	0	Off
PCI-X (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (2.5 V)			Off	None	10 pF	–	Off	0	Off
GTL (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL (2.5 V)			Off	None	10 pF	–	Off	0	Off
HSTL Class I			Off	None	20 pF	–	Off	0	Off
HSTL Class II			Off	None	20 pF	–	Off	0	Off
SSTL2 Class I and II			Off	None	30 pF	–	Off	0	Off
SSTL3 Class I and II			Off	None	30 pF	–	Off	0	Off
LVDS, B-LVDS, M-LVDS			Off	None	0 pF	–	Off	0	Off
LVPECL			Off	None	0 pF	–	Off	0	Off

Table 2-109 • 2.5 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	12.02	0.05	1.38	0.44	11.83	12.02	2.82	2.33	14.19	14.38	ns
	–1	0.58	10.22	0.04	1.18	0.38	10.06	10.22	2.40	1.98	12.07	12.23	ns
	–2	0.51	8.97	0.03	1.03	0.33	8.83	8.97	2.11	1.74	10.59	10.74	ns
8 mA	Std.	0.68	8.39	0.05	1.38	0.44	8.55	8.24	3.22	3.05	10.91	10.60	ns
	–1	0.58	7.14	0.04	1.18	0.38	7.27	7.01	2.74	2.59	9.28	9.02	ns
	–2	0.51	6.27	0.03	1.03	0.33	6.38	6.15	2.40	2.28	8.15	7.91	ns
12 mA	Std.	0.68	6.52	0.05	1.38	0.44	6.64	6.24	3.48	3.50	8.99	8.60	ns
	–1	0.58	5.54	0.04	1.18	0.38	5.65	5.31	2.96	2.98	7.65	7.31	ns
	–2	0.51	4.87	0.03	1.03	0.33	4.96	4.66	2.60	2.62	6.72	6.42	ns
16 mA	Std.	0.68	6.08	0.05	1.38	0.44	6.19	5.83	3.54	3.63	8.55	8.18	ns
	–1	0.58	5.17	0.04	1.18	0.38	5.27	4.96	3.01	3.08	7.27	6.96	ns
	–2	0.51	4.54	0.03	1.03	0.33	4.62	4.35	2.65	2.71	6.38	6.11	ns
24 mA	Std.	0.68	5.81	0.05	1.38	0.44	5.80	5.81	3.62	4.08	8.16	8.16	ns
	–1	0.58	4.94	0.04	1.18	0.38	4.94	4.94	3.08	3.47	6.94	6.95	ns
	–2	0.51	4.34	0.03	1.03	0.33	4.33	4.34	2.70	3.05	6.09	6.10	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Timing Characteristics

Table 2-113 • 1.8 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	16.70	0.05	1.53	2.01	0.44	16.50	16.70	2.93	1.67	18.86	19.06	ns
	–1	0.58	14.21	0.04	1.30	1.71	0.38	14.04	14.21	2.50	1.42	16.05	16.21	ns
	–2	0.51	12.47	0.03	1.14	1.50	0.33	12.32	12.47	2.19	1.25	14.09	14.23	ns
4 mA	Std.	0.68	12.01	0.05	1.53	2.01	0.44	12.24	11.34	3.43	2.92	14.59	13.70	ns
	–1	0.58	10.22	0.04	1.30	1.71	0.38	10.41	9.65	2.92	2.49	12.41	11.66	ns
	–2	0.51	8.97	0.03	1.14	1.50	0.33	9.14	8.47	2.56	2.18	10.90	10.23	ns
6 mA	Std.	0.68	9.46	0.05	1.53	2.01	0.44	9.54	8.54	3.76	3.54	11.99	10.90	ns
	–1	0.58	8.05	0.04	1.30	1.71	0.38	8.20	7.26	3.20	3.01	10.20	9.27	ns
	–2	0.51	7.06	0.03	1.14	1.50	0.33	7.20	6.38	2.81	2.64	8.96	8.14	ns
8 mA	Std.	0.68	8.81	0.05	1.53	2.01	0.44	8.97	8.00	3.84	3.71	11.33	10.36	ns
	–1	0.58	7.49	0.04	1.30	1.71	0.38	7.63	6.80	3.27	3.16	9.64	8.81	ns
	–2	0.51	6.58	0.03	1.14	1.50	0.33	6.70	5.97	2.87	2.77	8.46	7.73	ns
12 mA	Std.	0.68	8.37	0.05	1.53	2.01	0.44	8.53	7.97	3.95	4.33‘	10.89	10.33	ns
	–1	0.58	7.12	0.04	1.30	1.71	0.38	7.25	6.78	3.36	3.68	9.26	8.79	ns
	–2	0.51	6.25	0.03	1.14	1.50	0.33	6.37	5.95	2.85	3.23	8.13	7.71	ns
16 mA	Std.	0.68	8.37	0.05	1.53	2.01	0.44	8.53	7.97	3.95	4.33	10.89	10.33	ns
	–1	0.58	7.12	0.04	1.30	1.71	0.38	7.25	6.78	3.36	3.68	9.26	8.79	ns
	–2	0.51	6.25	0.03	1.14	1.50	0.33	6.37	5.95	2.95	3.23	8.13	7.71	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and push-pull output buffer.

Table 2-117 • Minimum and Maximum DC Input and Output Levels

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
Applicable to Pro I/O Banks												
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	15	15
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	15	15
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	15	15
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	55	66	15	15
Applicable to Advanced I/O Banks												
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	16	13	15	15
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	33	25	15	15
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	39	32	15	15
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	55	66	15	15
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	55	66	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

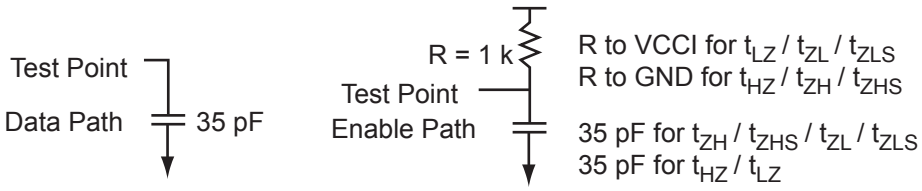


Figure 2-120 • AC Loading

Table 2-118 • 1.5 V LVCMOS AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	35

*Note: *Measuring point = Vtrip. See Table 2-89 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-125 • 3.3 V PCI/PCI-X, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 3.0 V
Applicable to Pro I/Os

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.96	0.05	1.11	1.76	0.44	3.01	2.10	3.45	3.81	5.37	4.46	ns
–1	0.58	2.52	0.04	0.94	1.50	0.38	2.56	1.79	2.94	3.24	4.57	3.80	ns
–2	0.51	2.21	0.03	0.83	1.32	0.33	2.25	1.57	2.58	2.85	4.01	3.33	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-126 • 3.3 V PCI/PCI-X, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 3.0 V
Applicable to Advanced I/Os

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.83	0.05	0.91	0.44	2.88	2.06	3.39	3.78	5.24	4.42	ns
–1	0.58	2.40	0.04	0.77	0.38	2.45	1.75	2.88	3.21	4.45	3.76	ns
–2	0.51	2.11	0.03	0.68	0.33	2.15	1.54	2.53	2.82	3.91	3.30	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Output Register

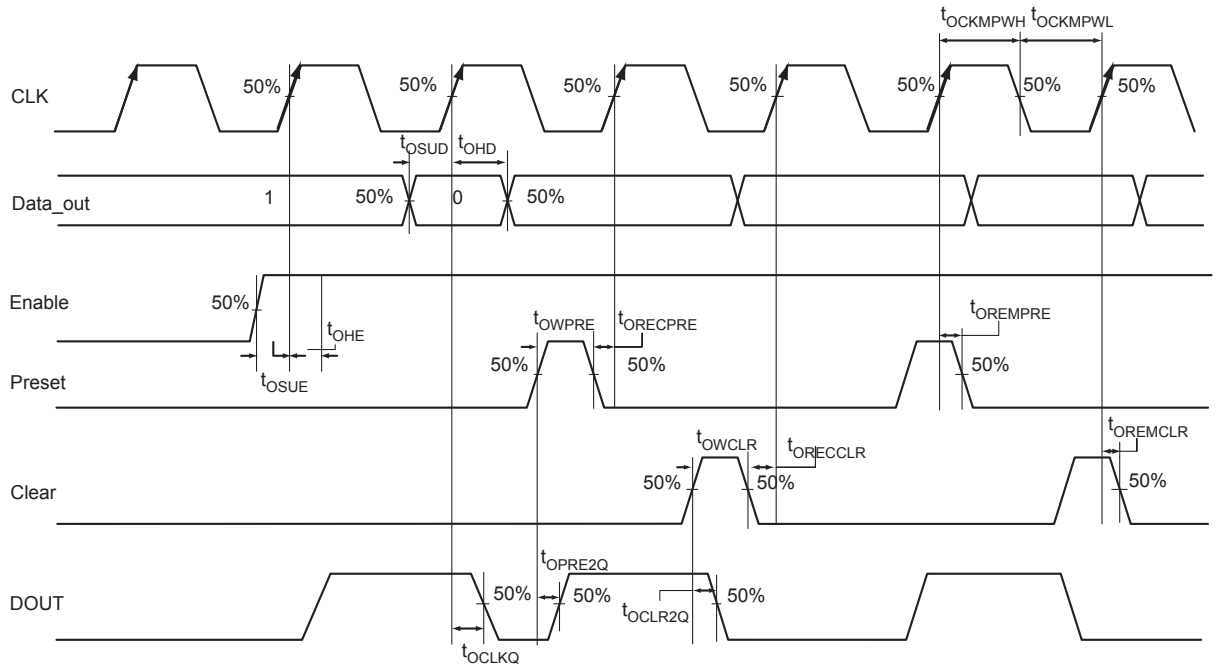


Figure 2-138 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-168 • **Output Data Register Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.61	0.69	0.81	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	0.37	0.43	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.45	0.51	0.60	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.83	0.94	1.11	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.83	0.94	1.11	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	0.26	0.31	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	0.26	0.31	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Security

Fusion devices have a built-in 128-bit AES decryption core. The decryption core facilitates secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a secure programming environment (such as the Microsemi in-house programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late stage product changes or personalization can be implemented easily and securely by simply sending a STAPL file with AES-encrypted data. Secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data. For more information, refer to the *Fusion Security* application note.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-197) block cipher is the National Institute of Standards and Technology (NIST) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4×10^{38} possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (securely) in Fusion devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of Fusion devices remain secure.

AES decryption can also be used on the 1,024-bit FlashROM to allow for secure remote updates of the FlashROM contents. This allows for easy, secure support for subscription model products. See the application note *Fusion Security* for more details.

AES for Flash Memory

AES decryption can also be used on the flash memory blocks. This allows for the secure update of the flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, and the decrypted data can then be stored in the flash memory block.

Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Microsemi).

The user can generate STP programming files from the Designer software and can use these files to program a device.

Fusion devices can be programmed in-system. During programming, VCCOSC is needed in order to power the internal 100 MHz oscillator. This oscillator is used as a source for the 20 MHz oscillator that is used to drive the charge pump for programming.

ISP

Fusion devices support IEEE 1532 ISP via JTAG and require a single VPUMP voltage of 3.3 V during programming. In addition, programming via a microcontroller in a target system can be achieved. Refer to the standard or the "In-System Programming (ISP) of Microsemi's Low Power Flash Devices Using FlashPro4/3/3X" chapter of the *Fusion FPGA Fabric User's Guide* for more details.

JTAG IEEE 1532

Programming with IEEE 1532

Fusion devices support the JTAG-based IEEE1532 standard for ISP. As part of this support, when a Fusion device is in an unprogrammed state, all user I/O pins are disabled. This is achieved by keeping the global IO_EN signal deactivated, which also has the effect of disabling the input buffers. Consequently, the SAMPLE instruction will have no effect while the Fusion device is in this unprogrammed state—different behavior from that of the ProASIC^{PLUS}® device family. This is done

Table 3-3 • **Input Resistance of Analog Pads**

Pads	Pad Configuration	Prescaler Range	Input Resistance to Ground
AV	Analog Input (direct input to ADC)	–	2 kΩ (typical)
		–	> 10 MΩ
	Analog Input (positive prescaler)	+16 V to +2 V	1 MΩ (typical)
		+1 V to +0.125 V	> 10 MΩ
	Analog Input (negative prescaler)	–16 V to –2 V	1 MΩ (typical)
		–1 V to –0.125 V	> 10 MΩ
	Digital input	+16 V to +2 V	1 MΩ (typical)
	Current monitor	+16 V to +2 V	1 MΩ (typical)
		–16 V to –2 V	1 MΩ (typical)
AT	Analog Input (direct input to ADC)	–	1 MΩ (typical)
	Analog Input (positive prescaler)	+16 V, +4 V	1 MΩ (typical)
	Digital input	+16 V, +4 V	1 MΩ (typical)
	Temperature monitor	+16 V, +4 V	> 10 MΩ

Table 3-4 • **Overshoot and Undershoot Limits (as measured on quiet I/Os)[1]**

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3.0 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at a junction temperature of 85°C.*
2. *The duration is allowed at one cycle out of six clock cycle. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*

Table 3-5 • **FPGA Programming, Storage, and Operating Limits**

Product Grade	Storage Temperature	Element	Grade Programming Cycles	Retention
Extended Temperature (K)	Min. T_J = –55°C	FPGA/FlashROM	500	20 years
	Min. T_J = 100°C	Embedded flash	< 1,000	20 years
			< 10,000	10 years
			< 15,000	5 years

Methodology

Total Power Consumption—P_{TOTAL}

Operating Mode, Standby Mode, and Sleep Mode

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

Operating Mode

$P_{STAT} = PDC1 + (N_{NVM\text{-}BLOCKS} * PDC4) + PDC5+ (N_{QUADS} * P_{DC6}) + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8}) + (N_{PLLS} * PDC9)$

$N_{NVM\text{-}BLOCKS}$ is the number of NVM blocks available in the device.

N_{QUADS} is the number of Analog Quads used in the design.

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = PDC2$

Sleep Mode

$P_{STAT} = PDC3$

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB}$

Standby Mode

$P_{DYN} = P_{XTL\text{-}OSC}$

Sleep Mode

$P_{DYN} = 0$ W

Global Clock Dynamic Contribution—P_{CLOCK}

Operating Mode

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Sleep Mode

$P_{CLOCK} = 0$ W

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Pin Number	AFS600 Function	AFS1500 Function
B5	IO05NDB0V0	IO04NDB0V0
B6	IO05PDB0V0	IO04PDB0V0
B7	GND	GND
B8	IO10NDB0V1	IO09NDB0V1
B9	IO13PDB0V1	IO11PDB0V1
B10	GND	GND
B11	IO17NDB1V0	IO24NDB1V0
B12	IO18NDB1V0	IO26NDB1V0
B13	GND	GND
B14	IO21NDB1V0	IO31NDB1V1
B15	IO21PDB1V0	IO31PDB1V1
B16	GND	GND
B17	GBC1/IO26PDB1V1	GBC1/IO40PDB1V2
B18	GBA1/IO28PDB1V1	GBA1/IO42PDB1V2
B19	GND	GND
B20	VCCPLB	VCCPLB
B21	GND	GND
B22	VCC	NC
C1	IO82PDB4V0	IO121PDB4V0
C2	NC	IO122PSB4V0
C3	IO00NDB0V0	IO00NDB0V0
C4	IO00PDB0V0	IO00PDB0V0
C5	VCCIB0	VCCIB0
C6	IO06NDB0V0	IO05NDB0V1
C7	IO06PDB0V0	IO05PDB0V1
C8	VCCIB0	VCCIB0
C9	IO13NDB0V1	IO11NDB0V1
C10	IO11PDB0V1	IO14PDB0V2
C11	VCCIB0	VCCIB0
C12	VCCIB1	VCCIB1
C13	IO20NDB1V0	IO29NDB1V1
C14	IO20PDB1V0	IO29PDB1V1
C15	VCCIB1	VCCIB1
C16	IO25NDB1V1	IO37NDB1V2
C17	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2

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Pin Number	AFS600 Function	AFS1500 Function
C18	VCCIB1	VCCIB1
C19	VCOMPLB	VCOMPLB
C20	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0
C21	NC	IO48PSB2V0
C22	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0
D1	IO82NDB4V0	IO121NDB4V0
D2	GND	GND
D3	IO83NDB4V0	IO123NDB4V0
D4	GAC2/IO83PDB4V0	GAC2/IO123PDB4V0
D5	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0
D6	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0
D7	GAC1/IO03PDB0V0	GAC1/IO03PDB0V0
D8	IO09NDB0V1	IO10NDB0V1
D9	IO09PDB0V1	IO10PDB0V1
D10	IO11NDB0V1	IO14NDB0V2
D11	IO16NDB1V0	IO23NDB1V0
D12	IO16PDB1V0	IO23PDB1V0
D13	NC	IO32NPB1V1
D14	IO23NDB1V1	IO34NDB1V1
D15	IO23PDB1V1	IO34PDB1V1
D16	IO25PDB1V1	IO37PDB1V2
D17	GBB1/IO27PDB1V1	GBB1/IO41PDB1V2
D18	VCCIB2	VCCIB2
D19	NC	IO47PPB2V0
D20	IO30NDB2V0	IO44NDB2V0
D21	GND	GND
D22	IO31NDB2V0	IO45NDB2V0
E1	IO81NDB4V0	IO120NDB4V0
E2	IO81PDB4V0	IO120PDB4V0
E3	VCCIB4	VCCIB4
E4	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0
E5	IO85NDB4V0	IO125NDB4V0
E6	GND	GND
E7	VCCIB0	VCCIB0
E8	NC	IO08NDB0V1

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the Fusion datasheet.

Revision	Changes	Page
Revision 2 (January 2013)	The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43178).	III
	Added values for Std., -1, and -2 grades to the "Speed Grade and Temperature Grade Matrix" table (SAR 44027).	IV
	Added values for minimum pulse width to Table 2-5 • AFS1500 Global Resource Timing, Extended Temperature Case Conditions: TJ = 100°C, VCC = 1.425 V and Table 2-6 • AFS600 Global Resource Timing, Extended Temperature Case Conditions: TJ = 100°C, VCC = 1.425 V in the "VersaNet Timing Characteristics" section. Use the software to determine the FRMAX for the device you are using (SAR 38976).	2-16
	The note in Table 2-11 • Fusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42562).	2-28
	In Table 2-57 • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3), changed the column heading from 'Full-Scale Voltage' to 'Full Scale Voltage in 10-Bit Mode', and added and updated Notes as required (SAR 34921).	2-130
	Added a note to Table 3-2 • Recommended Operating Conditions1 (SAR 43430): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	3-3
	Deleted the Die Size column from the Table 3-6 • Package Thermal Resistance (SAR 43503).	3-8
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40265). Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 1 (August 2012)	The phrase "without debug" was removed from the "Soft ARM® Cortex™- M1 Fusion Devices (M1)" section (SAR 34896).	I
	The maximum number of digital I/Os for AFS1500 was corrected to 223 in Table 1 • Fusion Extended Temperature Devices. The table previously stated 252 (SAR 38876).	I
	The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34678).	I, 1-2
	The Y security option and Licensed DPA Logo was added to the "Product Ordering Codes" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34720).	III
	The "Specifying I/O States During Programming" section is new (SAR 34692).	1-8
	The "RC Oscillator" section was revised to correct a sentence that did not differentiate accuracy for commercial and industrial temperature ranges, which is given in Table 2-7 • Electrical Characteristics of RC Oscillator (SAR 38780).	2-18