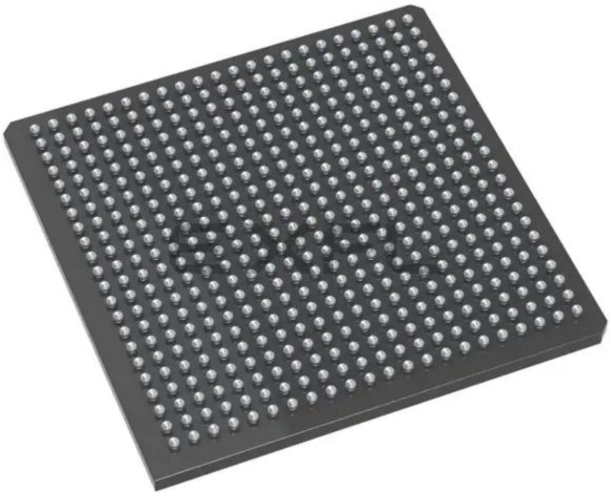

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-fg484k

Almost Full (AFULL) flags in addition to the normal EMPTY and FULL flags. The embedded FIFO control unit contains the counters necessary for the generation of the read and write address pointers. The SRAM/FIFO blocks can be cascaded to create larger configurations.

Clock Resources

PLLs and Clock Conditioning Circuits (CCCs)

Fusion devices provide designers with very flexible clock conditioning capabilities. Each member of the Fusion family contains six CCCs. For the Extended Temperature family, two of these CCCs also include a PLL.

The inputs of the CCC blocks are accessible from the FPGA core or from one of several inputs with dedicated CCC block connections.

The CCC block has the following key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock phase adjustment via programmable and fixed delays from –6.275 ns to +8.75 ns
- Clock skew minimization (PLL)
- Clock frequency synthesis (PLL)
- On-chip analog clocking resources usable as inputs:
  - 100 MHz on-chip RC oscillator
  - Crystal oscillator

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°
- Output duty cycle = 50% ± 1.5%
- Low output jitter. Samples of peak-to-peak period jitter when a single global network is used:
  - 70 ps at 350 MHz
  - 90 ps at 100 MHz
  - 180 ps at 24 MHz
  - Worst case < 2.5% × clock period
- Maximum acquisition time = 150 µs
- Low power consumption of 5 mW

Global Clocking

Fusion devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there are on-chip oscillators as well as a comprehensive global clock distribution network.

The integrated RC oscillator generates a 100 MHz clock. It is used internally to provide a known clock source to the flash memory read and write control. It can also be used as a source for the PLLs.

The crystal oscillator supports the following operating modes:

- Crystal (32.768 KHz to 20 MHz)
- Ceramic (500 KHz to 8 MHz)
- RC (32.768 KHz to 4 MHz)

Each VersaTile input and output port has access to nine VersaNets: six main and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via MUXes. The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

Digital I/Os with Advanced I/O Standards

The Fusion family of FPGAs features a flexible digital I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Fusion FPGAs support many different digital I/O standards, both single-ended and differential.

PLL Macro

The PLL functionality of the clock conditioning block is supported by the PLL macro. Note that the PLL macro reference clock uses the CLKA input of the CCC block, which is only accessible from the global A[2:0] package pins. Refer to Figure 2-22 on page 2-25 for more information.

The PLL macro provides five derived clocks (three independent) from a single reference clock. The PLL feedback loop can be driven either internally or externally. The PLL macro also provides power-down input and lock output signals. During power-up, POWERDOWN should be asserted Low until V_{CC} is up. See Figure 2-19 on page 2-22 for more information.

Inputs:

- CLKA: selected clock input
- POWERDOWN (active low): disables PLLs. The default state is power-down on (active low).

Outputs:

- LOCK (active high): indicates that PLL output has locked on the input reference signal
- GLA, GLB, GLC: outputs to respective global networks
- YB, YC: allows output from the CCC to be routed back to the FPGA core

As previously described, the PLL allows up to five flexible and independently configurable clock outputs. Figure 2-23 on page 2-26 illustrates the various clock output options and delay elements.

As illustrated, the PLL supports three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global networks, respectively, and/or routed to the device core (YB and YC).

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

There is also a delay element in the feedback loop that can be used to advance the clock relative to the reference clock.

The PLL macro reference clock can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate it from the hardwired I/O connection described earlier.

The visual PLL configuration in SmartGen, available with the Libero SoC and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user. SmartGen allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLKA) and the derived clocks (GLA, GLB, GLC, YB, and YC). SmartGen also allows the user to select where the input clock is coming from. SmartGen automatically instantiates the special macro, PLLINT, when needed.

Flash Memory Block Diagram

A simplified diagram of the flash memory block is shown in Figure 2-33.

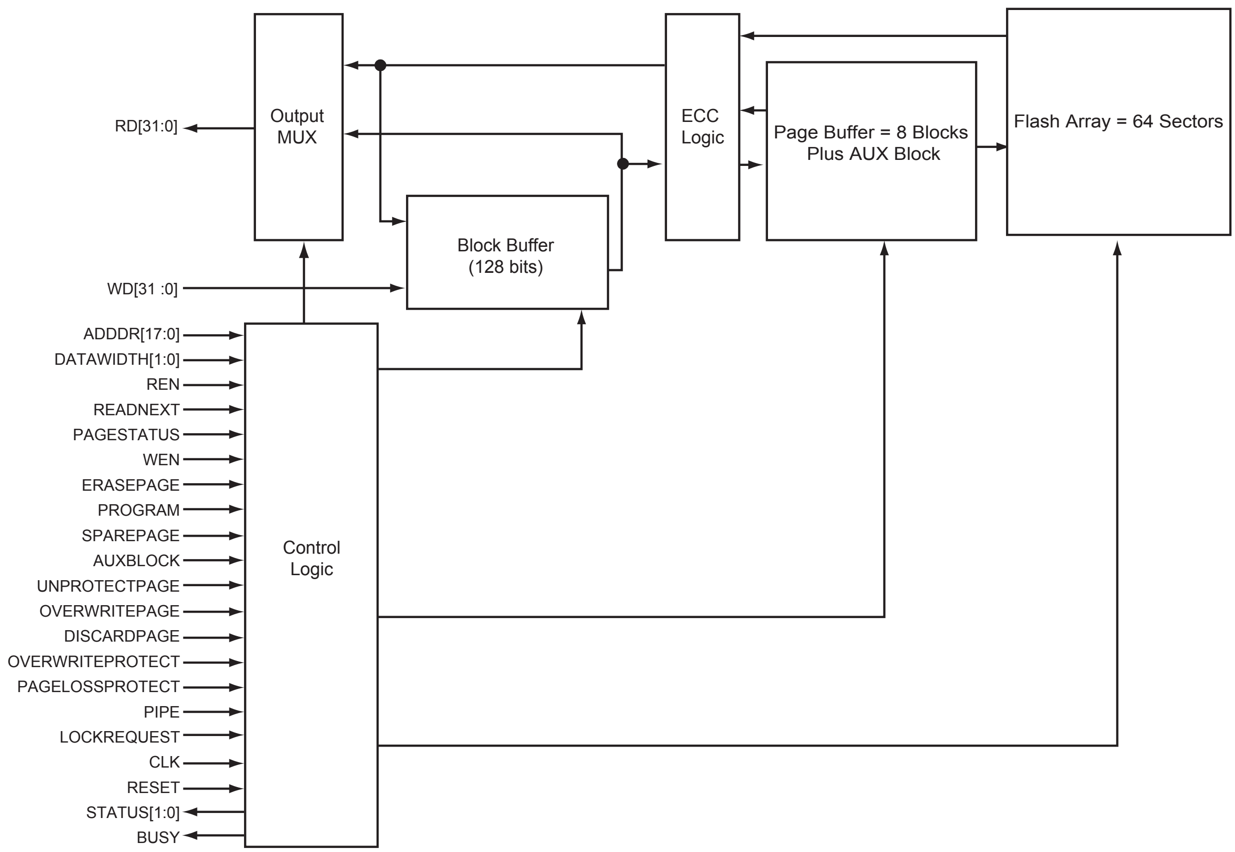

Figure 2-33 **• Flash Memory Block Diagram**

The logic consists of the following sub-blocks:

- Flash Array

  Contains all stored data. The flash array contains 64 sectors, and each sector contains 33 pages of data.
- Page Buffer

  A page-wide volatile register. A page contains 8 blocks of data and an AUX block.
- Block Buffer

  Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic

The FB stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

Data operations are performed in widths of 1 to 4 bytes. A write to a location in a page that is not already in the Page Buffer will cause the page to be read from the FB Array and stored in the Page Buffer. The block that was addressed during the write will be put into the Block Buffer, and the data written by WD will overwrite the data in the Block Buffer. After the data is written to the Block Buffer, the Block Buffer is then written to the Page Buffer to keep both buffers in sync. Subsequent writes to the same block will overwrite the Block Buffer and the Page Buffer. A write to another block in the page will cause the addressed block to be loaded from the Page Buffer, and the write will be performed as described previously.

The data width can be selected dynamically via the DATAWIDTH input bus. The truth table for the data width settings is detailed in Table 2-20. The minimum resolvable address is one 8-bit byte. For data widths greater than 8 bits, the corresponding address bits are ignored—when DATAWIDTH = 0 (2 bytes), ADDR[0] is ignored, and when DATAWIDTH = '10' or '11' (4 bytes), ADDR[1:0] are ignored. Data pins are LSB-oriented and unused WD data pins must be grounded.

Table 2-20 • **Data Width Settings**

DATAWIDTH[1:0]	Data Width
00	1 byte [7:0]
01	2 byte [15:0]
10, 11	4 bytes [31:0]

Flash Memory Block Protection

Page Loss Protection

When the PAGELOSSPROTECT pin is set to logic 1, it prevents writes to any page other than the current page in the Page Buffer until the page is either discarded or programmed.

A write to another page while the current page is Page Loss Protected will return a STATUS of '11'.

Overwrite Protection

Any page that is Overwrite Protected will result in the STATUS being set to '01' when an attempt is made to either write, program, or erase it. To set the Overwrite Protection state for a page, set the OVERWRITEPROTECT pin when a Program operation is undertaken. To clear the Overwrite Protect state for a given page, an Unprotect Page operation must be performed on the page, and then the page must be programmed with the OVERWRITEPROTECT pin cleared to save the new page.

LOCKREQUEST

The LOCKREQUEST signal is used to give the user interface control over simultaneous access of the FB from both the User and JTAG interfaces. When LOCKREQUEST is asserted, the JTAG interface will hold off any access attempts until LOCKREQUEST is deasserted.

Flash Memory Block Operations

FB Operation Priority

The FB provides for priority of operations when multiple actions are requested simultaneously. Table 2-21 shows the priority order (priority 0 is the highest).

Table 2-21 • **FB Operation Priority**

Operation	Priority
System Initialization	0
FB Reset	1
Read	2
Write	3
Erase Page	4
Program	5
Unprotect Page	6
Discard Page	7

TUE – Total Unadjusted Error

TUE is a comprehensive specification that includes linearity errors, gain error, and offset error. It is the worst-case deviation from the ideal device performance. TUE is a static specification (Figure 2-86).

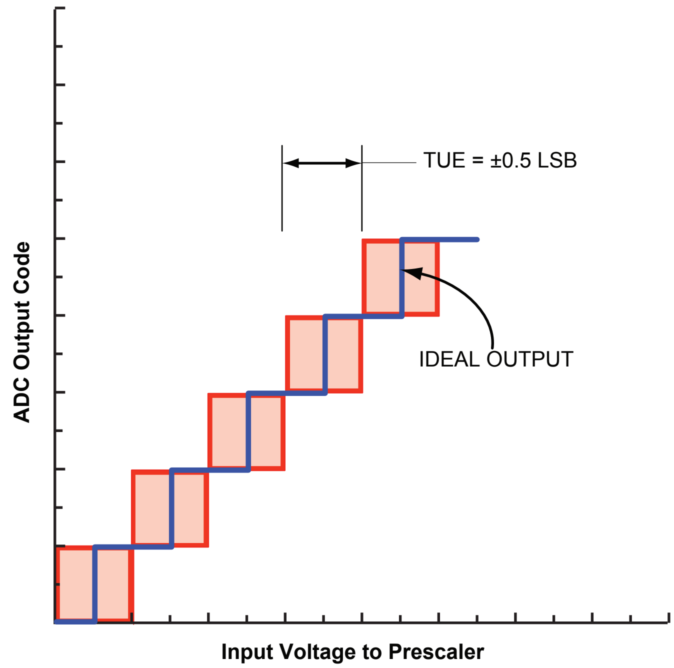

Figure 2-86 • **Total Unadjusted Error (TUE)**

ADC Operation

Once the ADC has powered up and been released from reset, ADCRESET, the ADC will initiate a calibration routine designed to provide optimal ADC performance. The Fusion ADC offers a robust calibration scheme to reduce integrated offset and linearity errors. The offset and linearity errors of the main capacitor array are compensated for with an 8-bit calibration capacitor array. The offset/linearity error calibration is carried out in two ways. First, a power-up calibration is carried out when the ADC comes out of reset. This is initiated by the CALIBRATE output of the Analog Block macro and is a fixed number of ADC_CLK cycles (3,840 cycles), as shown in Figure 2-88 on page 2-111. In this mode, the linearity and offset errors of the capacitors are calibrated.

To further compensate for drift and temperature-dependent effects, every conversion is followed by post-calibration of either the offset or a bit of the main capacitor array. The post-calibration ensures that, over time and with temperature, the ADC remains consistent.

After both calibration and the setting of the appropriate configurations, as explained above, the ADC is ready for operation. Setting the ADCSTART signal high for one clock period will initiate the sample and conversion of the analog signal on the channel as configured by CHNUMBER[4:0]. The status signals SAMPLE and BUSY will show when the ADC is sampling and converting (Figure 2-90 on page 2-112). Both SAMPLE and BUSY will initially go high. After the ADC has sampled and held the analog signal, SAMPLE will go low. After the entire operation has completed and the analog signal is converted, BUSY will go low and DATAVALID will go high. This indicates that the digital result is available on the RESULT[11:0] pins.

DATAVALID will remain high until a subsequent ADC_START is issued. The DATAVALID goes low on the rising edge of SYSCLK, as shown in Figure 2-89 on page 2-111. The RESULT signals will be kept constant until the ADC finishes the subsequent sample. The next sampled RESULT will be available when DATAVALID goes high again. It is ideal to read the RESULT when DATAVALID is '1'. The RESULT is latched and remains unchanged until the next DATAVLAID rising edge.

Table 2-45 • **STC Bits Function**

Name	Bits	Function
STC	[7:0]	Sample time control

Sample time is computed based on the period of ADCCLK.

Distribution Phase

The second phase is called the distribution phase. During distribution phase, the ADC computes the equivalent digital value from the value stored in the input capacitor. In this phase, the output signal SAMPLE goes back to '0', indicating the sample is completed; but the BUSY signal remains '1', indicating the ADC is still busy for distribution. The distribution time depends strictly on the number of bits. If the ADC is configured as a 10-bit ADC, then 10 ADCCLK cycles are needed. EQ 8 describes the distribution time.

$$t_{distrib} = N \times t_{ADCCLK}$$

EQ 21

N: Number of bits

Post-Calibration Phase

The last phase is the post-calibration phase. This is an optional phase. The post-calibration phase takes two ADCCLK cycles. The output BUSY signal will remain '1' until the post-calibration phase is completed. If the post-calibration phase is skipped, then the BUSY signal goes to '0' after distribution phase. As soon as BUSY signal goes to '0', the DATAVALID signal goes to '1', indicating the digital result is available on the RESULT output signals. DATAVAILD will remain '1' until the next ADCSTART is asserted. Microsemi recommends enabling post-calibration to compensate for drift and temperature-dependent effects. This ensures that the ADC remains consistent over time and with temperature. The post-calibration phase is enabled by bit 3 of the Mode register. EQ 9 describes the post-calibration time.

$$t_{post\text{-}cal} = MODE[3] \times (2 \times t_{ADCCLK})$$

EQ 22

MODE[3]: Bit 3 of the Mode register, described in Table 2-40.

The calculation for the conversion time for the ADC is summarized in EQ 23.

$$t_{conv} = t_{sync\_read} + t_{sample} + t_{distrib} + t_{post\text{-}cal} + t_{sync\_write}$$

EQ 23

t_{conv}: conversion time

t_{sync_read}: maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, t_{SYSCLK}.

t_{sample}: Sample time

$t_{distrib}$: Distribution time

$t_{post\text{-}cal}$: Post-calibration time

t_{sync_write}: Maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, t_{SYSCLK}.

Intra-Conversion

Performing a conversion during power-up calibration is possible but should be avoided, since the performance is not guaranteed, as shown in Table 2-49 on page 2-117. This is described as intra-conversion. Figure 2-91 on page 2-112 shows intra-conversion (conversion that starts during power-up calibration).

Injected Conversion

A conversion can be interrupted by another conversion. Before the current conversion is finished, a second conversion can be started by issuing a pulse on signal ADCSTART. When a second conversion is issued before the current conversion is completed, the current conversion would be dropped and the ADC would start the second conversion on the rising edge of the SYSCLK. This is known as injected conversion. Since the ADC is synchronous, the minimum time to issue a second conversion is two clock cycles of SYSCLK after the previous one. Figure 2-92 on page 2-113 shows injected conversion

**Table 2-49 • Analog Channel Specifications (continued)
Extended Temperature Range Conditions, T_J = 100°C (unless noted otherwise),
Typical: VCC33A = 3.3 V, VCC = 1.5 V**

<table>
<tr><th>Parameter</th><th>Description</th><th>Condition</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Units</th></tr>
<tr><td colspan="7">Temperature Monitor Using Analog Pad AT</td></tr>
<tr><td rowspan="12">External Temperature Monitor (external diode 2N3904, T_J = 25°C)[4]</td><td rowspan="3">Resolution</td><td>8-bit ADC</td><td colspan="3">4</td><td>°C</td></tr>
<tr><td>10-bit ADC</td><td colspan="3">1</td><td>°C</td></tr>
<tr><td>12-bit ADC</td><td colspan="3">0.25</td><td>°C</td></tr>
<tr><td rowspan="4">Systematic Offset[5]</td><td>AFS090, AFS250, uncalibrated[7]</td><td colspan="3">5</td><td>°C</td></tr>
<tr><td>AFS090, AFS250, calibrated[7]</td><td colspan="3">0</td><td>°C</td></tr>
<tr><td>AFS600, AFS1500, uncalibrated[7]</td><td colspan="3">11</td><td>°C</td></tr>
<tr><td>AFS600, AFS1500, calibrated[7]</td><td colspan="3">0</td><td>°C</td></tr>
<tr><td>Accuracy</td><td></td><td></td><td>±3</td><td>±5</td><td>°C</td></tr>
<tr><td rowspan="2">External Sensor Source Current</td><td>High level, TMSTBx = 0</td><td></td><td>10</td><td></td><td>µA</td></tr>
<tr><td>Low level, TMSTBx = 1</td><td></td><td>100</td><td></td><td>µA</td></tr>
<tr><td>Max Capacitance on AT pad</td><td></td><td></td><td></td><td>1.3</td><td>nF</td></tr>
<tr><td rowspan="8">Internal Temperature Monitor</td><td rowspan="3">Resolution</td><td>8-bit ADC</td><td>4</td><td></td><td></td><td>°C</td></tr>
<tr><td>10-bit ADC</td><td>1</td><td></td><td></td><td>°C</td></tr>
<tr><td>12-bit ADC</td><td>0.25</td><td></td><td></td><td>°C</td></tr>
<tr><td rowspan="4">Systematic Offset[5]</td><td>AFS090, AFS250, uncalibrated[7]</td><td colspan="3">5</td><td>°C</td></tr>
<tr><td>AFS090, AFS250, calibrated[7]</td><td colspan="3">0</td><td>°C</td></tr>
<tr><td>AFS600, AFS1500 uncalibrated[7]</td><td colspan="3">11</td><td>°C</td></tr>
<tr><td>AFS600, AFS1500 calibrated[7]</td><td colspan="3">0</td><td>°C</td></tr>
<tr><td>Accuracy</td><td></td><td></td><td>±3</td><td>±5</td><td>°C</td></tr>
<tr><td>t_{TMSHI}</td><td>Strobe High time</td><td></td><td>10</td><td></td><td>105</td><td>µs</td></tr>
<tr><td>t_{TMSLO}</td><td>Strobe Low time</td><td></td><td>5</td><td></td><td></td><td>µs</td></tr>
<tr><td>t_{TMSSET}</td><td>Settling time</td><td></td><td>5</td><td></td><td></td><td>µs</td></tr>
</table>

Notes:

1. *VRSM is the maximum voltage drop across the current sense resistor.*
2. *Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as V_{IND} does not exceed these limits.*
3. *VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.*
4. *An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.*
5. *The temperature offset is a fixed positive value.*
6. *The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
7. *When using SmartGen Analog System Builder, CalibIP is required to obtain 0 offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User's Guide.

Table 2-53 • **Analog Channel Accuracy: Monitoring Standard Positive Voltages**
Typical Conditions, T_A = 25°C

Input Voltage (V)	Calibrated Typical Error per Positive Prescaler Setting [1] (%FSR)							Direct ADC [2,3] (%FSR)
	16 V (AT)	16 V (12 V) (AV/AC)	8 V (AV/AC)	4 V (AT)	4 V (AV/AC)	2 V (AV/AC)	1 V (AV/AC)	VAREF = 2.56 V
15	1							
14	1							
12	1	1						
5	2	2	1					
3.3	2	2	1	1	1			
2.5	3	2	1	1	1			1
1.8	4	4	1	1	1	1		1
1.5	5	5	2	2	2	1		1
1.2	7	6	2	2	2	1		1
0.9	9	9	4	3	3	1	1	1

Notes:

1. *Requires enabling Analog Calibration using SmartGen Analog System Builder. For further details, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User's Guide.*
2. *Direct ADC mode using an external VAREF of 2.56V±4.6mV, without Analog Calibration macro.*
3. *For input greater than 2.56 V, the ADC output will saturate. A higher VAREF or prescaler usage is recommended.*

Examples

Calculating Accuracy for an Uncalibrated Analog Channel

Formula

For a given prescaler range, EQ 30 gives the output voltage.

Output Voltage = (Channel Output Offset in V) + (Input Voltage x Channel Gain)

EQ 30

where

Channel Output offset in V = Channel Input offset in LSBs x Equivalent voltage per LSB

Channel Gain Factor = 1+ (% Channel Gain / 100)

Example

Input Voltage = 5 V

Chosen Prescaler range = 8 V range

Refer to Table 2-51 on page 2-122.

Max. Output Voltage = (Max Positive input offset) + (Input Voltage x Max Positive Channel Gain)

Max. Positive input offset = (21 LSB) x (8 mV per LSB in 10-bit mode)

Max. Positive input offset = 166 mV

Max. Positive Gain Error = +3%

Max. Positive Channel Gain = 1 + (+3% / 100)

Max. Positive Channel Gain = 1.03

Max. Output Voltage = (166 mV) + (5 V x 1.03)

Max. Output Voltage = **5.316 V**

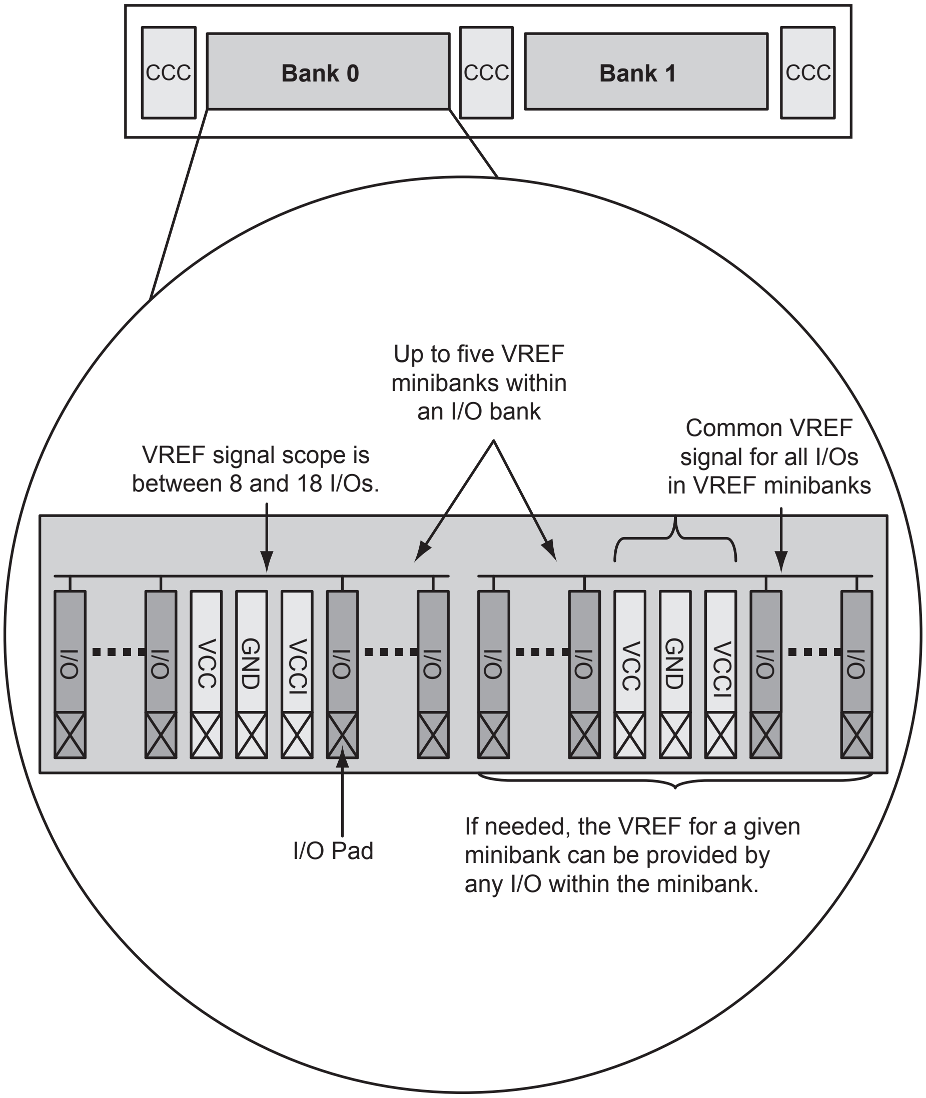

Figure 2-98 • **Fusion Pro I/O Bank Detail Showing VREF Minibanks (north side ofAFS600 and AFS1500)**

Table 2-67 • **I/O Standards Supported by Bank Type**

I/O Bank	**Single-Ended I/O Standards**	**Differential I/O Standards**	**Voltage-Referenced**	**Hot-Swap**
Advanced I/O	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X	LVPECL and LVDS	–	–
Pro I/O	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X	LVPECL and LVDS	GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II	Yes

At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss or transmitter overstress due to transmitter-to-transmitter current shorts. Figure 2-109 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 2-110 shows how bus contention is created, and Figure 2-111 on page 2-152 shows how it can be avoided with the skew circuit.

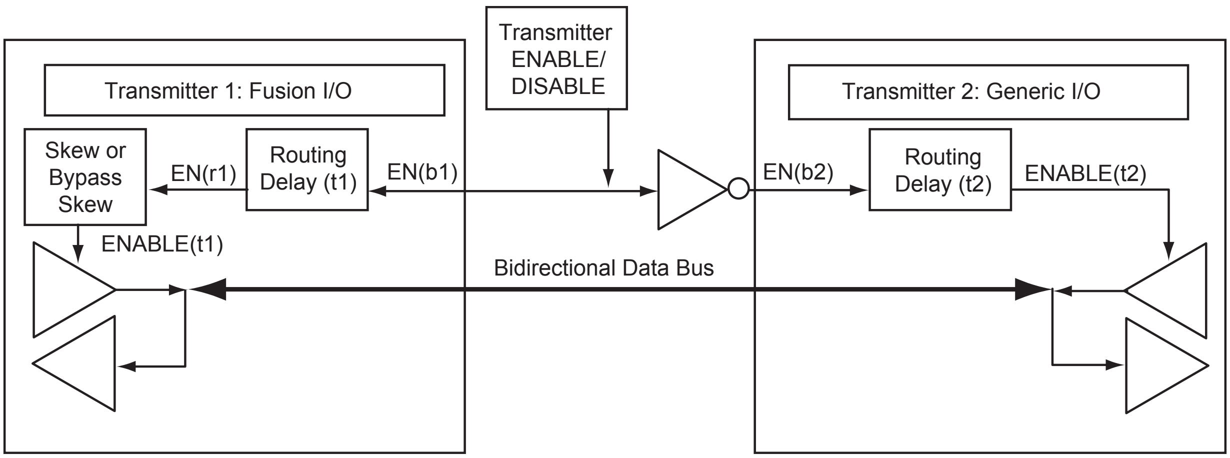

Figure 2-109 • **Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using Fusion Devices**

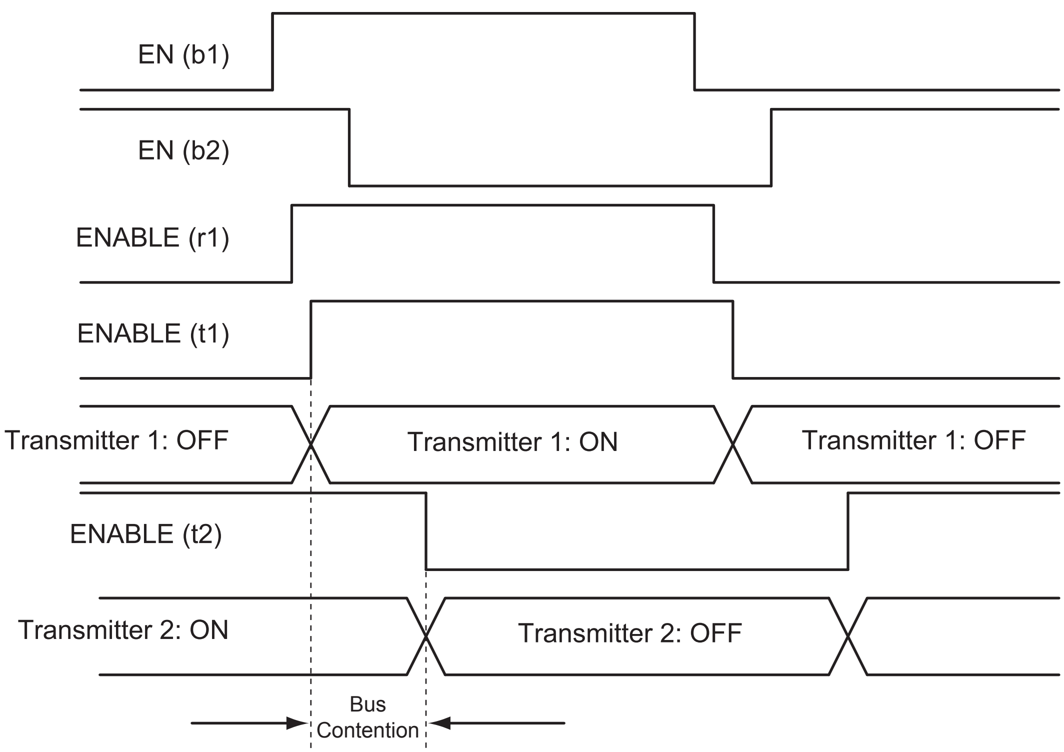

Figure 2-110 • **Timing Diagram (bypasses skew circuit)**

Table 2-83 • Fusion Pro I/O Supported Standards and Corresponding VREF and VTT Voltages Applicable to all I/O Bank types

I/O Standard	Input/Output Supply Voltage (VMVtyp/VCCI_TYP)	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_TYP)
LVTTL/LVCMOS 3.3 V	3.30 V	–	–
LVCMOS 2.5 V	2.50 V	–	–
LVCMOS 2.5 V / 5.0 V Input	2.50 V	–	–
LVCMOS 1.8 V	1.80 V	–	–
LVCMOS 1.5 V	1.50 V	–	–
PCI 3.3 V	3.30 V	–	–
PCI-X 3.3 V	3.30 V	–	–
GTL+ 3.3 V	3.30 V	1.00 V	1.50 V
GTL+ 2.5 V	2.50 V	1.00 V	1.50 V
GTL 3.3 V	3.30 V	0.80 V	1.20 V
GTL 2.5 V	2.50 V	0.80 V	1.20 V
HSTL Class I	1.50 V	0.75 V	0.75 V
HSTL Class II	1.50 V	0.75 V	0.75 V
SSTL3 Class I	3.30 V	1.50 V	1.50 V
SSTL3 Class II	3.30 V	1.50 V	1.50 V
SSTL2 Class I	2.50 V	1.25 V	1.25 V
SSTL2 Class II	2.50 V	1.25 V	1.25 V
LVDS	2.50 V	–	–
LVPECL	3.30 V	–	–

Table 2-85 • Fusion Pro I/O Attributes vs. I/O Standard Applications

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)	HOT_SWAPPABLE
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 2.5 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 2.5/5.0 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 1.8 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 1.5 V	3	3	3	3	3	3	3	3	3	3
PCI (3.3 V)			3		3	3	3	3		
PCI-X (3.3 V)	3		3		3	3	3	3		
GTL+ (3.3 V)			3		3	3	3	3		3
GTL+ (2.5 V)			3		3	3	3	3		3
GTL (3.3 V)			3		3	3	3	3		3
GTL (2.5 V)			3		3	3	3	3		3
HSTL Class I			3		3	3	3	3		3
HSTL Class II			3		3	3	3	3		3
SSTL2 Class I and II			3		3	3	3	3		3
SSTL3 Class I and II			3		3	3	3	3		3
LVDS, B-LVDS, M-LVDS			3			3	3	3		3
LVPECL						3	3	3		3

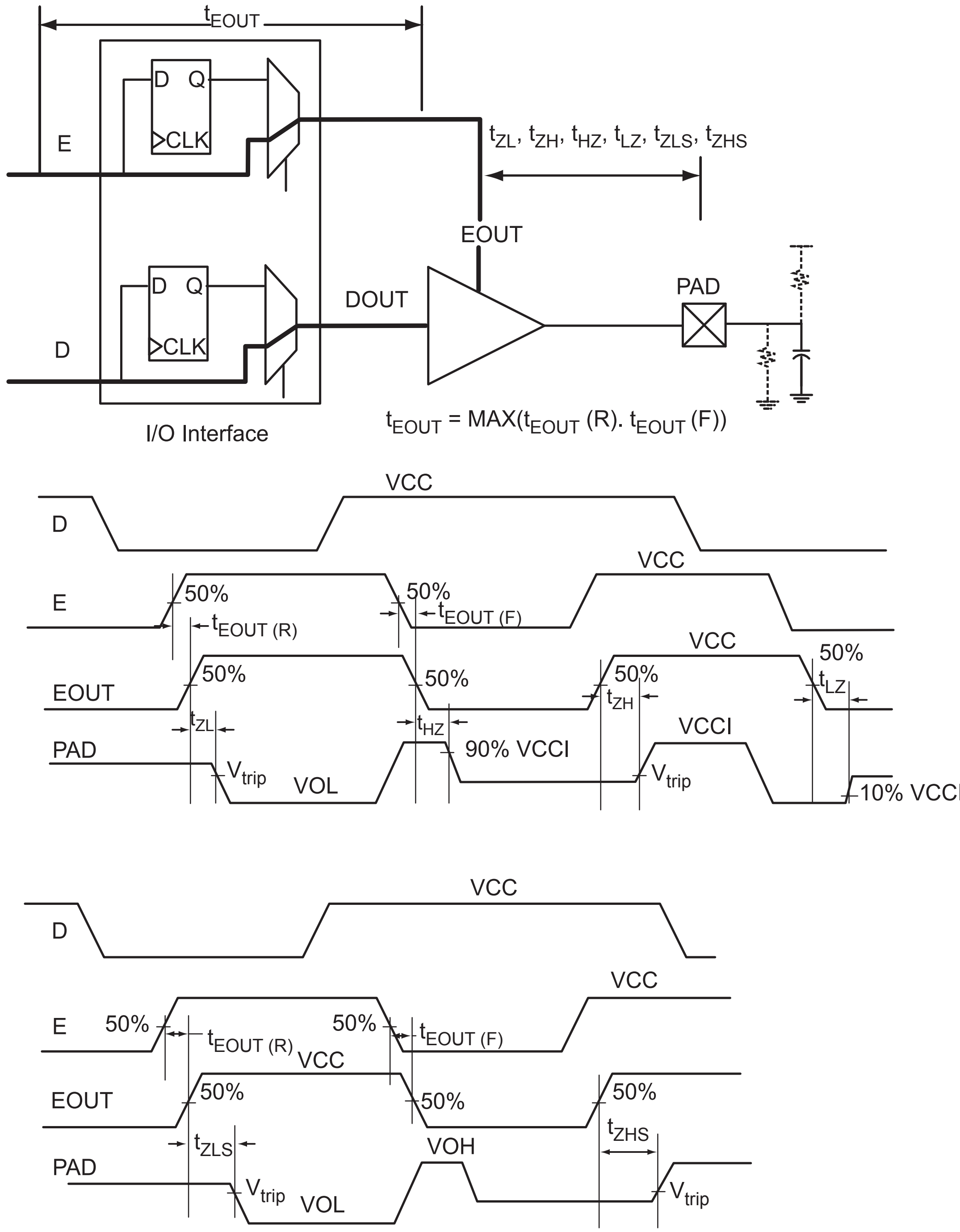

Figure 2-116 • **Tristate Output Buffer Timing Model and Delays (example)**

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
Applicable to Pro I/O Banks												
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10
Applicable to Advanced I/O Banks												
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	10	10

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

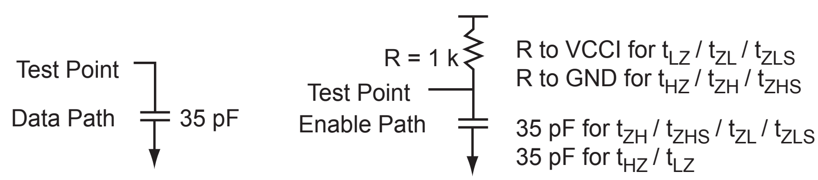

***Figure 2-118* • AC Loading**

***Table 2-106* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

Note: *Measuring point = V_{trip}. See Table 2-89 on page 2-166 for a complete table of trip points.

***Table 2-109* • 2.5 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	12.02	0.05	1.38	0.44	11.83	12.02	2.82	2.33	14.19	14.38	ns
	–1	0.58	10.22	0.04	1.18	0.38	10.06	10.22	2.40	1.98	12.07	12.23	ns
	–2	0.51	8.97	0.03	1.03	0.33	8.83	8.97	2.11	1.74	10.59	10.74	ns
8 mA	Std.	0.68	8.39	0.05	1.38	0.44	8.55	8.24	3.22	3.05	10.91	10.60	ns
	–1	0.58	7.14	0.04	1.18	0.38	7.27	7.01	2.74	2.59	9.28	9.02	ns
	–2	0.51	6.27	0.03	1.03	0.33	6.38	6.15	2.40	2.28	8.15	7.91	ns
12 mA	Std.	0.68	6.52	0.05	1.38	0.44	6.64	6.24	3.48	3.50	8.99	8.60	ns
	–1	0.58	5.54	0.04	1.18	0.38	5.65	5.31	2.96	2.98	7.65	7.31	ns
	–2	0.51	4.87	0.03	1.03	0.33	4.96	4.66	2.60	2.62	6.72	6.42	ns
16 mA	Std.	0.68	6.08	0.05	1.38	0.44	6.19	5.83	3.54	3.63	8.55	8.18	ns
	–1	0.58	5.17	0.04	1.18	0.38	5.27	4.96	3.01	3.08	7.27	6.96	ns
	–2	0.51	4.54	0.03	1.03	0.33	4.62	4.35	2.65	2.71	6.38	6.11	ns
24 mA	Std.	0.68	5.81	0.05	1.38	0.44	5.80	5.81	3.62	4.08	8.16	8.16	ns
	–1	0.58	4.94	0.04	1.18	0.38	4.94	4.94	3.08	3.47	6.94	6.95	ns
	–2	0.51	4.34	0.03	1.03	0.33	4.33	4.34	2.70	3.05	6.09	6.10	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

***Table 2-136* • Minimum and Maximum DC Input and Output Levels**

2.5 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
33 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33	124	169	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

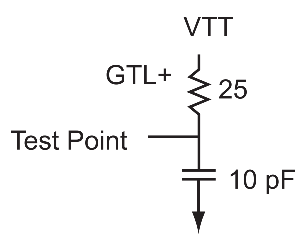

***Figure 2-125* • AC Loading**

***Table 2-137* • 2.5 V GTL+ AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

***Table 2-138* • 2.5 V GTL+**
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.33	0.05	1.60	0.44	2.37	2.21			4.73	4.57	ns
–1	0.58	1.98	0.04	1.36	0.38	2.02	1.88			4.02	3.89	ns
–2	0.51	1.74	0.03	1.19	0.33	1.77	1.65			3.53	3.41	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-161 • LVPECL Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-162 • LVPECL AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (Typ) (V)
1.64	1.94	Cross point	–

Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.

Timing Characteristics

Table 2-163 • LVPECL
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.68	1.90	0.05	1.72	ns
–1	0.58	1.61	0.04	1.47	ns
–2	0.51	1.42	0.03	1.29	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-164 • LVPECL
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.68	1.90	0.05	1.48	ns
–1	0.58	1.61	0.04	1.26	ns
–2	0.51	1.42	0.03	1.11	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Output Register

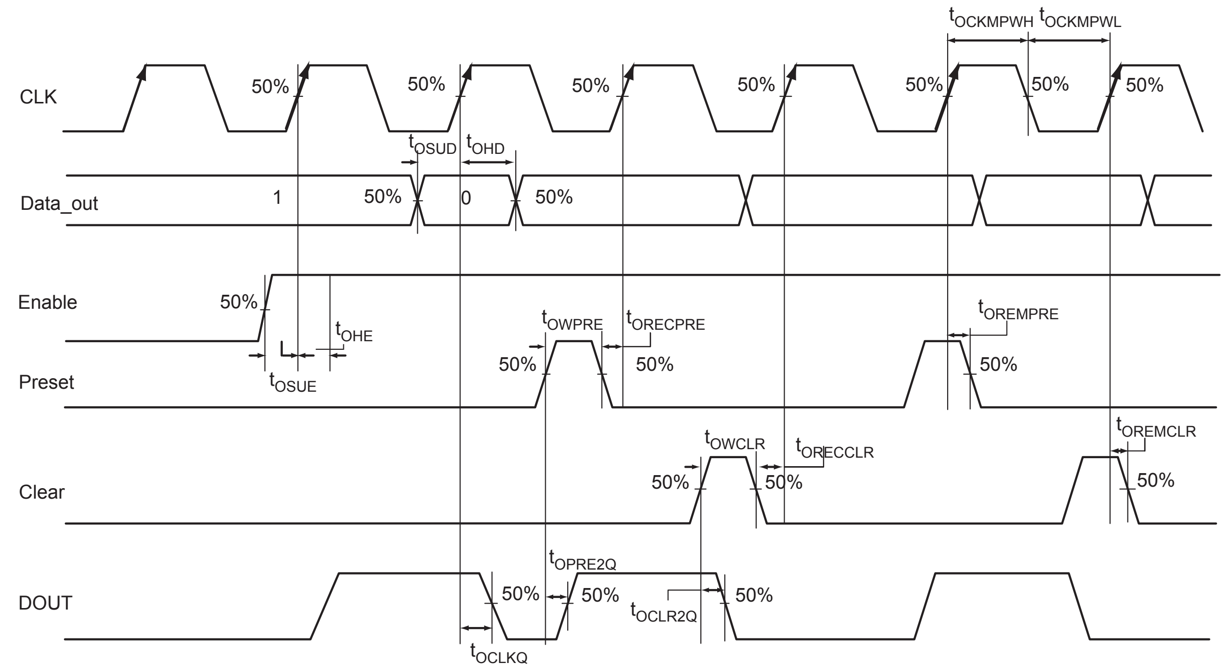

***Figure 2-138* • Output Register Timing Diagram**

Timing Characteristics

***Table 2-168* • Output Data Register Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.61	0.69	0.81	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	0.37	0.43	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.45	0.51	0.60	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.83	0.94	1.11	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.83	0.94	1.11	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	0.26	0.31	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	0.26	0.31	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

RC Oscillator Dynamic Contribution—$P_{RC\text{-}OSC}$

Operating Mode

$P_{RC\text{-}OSC}$ = PAC19

Standby Mode and Sleep Mode

$P_{RC\text{-}OSC}$ = 0 W

Analog System Dynamic Contribution—P_{AB}

Operating Mode

P_{AB} = PAC20

Standby Mode and Sleep Mode

P_{AB} = 0 W

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

***Table 3-14* • Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

***Table 3-15* • Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%
β_4	NVM enable rate for read operations	0%

Standby Mode and Sleep Mode

$P_{S\text{-}CELL} = 0\ W$

$P_{C\text{-}CELL} = 0\ W$

$P_{NET} = 0\ W$

$P_{LOGIC} = 0\ W$

I/O Input and Output Buffer Contribution—$P_{I/O}$

This example uses LVTTL 3.3 V I/O cells. The output buffers are 12 mA–capable, configured with high output slew and driving a 35 pF output load.

$F_{CLK} = 50\ MHz$

Number of input pins used: $N_{INPUTS} = 30$

Number of output pins used: $N_{OUTPUTS} = 40$

Estimated I/O buffer toggle rate: $\alpha_2 = 0.1$ (10%)

Estimated IO buffer enable rate: $\beta_1 = 1$ (100%)

Operating Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * PAC9 * F_{CLK}$

$P_{INPUTS} = 30 * (0.1 / 2) * 0.01739 * 50$

$P_{INPUTS} = 1.30\ mW$

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * PAC10 * F_{CLK}$

$P_{OUTPUTS} = 40 * (0.1 / 2) * 1 * 0.4747 * 50$

$P_{OUTPUTS} = 47.47\ mW$

$P_{I/O} = P_{INPUTS} + P_{OUTPUTS}$

$P_{I/O} = 1.30\ mW + 47.47\ mW$

$P_{I/O} = 48.77\ mW$

Standby Mode and Sleep Mode

$P_{INPUTS} = 0\ W$

$P_{OUTPUTS} = 0\ W$

$P_{I/O} = 0\ W$

RAM Contribution—P_{MEMORY}

Frequency of Read Clock: $F_{READ\text{-}CLOCK} = 10\ MHz$

Frequency of Write Clock: $F_{WRITE\text{-}CLOCK} = 10\ MHz$

Number of RAM blocks: $N_{BLOCKS} = 20$

Estimated RAM Read Enable Rate: $\beta_2 = 0.125$ (12.5%)

Estimated RAM Write Enable Rate: $\beta_3 = 0.125$ (12.5%)

Operating Mode

$P_{MEMORY} = (N_{BLOCKS} * P_{AC11} * \beta_2 * F_{READ\text{-}CLOCK}) + (N_{BLOCKS} * P_{AC12} * \beta_3 * F_{WRITE\text{-}CLOCK})$

$P_{MEMORY} = (20 * 0.025 * 0.125 * 10) + (20 * 0.030 * 0.125 * 10)$

$P_{MEMORY} = 1.38\ mW$

Standby Mode and Sleep Mode

$P_{MEMORY} = 0\ W$