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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs1500-fgg484k

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diode. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADC MUX.

Figure 1-1 on page 1-5 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad measures the source of the power supply. The AC pad measures the voltage drop across an external sense resistor to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad measures the load-side voltage level.

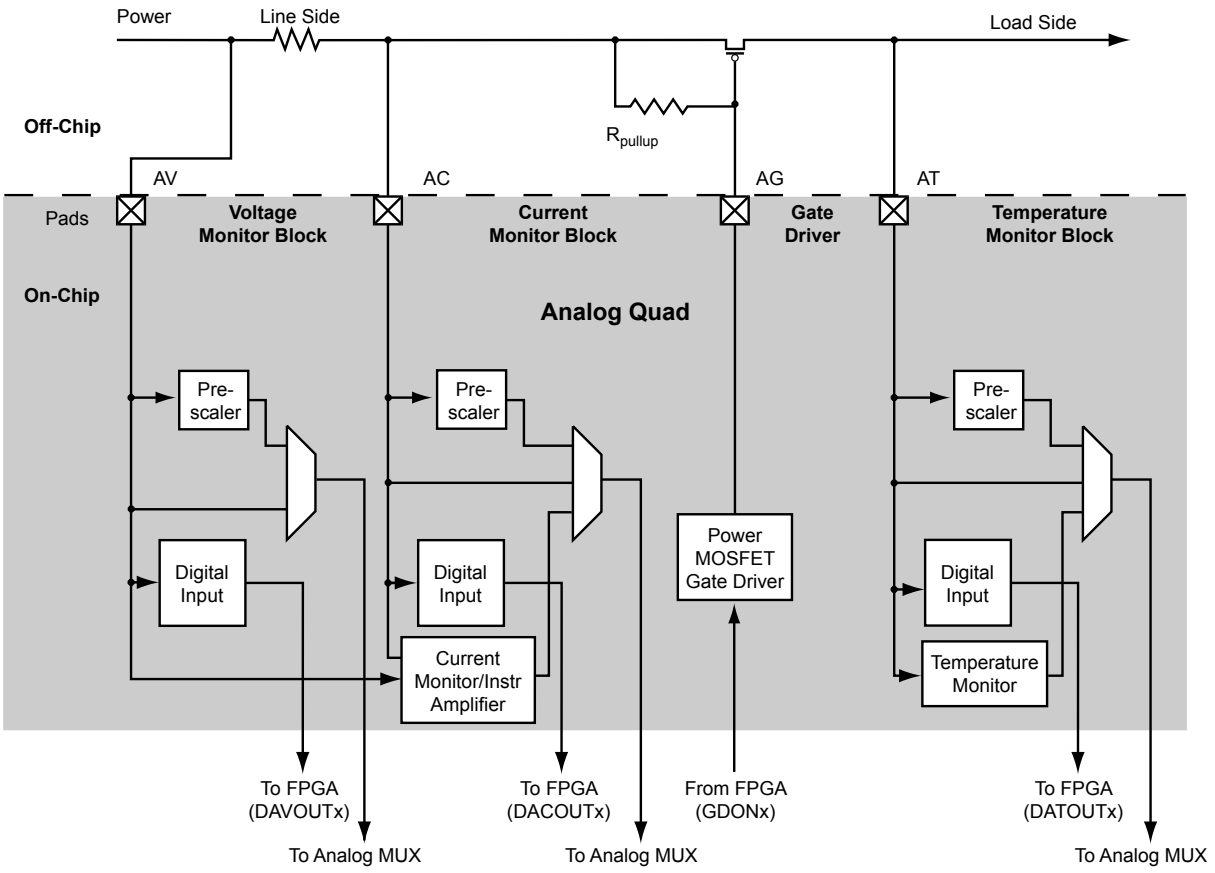


Figure 1-1 • **Analog Quad**

Embedded Memories

Flash Memory Blocks

The flash memory available in each Fusion device is composed of two to four flash blocks, each 2 Mbits in density. Each block operates independently with a dedicated flash controller and interface. Fusion flash memory blocks combine fast access times (60 ns random access and 10 ns access in Read-Ahead mode) with a configurable 8-, 16-, or 32-bit datapath, enabling high-speed flash operation without wait states. The memory block is organized in pages and sectors. Each page has 128 bytes, with 33 pages comprising one sector and 64 sectors per block. The flash block can support multiple partitions. The only constraint on size is that partition boundaries must coincide with page boundaries. The flexibility and granularity enable many use models and allow added granularity in programming updates.

Fusion devices support two methods of external access to the flash memory blocks. The first method is a serial interface that features a built-in JTAG-compliant port, which allows in-system programmability during user or monitor/test modes. This serial interface supports programming of an AES-encrypted stream. Secure data can be passed through the JTAG interface, decrypted, and then programmed in the flash block. The second method is a soft parallel interface.

Global Resource Characteristics

AFS600 VersaNet Topology

Clock delays are device-specific. Figure 2-15 is an example of a global tree used for clock routing. The global tree presented in Figure 2-15 is driven by a CCC located on the west side of the AFS600 device. It is used to drive all D-flip-flops in the device.

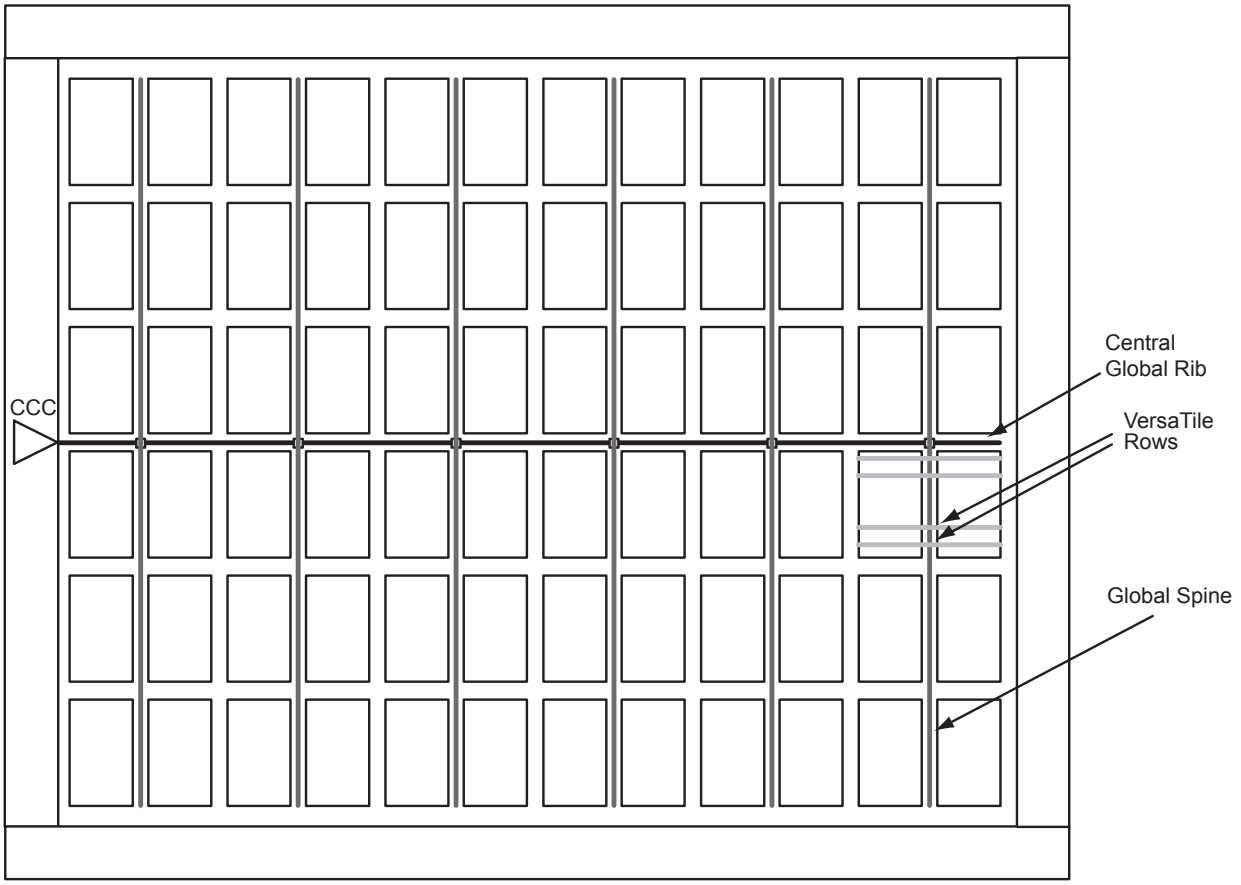


Figure 2-15 • **Example of Global Tree Use in an AFS600 Device for Clock Routing**

CCC and PLL Characteristics

Timing Characteristics

Table 2-11 • Fusion CCC/PLL Specification

Parameter		Min.	Typ.	Max.	Unit
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75		350	MHz
Delay Increments in Programmable Delay Blocks[1,2]			160[3]		ps
Number of Programmable Values in Each Programmable Delay Block				32	
Input Period Jitter				1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}		Max Peak-to-Peak Period Jitter			
		1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz		0.50%		0.70%	
24 MHz to 100 MHz		1.00%		1.20%	
100 MHz to 250 MHz		1.75%		2.00%	
250 MHz to 350 MHz		2.50%		5.60%	
Acquisition Time	LockControl = 0			300	µs
	LockControl = 1			6.0	ms
Tracking Jitter[4]	LockControl = 0			1.6	ns
	LockControl = 1			0.8	ns
Output Duty Cycle		48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1,2]		0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 [1,2]		0.025		5.56	ns
Delay Range in Block: Fixed Delay[1,2]			2.2		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 3-7 on page 3-10 for deratings.*
2. *T_J = 25°C, VCC = 1.5 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.*

No-Glitch MUX (NGMUX)

Positioned downstream from the PLL/CCC blocks, the NGMUX provides a special switching sequence between two asynchronous clock domains that prevents generating any unwanted narrow clock pulses. The NGMUX is used to switch the source of a global between three different clock sources. Allowable inputs are either two PLL/CCC outputs or a PLL/CCC output and a regular net, as shown in Figure 2-24. The GLMUXCFG[1:0] configuration bits determine the source of the CLK inputs (i.e., internal signal or GLC). These are set by SmartGen during design but can also be changed by dynamically reconfiguring the PLL. The GLMUXSEL[1:0] bits control which clock source is passed through the NGMUX to the global network (GL). See Table 2-12.

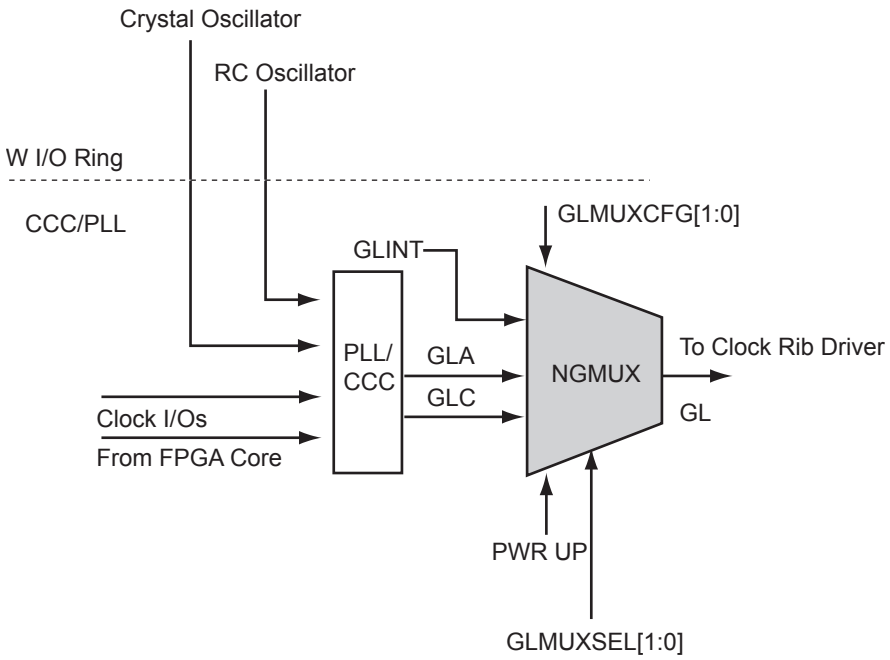


Figure 2-24 • **NGMUX**

Table 2-12 • **NGMUX Configuration and Selection Table**

GLMUXCFG[1:0]	GLMUXSEL[1:0]		Selected Input Signal	MUX Type
00	X	0	GLA	2-to-1 GLMUX
	X	1	GLC	
01	X	0	GLA	2-to-1 GLMUX
	X	1	GLINT	

SRAM and FIFO

All Fusion devices have SRAM blocks along the north side of the device. Additionally, AFS600 and AFS1500 devices have an SRAM block on the south side of the device. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz. The following configurations are available:

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—two read, two write or one read, one write)
- 512×9, 256×18 (two-port RAM—one read and one write)
- Sync write, sync pipelined/nonpipelined read

The Fusion SRAM memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY).

During RAM operation, addresses are sourced by the user logic, and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to Figure 2-47 for more information about the implementation of the embedded FIFO controller.

The Fusion architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. This is done with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1. For example, the write size can be set to 256×18 and the read size to 512×9.

Both the write and read widths for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in Table 2-26 on page 2-58.

When a width of one, two, or four is selected, the ninth bit is unused. For example, when writing 9-bit values and reading 4-bit values, only the first four bits and the second four bits of each 9-bit value are addressable for read operations. The ninth bit is not accessible.

Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.

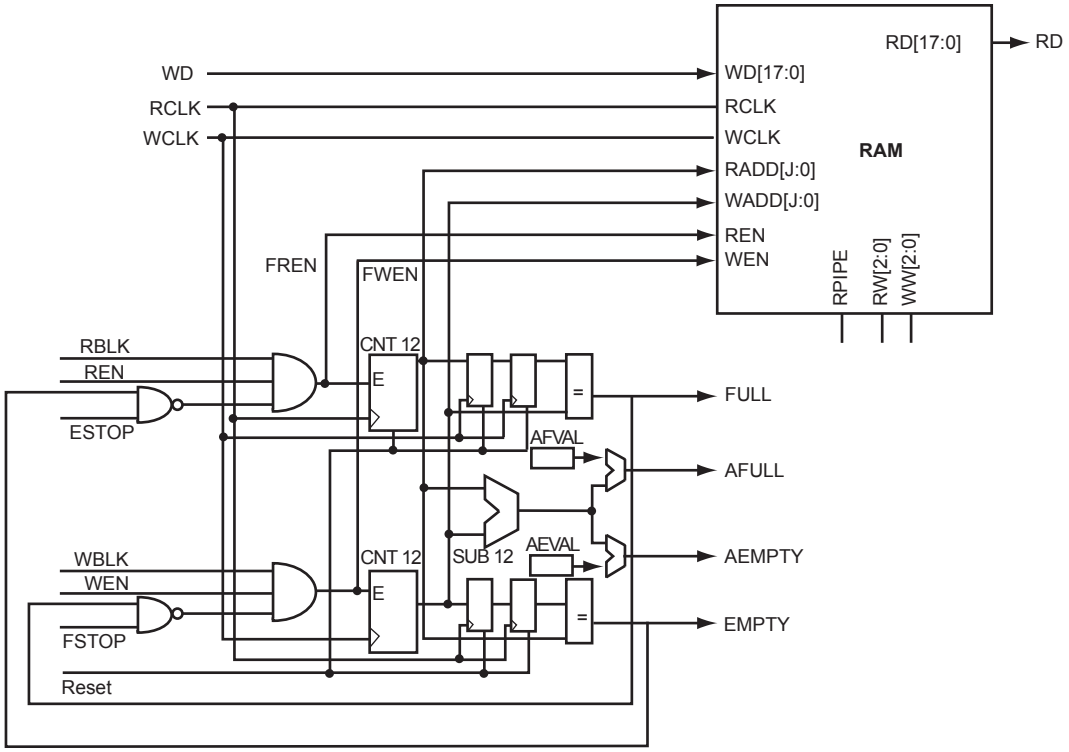
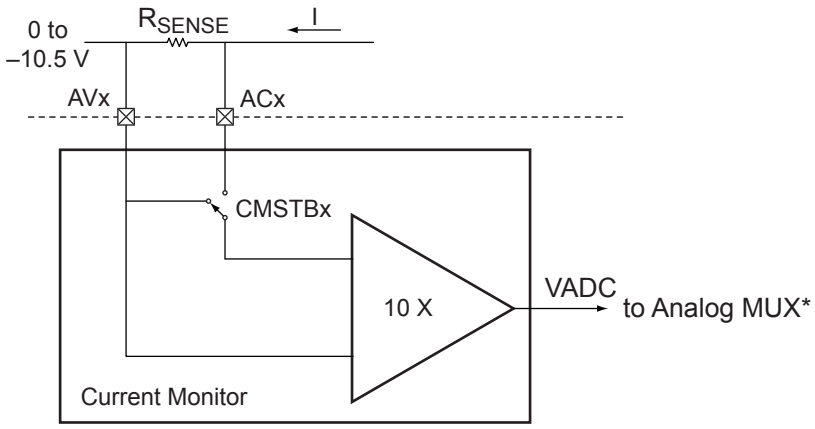


Figure 2-47 • **Fusion RAM Block with Embedded FIFO Controller**

Table 2-36 • Recommended Resistor for Different Current Range Measurement

Current Range	Recommended Minimum Resistor Value (Ohms)
> 5 mA – 10 mA	10 – 20
> 10 mA – 20 mA	5 – 10
> 20 mA – 50 mA	2.5 – 5
> 50 mA – 100 mA	1 – 2
> 100 mA – 200 mA	0.5 – 1
> 200 mA – 500 mA	0.3 – 0.5
> 500 mA – 1 A	0.1 – 0.2
> 1 A – 2 A	0.05 – 0.1
> 2 A – 4 A	0.025 – 0.05
> 4 A – 8 A	0.0125 – 0.025
> 8 A – 12 A	0.00625 – 0.02



*Note: *Refer to Table 2-39 on page 2-105 for the MUX channel number.*

Figure 2-72 • Negative Current Monitor

Terminology

Accuracy

The accuracy of Fusion Current Monitor is ±2 mV minimum plus 5% of the differential voltage at the input. The input accuracy can be translated to error at the ADC output by using EQ 4. The 10 V/V gain is the gain of the Current Monitor Circuit, as described in the "Current Monitor" section on page 2-86. For 8-bit mode, $N = 8$, $V_{AREF} = 2.56$ V, zero differential voltage between AV and AC, the Error (E_{ADC}) is equal to 2 LSBs.

$$E_{ADC} = (2mV + 0.05|V_{AV} - V_{AC}|) \times (10V)/V \times \frac{2^N}{VAREF}$$

EQ 4

where

N is the number of bits

*V*AREF is the Reference voltage

V_{AV} is the voltage at AV pad

V_{AC} is the voltage at AC pad

ADC Input Multiplexer

At the input to the Fusion ADC is a 32:1 multiplexer. Of the 32 input channels, up to 30 are user definable. Two of these channels are hardwired internally. Channel 31 connects to an internal temperature diode so the temperature of the Fusion device itself can be monitored. Channel 0 is wired to the FPGA's 1.5 V VCC supply, enabling the Fusion device to monitor its own power supply. Doing this internally makes it unnecessary to use an analog I/O to support these functions. The balance of the MUX inputs are connected to Analog Quads (see the "Analog Quad" section on page 2-80). Table 2-39 defines which Analog Quad inputs are associated with which specific analog MUX channels. The number of Analog Quads present is device-dependent; refer to the family list in the "Fusion Extended Temperature Devices" table on page I of this datasheet for the number of quads per device. Regardless of the number of quads populated in a device, the internal connections to both VCC and the internal temperature diode remain on Channels 0 and 31, respectively. To sample the internal temperature monitor, it must be strobed (similar to the AT pads). The TMSTBINT pin on the Analog Block macro is the control for strobing the internal temperature measurement diode.

To determine which channel is selected for conversion, there is a five-pin interface on the Analog Block, CHNUMBER[4:0], defined in Table 2-38.

Table 2-38 • **Channel Selection**

Channel Number	CHNUMBER[4:0]
0	00000
1	00001
2	00010
3	00011
. . .	. . .
30	11110
31	11111

Table 2-39 shows the correlation between the analog MUX input channels and the analog input pins.

Table 2-39 • **Analog MUX Channels**

Analog MUX Channel	Signal	Analog Quad Number
0	Vcc_analog	
1	AV0	Analog Quad 0
2	AC0	
3	AT0	
4	AV1	Analog Quad 1
5	AC1	
6	AT1	
7	AV2	Analog Quad 2
8	AC2	
9	AT2	
10	AV3	Analog Quad 3
11	AC3	
12	AT3	
13	AV4	Analog Quad 4
14	AC4	
15	AT4	

connected between the VAREF and ADCGNDREF pins. The VAREFSEL control pin is used to select the reference voltage.

Table 2-41 • **VAREF Bit Function**

Name	Bit	Function
VAREF	0	Reference voltage selection 0 – Internal voltage reference selected. VAREF pin outputs 2.56 V. 1 – Input external voltage reference from VAREF and ADCGNDREF

ADC Clock

The speed of the ADC depends on its internal clock, ADCCLK, which is not accessible to users. The ADCCLK is derived from SYSCLK. Input signal TVC[7:0], Time Divider Control, determines the speed of the ADCCLK in relationship to SYSCLK, based on EQ 15.

$$t_{ADCCLK} = 4 \times (1 + TVC) \times t_{SYSCLK}$$

EQ 15

TVC: Time Divider Control (0–255)

t_{ADCCLK} is the period of ADCCLK, and must be between 0.5 MHz and 10 MHz

t_{SYSCLK} is the period of SYSCLK

Table 2-42 • **TVC Bits Function**

Name	Bits	Function
TVC	[7:0]	SYSCLK divider control

The frequency of ADCCLK, f_{ADCCLK}, must be within 0.5 Hz to 10 MHz.

The inputs to the ADC are synchronized to SYSCLK. A conversion is initiated by asserting the ADCSTART signal on a rising edge of SYSCLK. Figure 2-89 on page 2-111 and Figure 2-90 on page 2-112 show the timing diagram for the ADC.

Acquisition Time or Sample Time Control

Acquisition time (t_{SAMPLE}) specifies how long an analog input signal has to charge the internal capacitor array. Figure 2-87 shows a simplified internal input sampling mechanism of a SAR ADC.

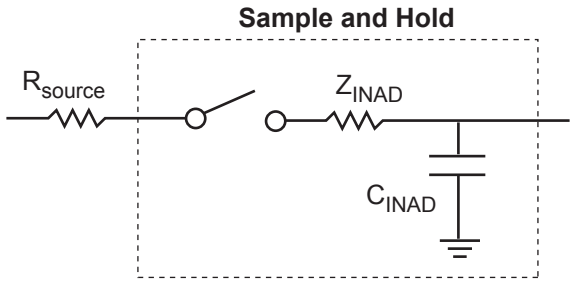


Figure 2-87 • **Simplified Sample and Hold Circuitry**

The internal impedance (Z_{INAD}), external source resistance (R_{SOURCE}), and sample capacitor (C_{INAD}) form a simple RC network. As a result, the accuracy of the ADC can be affected if the ADC is given insufficient time to charge the capacitor. To resolve this problem, you can either reduce the source resistance or increase the sampling time by changing the acquisition time using the STC signal.

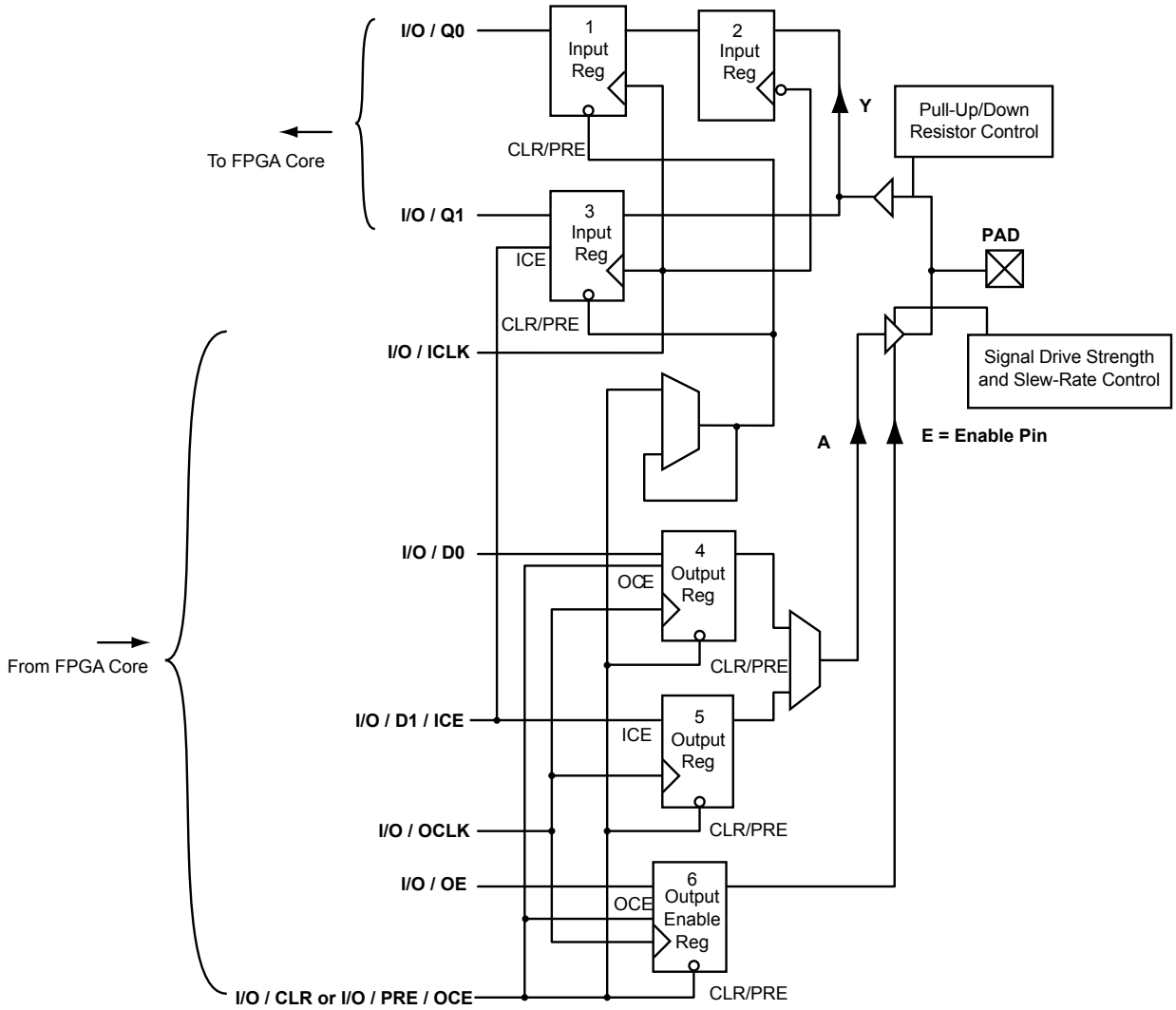
EQ 16 through EQ 18 can be used to calculate the acquisition time required for a given input. The STC signal gives the number of sample periods in ADCCLK for the acquisition time of the desired signal. If the actual acquisition time is higher than the STC value, the settling time error can affect the accuracy of the ADC, because the sampling capacitor is only partially charged within the given sampling cycle. Example acquisition times are given in Table 2-43 and Table 2-44. When controlling the sample time for the ADC

I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 2-99 for a simplified representation of the I/O block.

The number of input registers is selected by a set of switches (not shown in Figure 2-99) between registers to implement single or differential data transmission to and from the FPGA core. The Designer software sets these switches for the user.

A common CLR/PRE signal is employed by all I/O registers when I/O register combining is used. Input register 2 does not have a CLR/PRE pin, as this register is used for DDR implementation. The I/O register combining must satisfy some rules.



Note: Fusion I/Os have registers to support DDR functionality (see the "Double Data Rate (DDR) Support" section on page 2-140 for more information).

Figure 2-99 • **I/O Block Logical Representation**

Selectable Skew between Output Buffer Enable/Disable Time

The configurable skew block is used to delay the output buffer assertion (enable) without affecting deassertion (disable) time.

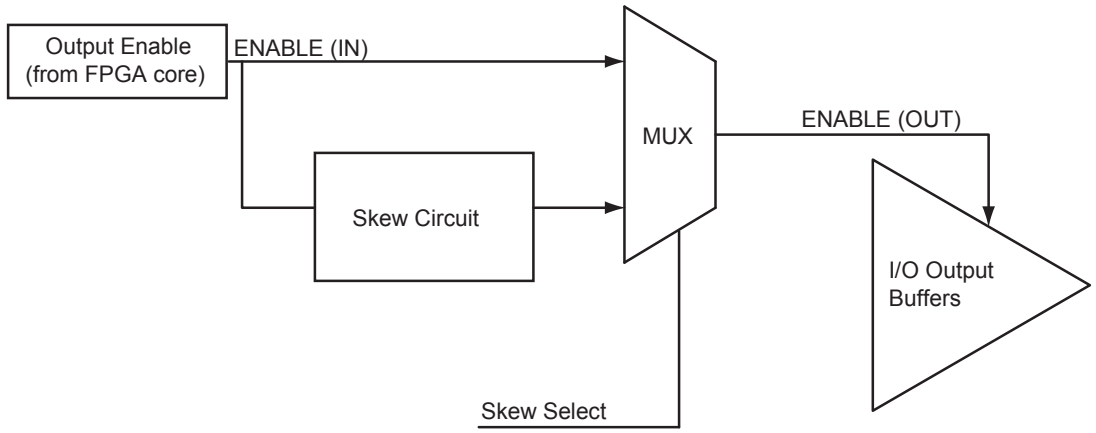


***Figure 2-106* • Block Diagram of Output Enable Path**

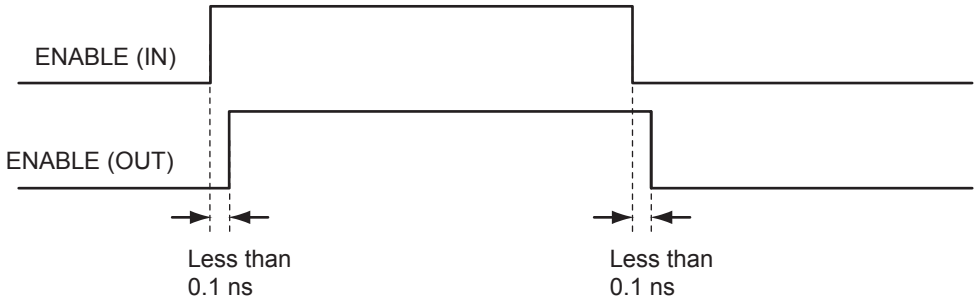


***Figure 2-107* • Timing Diagram (option1: bypasses skew circuit)**

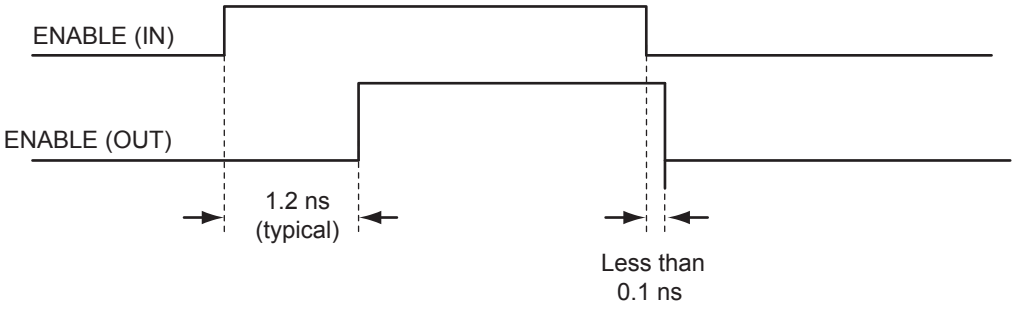


***Figure 2-108* • Timing Diagram (option 2: enables skew circuit)**

Table 2-81 • **Fusion Pro I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)
LVTTL/LVCMOS 3.3 V	Refer to the following tables for more information: Table 2-79 on page 2-153 Table 2-80 on page 2-153	Refer to the following tables for more information: Table 2-79 on page 2-153 Table 2-80 on page 2-153	Off	None	35 pF	–	Off	0	Off
LVCMOS 2.5 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 2.5/5.0 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.8 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.5 V			Off	None	35 pF	–	Off	0	Off
PCI (3.3 V)			Off	None	10 pF	–	Off	0	Off
PCI-X (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (2.5 V)			Off	None	10 pF	–	Off	0	Off
GTL (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL (2.5 V)			Off	None	10 pF	–	Off	0	Off
HSTL Class I			Off	None	20 pF	–	Off	0	Off
HSTL Class II			Off	None	20 pF	–	Off	0	Off
SSTL2 Class I and II			Off	None	30 pF	–	Off	0	Off
SSTL3 Class I and II			Off	None	30 pF	–	Off	0	Off
LVDS, B-LVDS, M-LVDS			Off	None	0 pF	–	Off	0	Off
LVPECL			Off	None	0 pF	–	Off	0	Off

Detailed I/O DC Characteristics

Table 2-93 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
CIN	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
CINCLK	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-94 • I/O Output Buffer Maximum Resistances [1]

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (ohms) [2]	$R_{PULL\text{-}UP}$ (ohms) [3]
Applicable to Pro I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	20 mA	11	–
2.5 V GTL	20 mA	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: www.microsemi.com/soc/techdocs/models/ibis.html.*
2. *R(PULL-DOWN-MAX) = VOLspec / IOLspec*
3. *R(PULL-UP-MAX) = (VCCImax – VOHspec) / IOHspec*

Table 2-108 • 2.5 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	9.30	0.05	1.59	1.75	0.44	8.57	9.30	2.87	2.41	10.93	11.65	ns
	–1	0.58	7.91	0.04	1.36	1.49	0.38	7.29	7.91	2.44	2.05	9.30	9.91	ns
	–2	0.51	6.94	0.03	1.19	1.31	0.33	6.40	6.94	2.14	1.80	8.16	8.70	ns
8 mA	Std.	0.68	5.56	0.05	1.59	1.75	0.44	5.56	5.56	3.27	3.19	7.91	7.92	ns
	–1	0.58	4.73	0.04	1.36	1.49	0.38	4.73	4.73	2.78	2.72	6.73	6.73	ns
	–2	0.51	4.15	0.03	1.19	1.31	0.33	4.15	4.15	2.44	2.38	5.91	5.91	ns
12 mA	Std.	0.68	3.95	0.05	1.59	1.75	0.44	4.02	3.68	3.55	3.69	6.38	6.04	ns
	–1	0.58	3.36	0.04	1.36	1.49	0.38	3.42	3.13	3.02	3.14	5.43	5.14	ns
	–2	0.51	2.95	0.03	1.19	1.31	0.33	3.00	2.75	2.65	2.75	4.76	4.51	ns
16 mA	Std.	0.68	3.72	0.05	1.59	1.75	0.44	3.79	3.29	3.61	3.82	6.15	5.65	ns
	–1	0.58	3.16	0.04	1.36	1.49	0.38	3.22	2.80	3.07	3.25	5.23	4.80	ns
	–2	0.51	2.78	0.03	1.19	1.31	0.33	2.83	2.46	2.69	2.85	4.59	4.22	ns
24 mA	Std.	0.68	3.44	0.05	1.59	1.75	0.44	3.50	2.62	3.69	4.33	5.86	4.98	ns
	–1	0.58	2.93	0.04	1.36	1.49	0.38	2.98	2.23	3.14	3.68	4.99	4.23	ns
	–2	0.51	2.57	0.03	1.19	1.31	0.33	2.62	1.95	2.75	3.23	4.38	3.72	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-139 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
8 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8	39	32	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

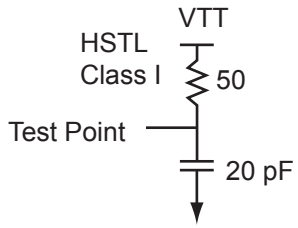


Figure 2-126 • AC Loading

Table 2-140 • HSTL Class I AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

*Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

Table 2-141 • HSTL Class I
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	3.25	0.05	2.24	0.44	3.41	3.31			5.77	5.67	ns
–1	0.58	2.85	0.04	1.91	0.38	2.90	2.82			4.91	4.83	ns
–2	0.51	2.50	0.03	1.67	0.33	2.55	2.48			4.31	4.24	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-151 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
16 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	16	16	54	51	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

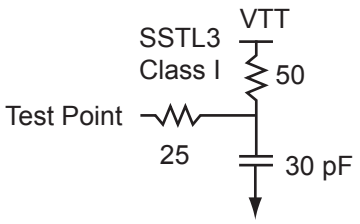


Figure 2-130 • AC Loading

SSTL3 Class I

Table 2-152 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

*Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

Table 2-153 • SSTL3 Class I
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.43	0.05	1.32	0.44	2.48	1.94			4.84	4.29	ns
–1	0.58	2.07	0.04	1.12	0.38	2.11	1.65			4.11	3.65	ns
–2	0.51	1.82	0.03	0.99	0.33	1.85	1.45			3.61	3.21	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

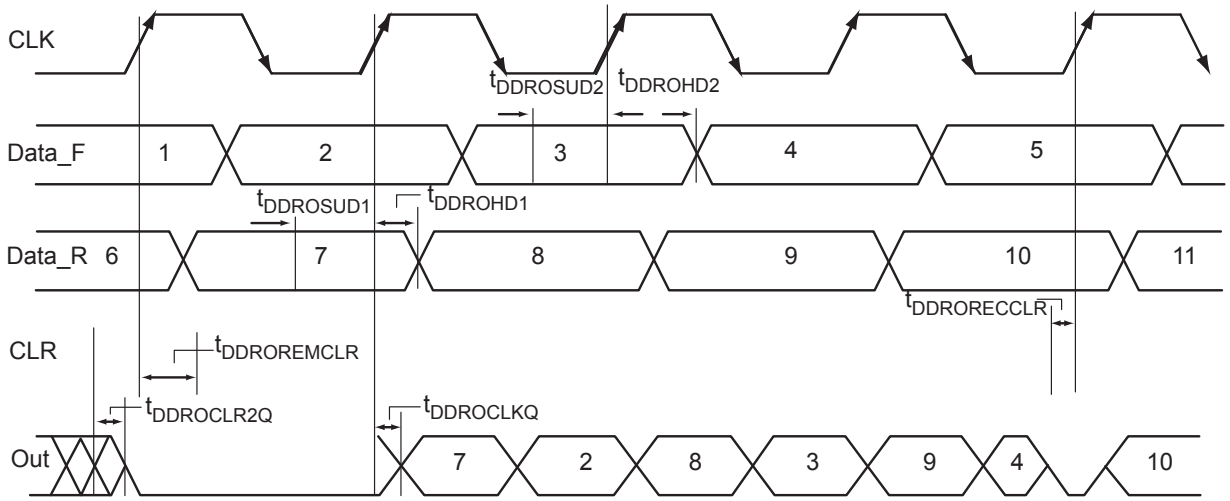


***Figure 2-143* • Output DDR Timing Diagram**

Timing Characteristics

***Table 2-173* • Output DDR Propagation Delays**
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.72	0.82	0.97	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.39	0.44	0.52	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.39	0.43	0.52	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.83	0.94	1.11	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	0.26	0.31	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.36	0.41	0.48	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.37	0.43	ns
FDDOMAX	Maximum Frequency for the Output DDR	1,404	1,232	1,048	MHz

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 3-8 • **AFS1500 Quiescent Supply Current Characteristics (continued)**

Parameter	Description	Conditions	Temp.	Min.	Typ.	Max.	Unit
IJTAG	JTAG I/O quiescent current	Operational standby[4], VJTAG = 3.63 V	T_J = 25°C		80	100	µA
			T_J = 85°C		80	100	µA
			T_J = 100°C		80	100	µA
		Standby mode[5] or Sleep mode[6], VJTAG = 0 V			0	0	µA
IPP	Programming supply current	Non-programming mode, VPUMP = 3.63 V	T_J = 25°C		39	80	µA
			T_J = 85°C		40	80	µA
			T_J = 100°C		40	80	µA
		Standby mode[5] or Sleep mode[6], VPUMP = 0 V			0	0	µA
ICCNVM	Embedded NVM current	Reset asserted, VCCNVM = 1.575 V	T_J = 25°C		50	150	µA
			T_J =85°C		50	150	µA
			T_J = 100°C		50	150	µA
ICCPLL	1.5 V PLL quiescent current	Operational standby, VCCPLL = 1.575 V	T_J = 25°C		130	200	µA
			T_J = 85°C		130	200	µA
			T_J = 100°C		130	200	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC and ICC15A.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V. Sleep mode is not supported between –40°C and –55°C*

Revision	Changes	Page
Revision 1 (continued)	The "Intra-Conversion" section and "Injected Conversion" section had definitions incorrectly interchanged and have been corrected. Figure 2-91 • Intra-Conversion Timing Diagram and Figure 2-92 • Injected-Conversion Timing Diagram were also incorrectly interchanged and have been replaced correctly. Reference in the figure notes to EQ 10 has been corrected to EQ 23 (SAR 34917).	2-109, 2-112
	In Table 3-3 • Input Resistance of Analog Pads, the prescalar range for the 'Analog Input (direct input to ADC)" configurations was removed as inapplicable for direct inputs. The input resistance for direct inputs is covered in Table 2-50 • Electrical Characteristics (SAR 38709).	2-120
	The value for impedance of VINAP in Table 2-50 • Electrical Characteristics was corrected by moving it to the Typical column rather than the Minimum column (SAR 32822).	2-120
	The "Examples" for calibrating accuracy for ADC channels were revised and corrected to make them consistent with terminology in the associated tables (SARs 38699, 38700).	2-124
	A note was added to Table 2-56 • Analog Quad ACM Byte Assignment and the introductory text for Table 2-66 • Internal Temperature Monitor Control Truth Table, stating that for the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set (SAR 38701).	2-129, 2-132
	t_{DOUT} was corrected to t_{DIN} in Figure 2-114 • Input Buffer Timing Model and Delays (example) (SAR 38704).	2-161
	The drive strength, IOL, and IOH for 3.3 V GTL and 2.5 V GTL were changed from 25 mA to 20 mA in the following tables (SAR 38778): Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Extended Temperature Conditions Table 2-91 • Summary of I/O Timing Characteristics – Software Default Settings, Extended Temperature Case Conditions: TJ = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI as Per Configuration Table 2-94 • I/O Output Buffer Maximum Resistances 1 Table 2-127 • Minimum and Maximum DC Input and Output Levels Table 2-130 • Minimum and Maximum DC Input and Output Levels	2-164 2-167 2-169 2-197 2-198
	The formulas in the table notes for Table 2-95 • I/O Weak Pull-Up/Pull-Down Resistances, Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values were corrected (SAR 34752).	2-171
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34881).	2-175
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34801): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-180
	The following notes were removed from Table 2-157 • LVDS Minimum and Maximum DC Input and Output Levels (SAR 34809): ±5% Differential input voltage = ±350 mV	2-207
	Corrected the inadvertent error in maximum values for LVPECL VIH and VIL and revised them to "3.6" in Table 2-161 • LVPECL Minimum and Maximum DC Input and Output Levels, making these consistent with Table 3-1 • Absolute Maximum Ratings, and Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os)1 (SAR 37688).	2-210

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