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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	172
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-1fgg484k

FPGA logic or an on-chip soft microprocessor can access flash memory through the parallel interface. Since the flash parallel interface is implemented in the FPGA fabric, it can potentially be customized to meet special user requirements. For more information, refer to the *CoreCFI Handbook.* The flash memory parallel interface provides configurable byte-wide (×8), word-wide (×16), or dual-word-wide (×32) data port options. Through the programmable flash parallel interface, the on-chip and off-chip memories can be cascaded for wider or deeper configurations.

The flash memory has built-in security. The user can configure either the entire flash block or the small blocks to prevent unintentional or intrusive attempts to change or destroy the storage contents. Each on-chip flash memory block has a dedicated controller, enabling each block to operate independently.

The flash block logic consists of the following sub-blocks:

- Flash block – Contains all stored data. The flash block contains 64 sectors and each sector contains 33 pages of data.
- Page Buffer – Contains the contents of the current page being modified. A page contains 8 blocks of data.
- Block Buffer – Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic – The flash memory stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

User Nonvolatile FlashROM

In addition to the flash blocks, Fusion devices have 1 Kbit of user-accessible, nonvolatile FlashROM on-chip. The FlashROM is organized as 8×128-bit pages. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IEEE 1532 JTAG programming interface. Pages can be individually programmed (erased and written). On-chip AES decryption can be used selectively over public networks to securely load data such as security keys stored in the FlashROM for a user design.

The FlashROM can be programmed (erased and written) via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing.

The FlashPoint tool in the Fusion development software solutions, Libero SoC and Designer, has extensive support for flash memory blocks and FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using the Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

Fusion devices have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be written through a 4-bit port and read as a single bitstream. The SRAM blocks can be initialized from the flash memory blocks or via the device JTAG port (ROM emulation mode), using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and

Timing Characteristics

Table 2-1 • Combinatorial Cell Propagation Delays
Extended Temperature Range Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–2	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.47	0.55	ns
AND2	Y = A · B	t_{PD}	0.49	0.55	0.65	ns
NAND2	Y = !(A · B)	t_{PD}	0.49	0.55	0.65	ns
OR2	Y = A + B	t_{PD}	0.50	0.57	0.67	ns
NOR2	Y = !(A + B)	t_{PD}	0.50	0.57	0.67	ns
XOR2	Y = A ⊕ B	t_{PD}	0.76	0.87	1.02	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.72	0.82	0.96	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.90	1.03	1.21	ns
MUX2	Y = A !S + B S	t_{PD}	0.52	0.60	0.70	ns
AND3	Y = A · B · C	t_{PD}	0.58	0.66	0.77	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Sample VersaTile Specifications—Sequential Module

The Fusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library (Figure 2-5). For more details, refer to the *IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide*.

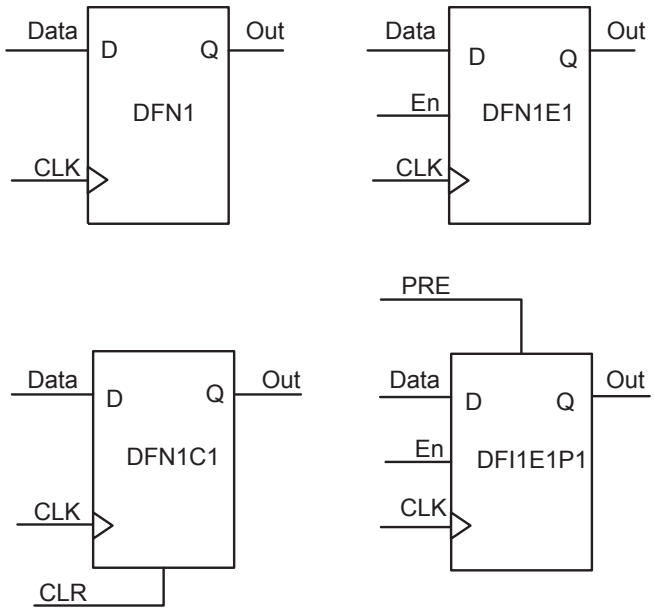


Figure 2-5 • Sample of Sequential Cells

Global Resources (VersaNets)

Fusion devices offer powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has six CCCs. The west CCC also contains a PLL core. In the AFS600 and AFS1500, the west and the east CCCs each contain a PLL. The PLLs include delay lines, a phase shifter (0°, 90°, 180°, 270°), and clock multipliers/dividers. Each CCC has all the circuitry needed for the selection and interconnection of inputs to the VersaNet global network. The east and west CCCs each have access to three VersaNet global lines on each side of the chip (six lines total). The CCCs at the four corners each have access to three quadrant global lines on each quadrant of the chip.

Advantages of the VersaNet Approach

One of the architectural benefits of Fusion is the set of powerful and low-delay VersaNet global networks. Fusion offers six chip (main) global networks that are distributed from the center of the FPGA array (Figure 2-11). In addition, Fusion devices have three regional globals (quadrant globals) in each of the four chip quadrants. Each core VersaTile has access to nine global network resources: three quadrant and six chip (main) global networks. There are a total of 18 global networks on the device. Each of these networks contains spines and ribs that reach all VersaTiles in all quadrants (Figure 2-12 on page 2-12). This flexible VersaNet global network architecture allows users to map up to 180 different internal/external clocks in a Fusion device. Details on the VersaNet networks are given in Table 2-4 on page 2-12. The flexibility of the Fusion VersaNet global network allows the designer to address several design requirements. User applications that are clock-resource-intensive can easily route external or gated internal clocks using VersaNet global routing networks. Designers can also drastically reduce delay penalties and minimize resource usage by mapping critical, high-fanout nets to the VersaNet global network.

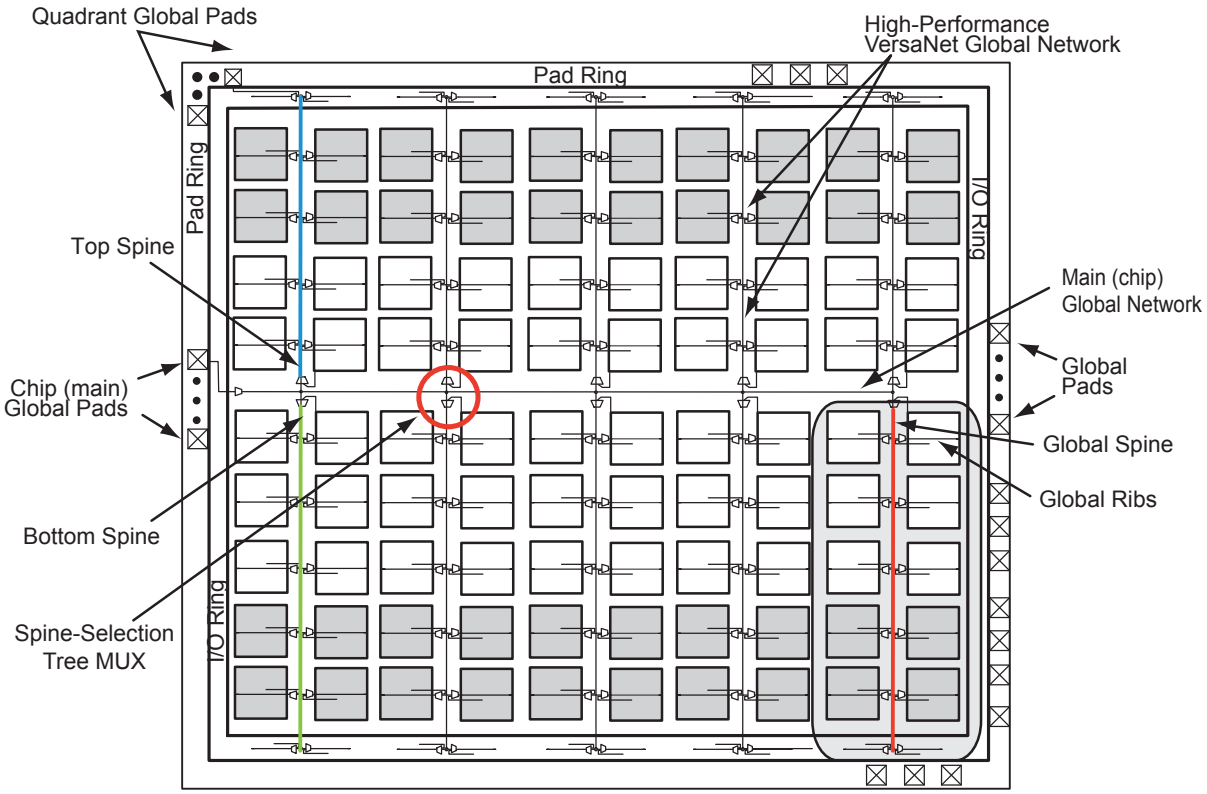
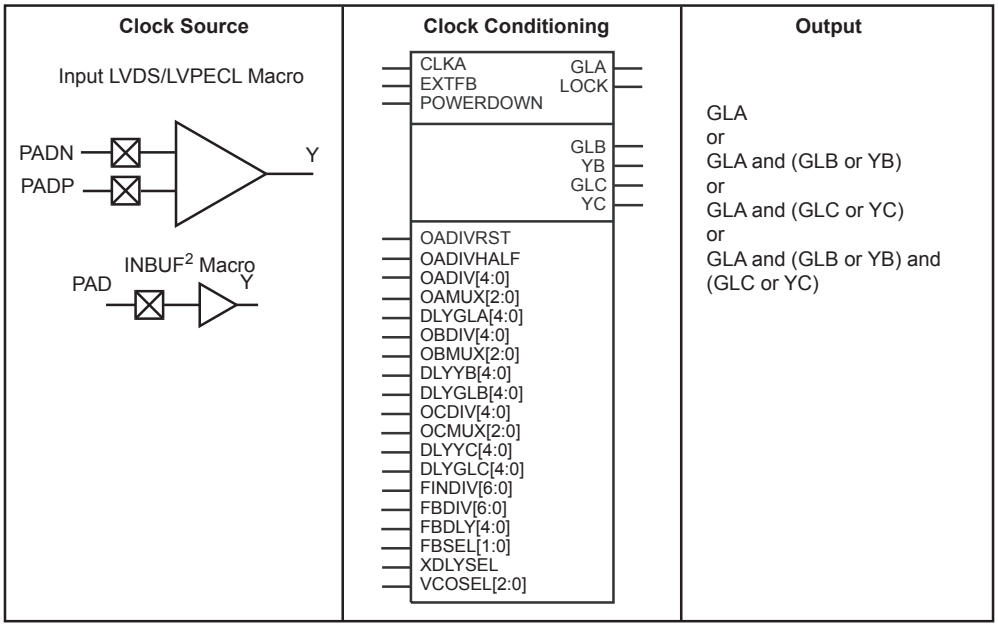


Figure 2-11 • **Overview of Fusion VersaNet Global Network**



Notes:

1. *Visit the Microsemi SoC Products Group website for future application notes concerning dynamic PLL reconfiguration. Refer to the "PLL Macro" section on page 2-27 for signal descriptions.*
2. *Many specific INBUF macros support the wide variety of single-ended and differential I/O standards for the Fusion family.*
3. *Refer to the IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide for more information.*

Figure 2-19 • **Fusion CCC Options: Global Buffers with the PLL Macro**

Table 2-10 • **Available Selections of I/O Standards within CLKBUF and CLKBUF_LVDS/LVPECL Macros**

CLKBUF Macros
CLKBUF_LVCMOS5
CLKBUF_LVCMOS33[1]
CLKBUF_LVCMOS18
CLKBUF_LVCMOS15
CLKBUF_PCI
CLKBUF_LVDS[2]
CLKBUF_LVPECL

Notes:

1. *This is the default macro. For more details, refer to the IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide.*
2. *The B-LVDS and M-LVDS standards are supported with CLKBUF_LVDS.*

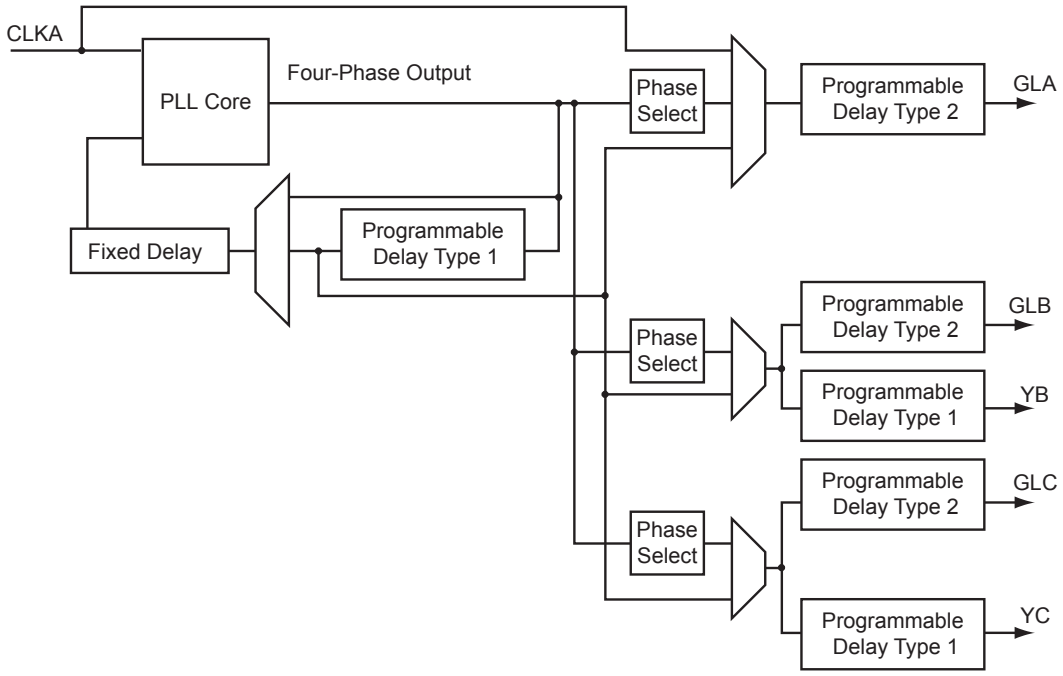
CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.

Figure 2-23 • **PLL Block**

PLL Macro

The PLL functionality of the clock conditioning block is supported by the PLL macro. Note that the PLL macro reference clock uses the CLKA input of the CCC block, which is only accessible from the global A[2:0] package pins. Refer to Figure 2-22 on page 2-25 for more information.

The PLL macro provides five derived clocks (three independent) from a single reference clock. The PLL feedback loop can be driven either internally or externally. The PLL macro also provides power-down input and lock output signals. During power-up, POWERDOWN should be asserted Low until V_{CC} is up. See Figure 2-19 on page 2-22 for more information.

Inputs:

- CLKA: selected clock input
- POWERDOWN (active low): disables PLLs. The default state is power-down on (active low).

Outputs:

- LOCK (active high): indicates that PLL output has locked on the input reference signal
- GLA, GLB, GLC: outputs to respective global networks
- YB, YC: allows output from the CCC to be routed back to the FPGA core

As previously described, the PLL allows up to five flexible and independently configurable clock outputs. Figure 2-23 on page 2-26 illustrates the various clock output options and delay elements.

As illustrated, the PLL supports three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global networks, respectively, and/or routed to the device core (YB and YC).

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

There is also a delay element in the feedback loop that can be used to advance the clock relative to the reference clock.

The PLL macro reference clock can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate it from the hardwired I/O connection described earlier.

The visual PLL configuration in SmartGen, available with the Libero SoC and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user. SmartGen allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLKA) and the derived clocks (GLA, GLB, GLC, YB, and YC). SmartGen also allows the user to select where the input clock is coming from. SmartGen automatically instantiates the special macro, PLLINT, when needed.

Access to the FB is controlled by the BUSY signal. The BUSY output is synchronous to the CLK signal. FB operations are only accepted in cycles where BUSY is logic 0.

Write Operation

Write operations are initiated with the assertion of the WEN signal. Figure 2-35 illustrates the multiple Write operations.

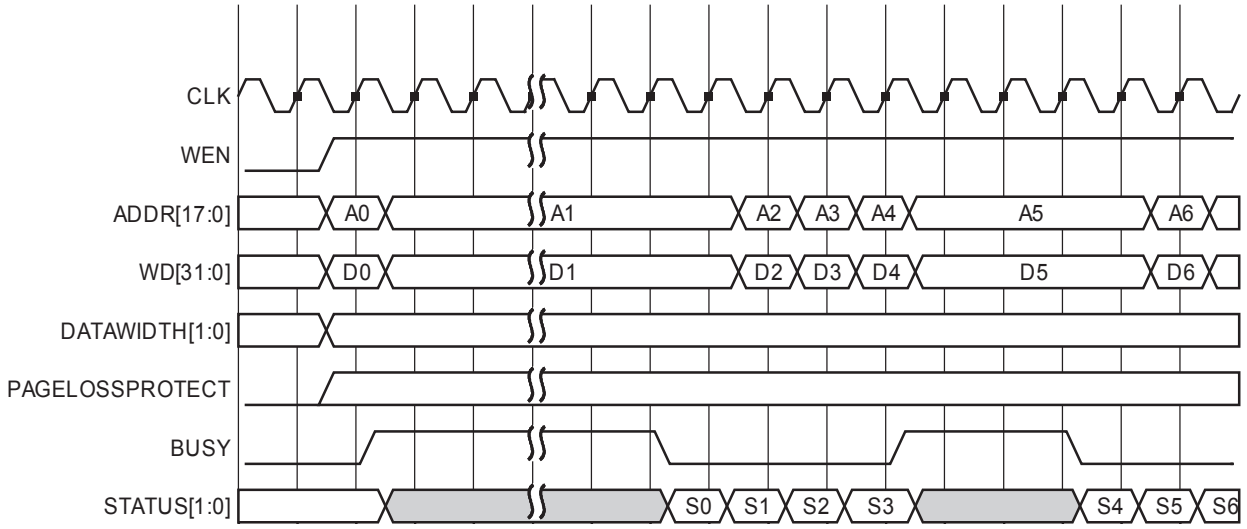


Figure 2-35 • **FB Write Waveform**

When a Write operation is initiated to a page that is currently not in the Page Buffer, the FB control logic will issue a BUSY signal to the user interface while the page is loaded from the FB Array into the Page Buffer. A Copy Page operation takes no less than 55 cycles and could take more if a Write or Unprotect Page operation is started while the NVM is busy pre-fetching a block. The basic operation is to read a block from the array into the block register (5 cycles) and then write the block register to the page buffer (1 cycle) and if necessary, when the copy is complete, reading the block being written from the page buffer into the block buffer (1 cycle). A page contains 9 blocks, so 9 blocks multiplied by 6 cycles to read/write each block, plus 1 is 55 cycles total. Subsequent writes to the same block of the page will incur no busy cycles. A write to another block in the page will assert BUSY for four cycles (five cycles when PIPE is asserted), to allow the data to be written to the Page Buffer and have the current block loaded into the Block Buffer.

Write operations are considered successful as long as the STATUS output is '00'. A non-zero STATUS indicates that an error was detected during the operation and the write was not performed. Note that the STATUS output is "sticky"; it is unchanged until another operation is started.

Only one word can be written at a time. Write word width is controlled by the DATAWIDTH bus. Users are responsible for keeping track of the contents of the Page Buffer and when to program it to the array. Just like a regular RAM, writing to random addresses is possible. Users can write into the Page Buffer in any order but will incur additional BUSY cycles. It is not necessary to modify the entire Page Buffer before saving it to nonvolatile memory.

Write errors include the following:

1. Attempting to write a page that is Overwrite Protected (STATUS = '01'). The write is not performed.
2. Attempting to write to a page that is not in the Page Buffer when Page Loss Protection is enabled (STATUS = '11'). The write is not performed.

Flash Memory Block Characteristics

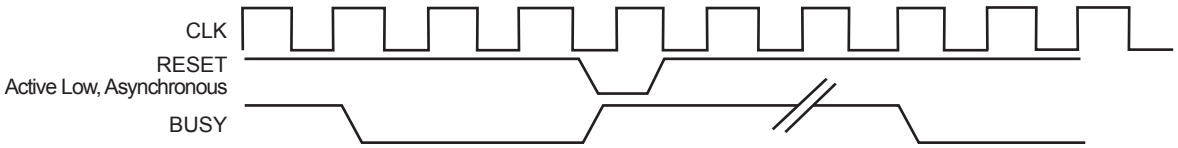


Figure 2-44 • **Reset Timing Diagram**

Table 2-24 • **Flash Memory Block Timing, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V**

Parameter	Description	–2	–1	Std.	Units
t_{CLK2RD}	Clock-to-Q in 5-cycle read mode of the Read Data	8.24	9.39	11.04	ns
	Clock-to-Q in 6-cycle read mode of the Read Data	5.10	5.81	6.83	ns
$t_{CLK2BUSY}$	Clock-to-Q in 5-cycle read mode of BUSY	5.19	5.91	6.95	ns
	Clock-to-Q in 6-cycle read mode of BUSY	4.59	5.23	6.15	ns
$t_{CLK2STATUS}$	Clock-to-Status in 5-cycle read mode	11.59	13.21	15.53	ns
	Clock-to-Status in 6-cycle read mode	4.62	5.26	6.19	ns
t_{DSUNVM}	Data Input Setup time for the Control Logic	1.98	2.26	2.65	ns
t_{DHNVM}	Data Input Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{ASUNVM}	Address Input Setup time for the Control Logic	2.84	3.24	3.81	ns
t_{AHNVM}	Address Input Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUDWNVM}$	Data Width Setup time for the Control Logic	1.91	2.17	2.56	ns
$t_{HDDWNVM}$	Data Width Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SURENNVM}$	Read Enable Setup time for the Control Logic	3.97	4.53	5.32	ns
$t_{HDRENNVM}$	Read Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUWENNVM}$	Write Enable Setup time for the Control Logic	2.44	2.78	3.27	ns
$t_{HDWENNVM}$	Write Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUPROGNVM}$	Program Setup time for the Control Logic	2.23	2.54	2.98	ns
$t_{HDPROGNVM}$	Program Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUSPAREPAGE}$	SparePage Setup time for the Control Logic	3.86	4.40	5.17	ns
$t_{HDSPAREPAGE}$	SparePage Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUAUXBLK}$	Auxiliary Block Setup Time for the Control Logic	3.85	4.39	5.16	ns
$t_{HDAUXBLK}$	Auxiliary Block Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SURDNEXT}$	ReadNext Setup Time for the Control Logic	2.23	2.54	2.99	ns
$t_{HDRDNEXT}$	ReadNext Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUERASEPG}$	Erase Page Setup Time for the Control Logic	3.87	4.41	5.19	ns
$t_{HDERASEPG}$	Erase Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUUNPROTECTPG}$	Unprotect Page Setup Time for the Control Logic	2.07	2.36	2.77	ns
$t_{HDUNPROTECTPG}$	Unprotect Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUDISCARDPG}$	Discard Page Setup Time for the Control Logic	1.94	2.21	2.60	ns
$t_{HDDISCARDPG}$	Discard Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUOVERWRPRO}$	Overwrite Protect Setup Time for the Control Logic	1.69	1.92	2.26	ns
$t_{HDOVERWRPRO}$	Overwrite Protect Hold Time for the Control Logic	0.00	0.00	0.00	ns

To initiate a current measurement, the appropriate Current Monitor Strobe (CMSTB) signal on the AB macro must be asserted low for at least t_{CMSLO} in order to discharge the previous measurement. Then CMSTB must be asserted high for at least t_{CMSET} prior to asserting the ADCSTART signal. The CMSTB must remain high until after the SAMPLE signal is deasserted by the AB macro. Note that the minimum sample time cannot be less than t_{CMSHI}. Figure 2-70 shows the timing diagram of CMSTB in relationship with the ADC control signals.

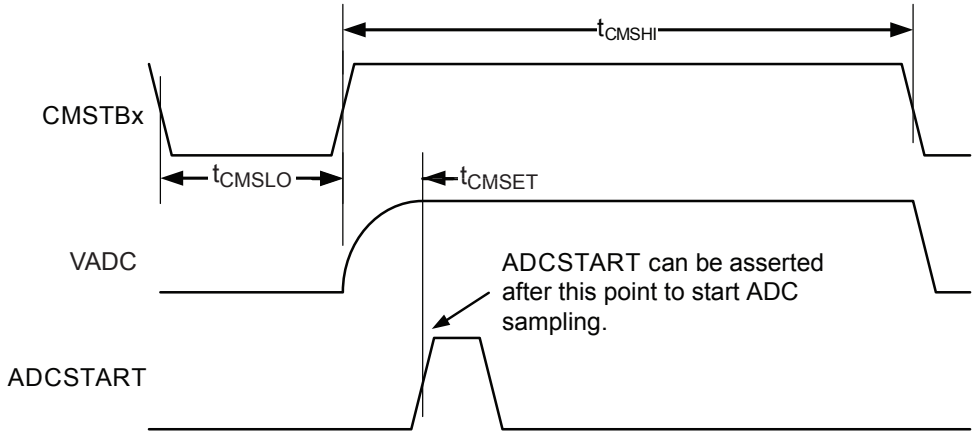


Figure 2-70 • **Timing Diagram for Current Monitor Strobe**

Figure 2-71 on page 2-88 illustrates positive current monitor operation. The differential voltage between AV and AC goes into the 10× amplifier and is then converted by the ADC. For example, a current of 1.5 A is drawn from a 10 V supply and is measured by the voltage drop across a 0.050 Ω sense resistor, The voltage drop is amplified by ten times by the amplifier and then measured by the ADC. The 1.5 A current creates a differential voltage across the sense resistor of 75 mV. This becomes 750 mV after amplification. Thus, the ADC measures a current of 1.5 A as 750 mV. Using an ADC with 8-bit resolution and VAREF of 2.56 V, the ADC result is decimal 75. EQ 3 shows how to compute the current from the ADC result.

$$|I| = (ADC \times V_{AREF}) / (10 \times 2^{N} \times R_{sense})$$

EQ 3

where

I is the current flowing through the sense resistor

ADC is the result from the ADC

VAREF is the Reference voltage

N is the number of bits

Rsense is the resistance of the sense resistor

C_{GS} is not a fixed capacitance but, depending on the circuitry connected to its drain terminal, can vary significantly during the course of a turn-on or turn-off transient. Thus, EQ 6 on page 2-90 can only be used for a first-order estimate of the switching speed of the external MOSFET.

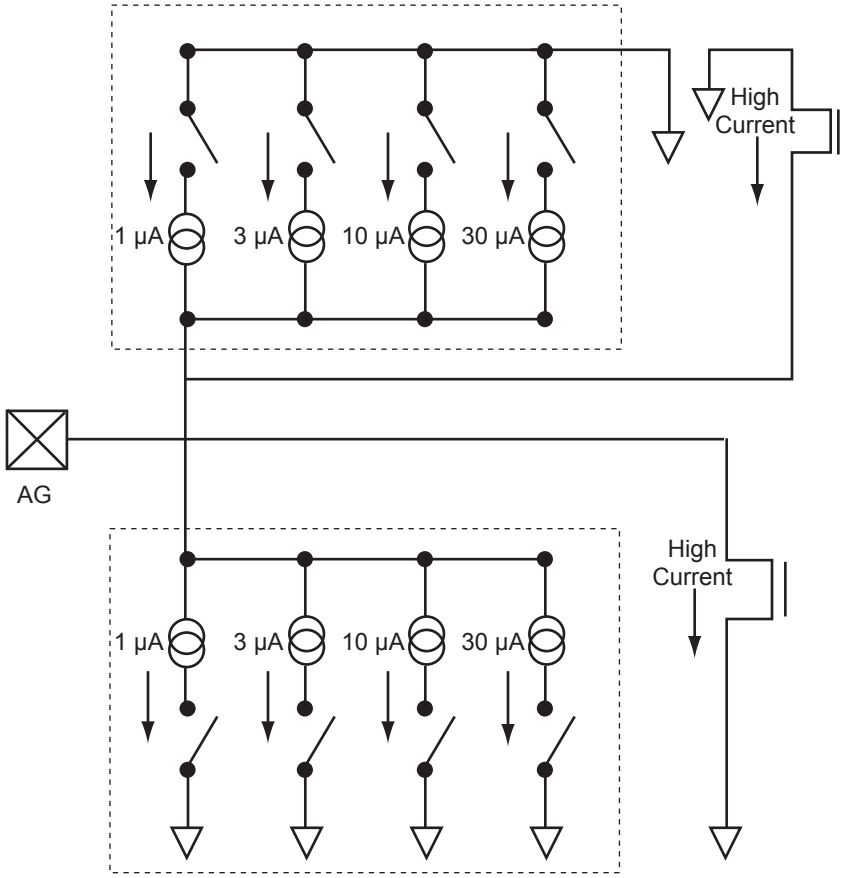


Figure 2-74 • **Gate Driver Example**

Features Supported on Pro I/Os

Table 2-72 lists all features supported by transmitter/receiver for single-ended and differential I/Os.

Table 2-72 • **Fusion Pro I/O Features**

Feature	Description
Single-ended and voltage-referenced transmitter features	• Hot insertion in every mode except PCI or 5 V input tolerant (these modes use clamp diodes and do not allow hot insertion) • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os. • Weak pull-up and pull-down • Two slew rates • Skew between output buffer enable/disable time: 2 ns delay (rising edge) and 0 ns delay (falling edge); see "Selectable Skew between Output Buffer Enable/Disable Time" on page 2-150 for more information • Five drive strengths • 5 V–tolerant receiver ("5 V Input Tolerance" section on page 2-145) • LVTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs ("5 V Output Tolerance" section on page 2-149) • High performance (Table 2-77 on page 2-144)
Single-ended receiver features	• Schmitt trigger option • ESD protection • Programmable delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V) • High performance (Table 2-77 on page 2-144) • Separate ground planes, GND/GNDQ, for input buffers only to avoid output-induced noise in the input circuitry
Voltage-referenced differential receiver features	• Programmable Delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V) • High performance (Table 2-77 on page 2-144) • Separate ground planes, GND/GNDQ, for input buffers only to avoid output-induced noise in the input circuitry
CMOS-style LVDS, B-LVDS, M-LVDS, or LVPECL transmitter	• Two I/Os and external resistors are used to provide a CMOS-style LVDS, B-LVDS, M-LVDS, or LVPECL transmitter solution. • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os. • Weak pull-up and pull-down • Fast slew rate
LVDS/LVPECL differential receiver features	• ESD protection • High performance (Table 2-77 on page 2-144) • Programmable delay: 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V) • Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry

Double Data Rate (DDR) Support

Fusion Pro I/Os support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making it very efficient for implementing very high-speed systems.

DDR interfaces can be implemented using HSTL, SSTL, LVDS, and LVPECL I/O standards. In addition, high-speed DDR interfaces can be implemented using LVDS I/O.

Input Support for DDR

The basic structure to support a DDR input is shown in Figure 2-100. Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock.

Each I/O tile on Fusion devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in Figure 2-101 on page 2-141. New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

Refer to the application note *Using DDR for Fusion Devices* for more information.

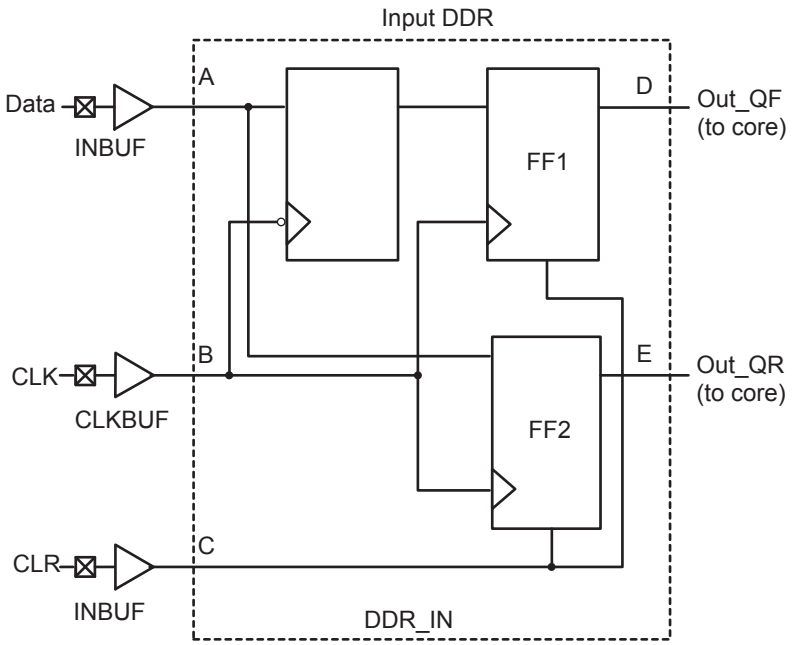


***Figure 2-100* • DDR Input Register Support in Fusion Devices**

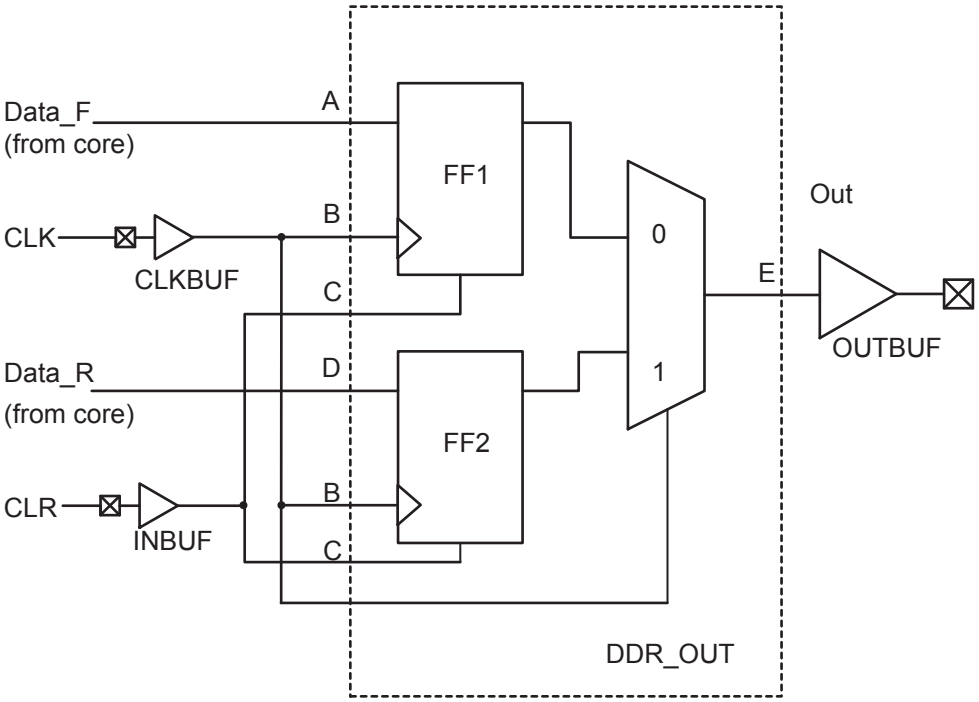


***Figure 2-101* • DDR Output Support in Fusion Devices**

User I/O Characteristics

Timing Model

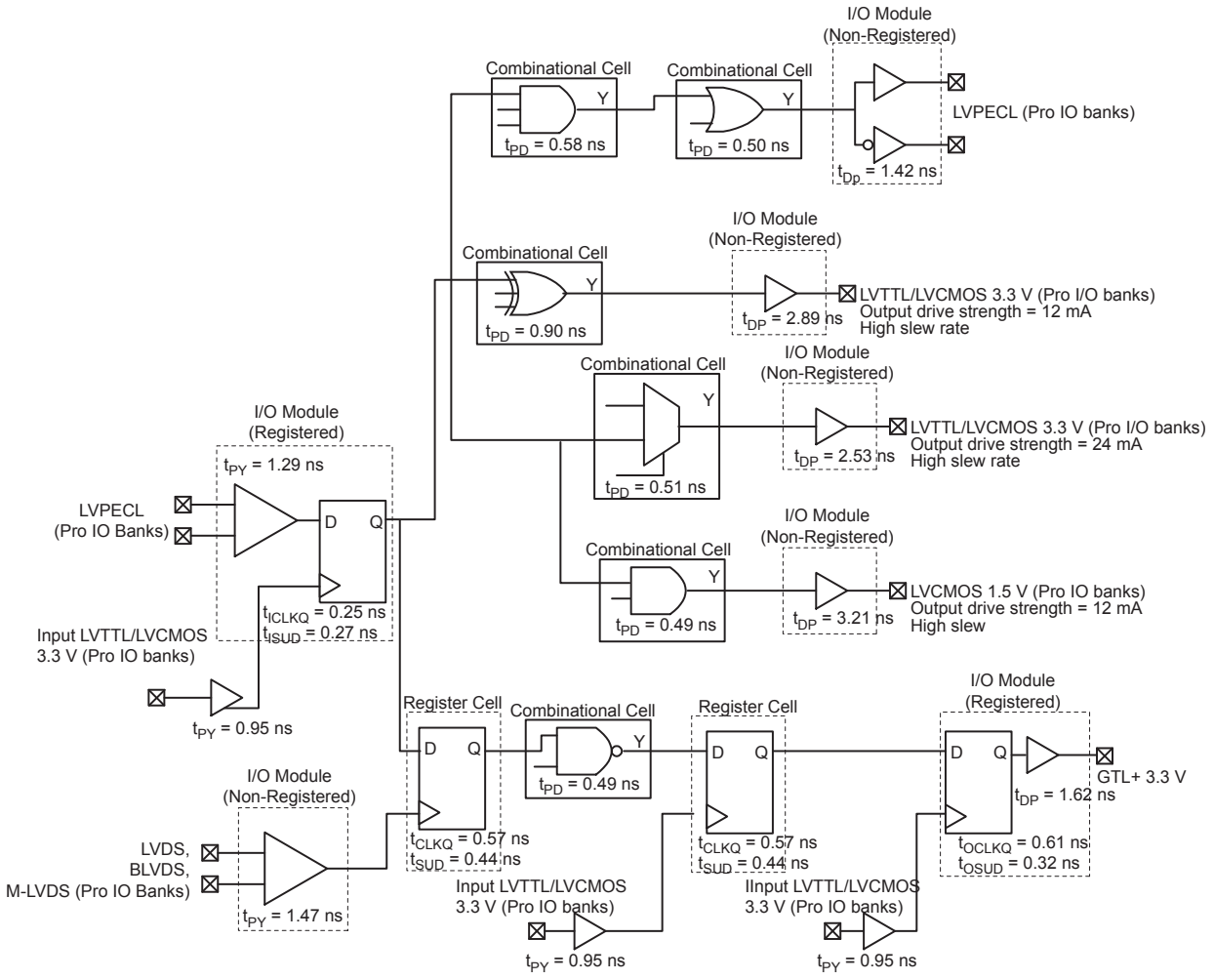


Figure 2-113 • **Timing Model**
Operating Conditions: –2 Speed, Extended Temperature Range (T_J = 100°C),
Worst-Case VCC = 1.425 V

Timing Characteristics

Table 2-107 • 2.5 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	12.66	0.05	1.59	1.75	0.44	12.89	12.24	2.87	2.32	15.25	14.60	ns
	–1	0.58	10.77	0.04	1.36	1.49	0.38	10.97	10.42	2.44	1.97	12.97	12.42	ns
	–2	0.51	9.45	0.03	1.19	1.31	0.33	9.63	9.14	2.14	1.73	11.39	10.90	ns
8 mA	Std.	0.68	9.21	0.05	1.59	1.75	0.44	9.38	8.45	3.27	3.09	11.74	10.81	ns
	–1	0.58	7.83	0.04	1.36	1.49	0.38	7.98	7.19	2.78	2.63	9.98	9.19	ns
	–2	0.51	6.88	0.03	1.19	1.31	0.33	7.00	6.31	2.44	2.31	8.76	8.07	ns
12 mA	Std.	0.68	7.14	0.05	1.59	1.75	0.44	7.28	6.44	3.55	3.58	9.63	8.80	ns
	–1	0.58	6.08	0.04	1.36	1.49	0.38	6.19	5.48	3.02	3.04	8.20	7.48	ns
	–2	0.51	5.33	0.03	1.19	1.31	0.33	5.43	4.81	2.65	2.67	7.19	6.57	ns
16 mA	Std.	0.68	6.65	0.05	1.59	1.75	0.44	6.77	6.04	3.61	3.71	9.13	8.40	ns
	–1	0.58	5.66	0.04	1.36	1.49	0.38	5.76	5.14	3.07	3.16	7.77	7.14	ns
	–2	0.51	4.97	0.03	1.19	1.31	0.33	5.06	4.51	2.69	2.77	6.82	6.27	ns
24 mA	Std.	0.68	6.25	0.05	1.59	1.75	0.44	6.37	6.02	3.69	4.22	8.73	8.37	ns
	–1	0.58	5.32	0.04	1.36	1.49	0.38	5.42	5.12	3.14	3.59	7.43	7.12	ns
	–2	0.51	4.67	0.03	1.19	1.31	0.33	4.76	4.49	2.75	3.15	6.52	6.25	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-122 • 1.5 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	9.00	0.05	1.79	0.44	7.20	8.82	3.57	2.92	9.55	11.18	ns
	–1	0.58	7.65	0.04	1.52	0.38	6.12	7.50	3.04	2.48	8.13	9.51	ns
	–2	0.51	6.72	0.03	1.34	0.33	5.37	6.59	2.67	2.18	7.13	8.35	ns
4 mA	Std.	0.68	5.71	0.05	1.79	0.44	5.11	5.60	3.94	3.59	7.47	7.96	ns
	–1	0.58	4.85	0.04	1.52	0.38	4.35	4.77	3.36	3.05	6.36	6.77	ns
	–2	0.51	4.26	0.03	1.34	0.33	3.82	4.18	2.95	2.68	5.58	5.95	ns
6 mA	Std.	0.68	5.07	0.05	1.79	0.44	4.80	4.92	4.03	3.76	7.15	7.28	ns
	–1	0.58	4.31	0.04	1.52	0.38	4.08	4.19	3.43	3.20	6.09	6.19	ns
	–2	0.51	3.78	0.03	1.34	0.33	3.58	3.68	3.01	2.81	5.34	5.44	ns
8 mA	Std.	0.68	4.66	0.05	1.79	0.44	4.38	3.77	4.16	4.43	6.74	6.13	ns
	–1	0.58	3.96	0.04	1.52	0.38	3.73	3.21	3.54	3.77	5.73	5.21	ns
	–2	0.51	3.48	0.03	1.34	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns
12 mA	Std.	0.68	4.66	0.05	1.79	0.44	4.38	3.77	4.16	4.43	6.74	6.13	ns
	–1	0.58	3.96	0.04	1.52	0.38	3.73	3.21	3.54	3.77	5.73	5.21	ns
	–2	0.51	3.48	0.03	1.34	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-139 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
8 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8	39	32	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

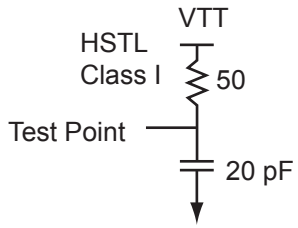


Figure 2-126 • AC Loading

Table 2-140 • HSTL Class I AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

*Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

Table 2-141 • HSTL Class I
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	3.25	0.05	2.24	0.44	3.41	3.31			5.77	5.67	ns
–1	0.58	2.85	0.04	1.91	0.38	2.90	2.82			4.91	4.83	ns
–2	0.51	2.50	0.03	1.67	0.33	2.55	2.48			4.31	4.24	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

θ_{JA} = 19.00°C/W (taken from Table 3-6 on page 3-8).

T_A = 75.00°C

$$\text{Maximum Power Allowed} = \frac{100.00°C - 75.00°C}{19.00°C/W} = 1.3\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

T_J = 100.00°C

T_A = 70.00°C

From the datasheet:

θ_{JA} = 17.00°C/W

θ_{JC} = 8.28°C/W

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{17.00\ W} = 1.76\ W$$

EQ 6

Sequential Cells Dynamic Contribution—$P_{S\text{-}CELL}$

Operating Mode

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + (\alpha_1 / 2) * PAC6) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-14 on page 3-23.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$P_{S\text{-}CELL} = 0$ W

Combinatorial Cells Dynamic Contribution—$P_{C\text{-}CELL}$

Operating Mode

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * PAC7 * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-14 on page 3-23.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$P_{C\text{-}CELL} = 0$ W

Routing Net Dynamic Contribution—P_{NET}

Operating Mode

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-14 on page 3-23.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$P_{NET} = 0$ W

I/O Input Buffer Dynamic Contribution—P_{INPUTS}

Operating Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * PAC9 * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-14 on page 3-23.

F_{CLK} is the global clock signal frequency.

Standby Mode and Sleep Mode

$P_{INPUTS} = 0$ W

I/O Output Buffer Dynamic Contribution—$P_{OUTPUTS}$

Operating Mode

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-14 on page 3-23.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 3-15 on page 3-23.

F_{CLK} is the global clock signal frequency.

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51700117-2/01.13