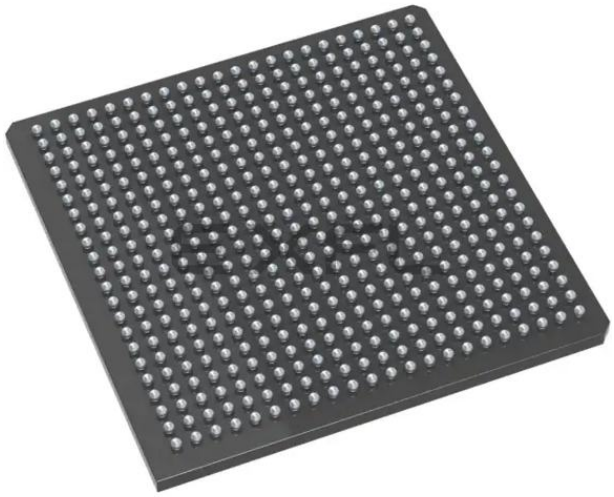


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	172
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-fg484k

Instant On

Flash-based Fusion devices are Level 0 Instant On. Instant On Fusion devices greatly simplify total system design and reduce total system cost by eliminating the need for CPLDs. The Fusion Instant On clocking (PLLs) replaces off-chip clocking resources. The Fusion mix of Instant On clocking and analog resources makes these devices an excellent choice for both system supervisor and system management functions. Instant On from a single 3.3 V source enables Fusion devices to initiate, control, and monitor multiple voltage supplies while also providing system clocks. In addition, glitches and brownouts in system power will not corrupt the Fusion device flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design. Flash-based Fusion devices simplify total system design and reduce cost and design risk, while increasing system reliability.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. Another source of radiation-induced firm errors is alpha particles. For an alpha to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in Fusion flash-based FPGAs. Once it is programmed, the flash cell configuration element of Fusion FPGAs cannot be altered by high-energy neutrons and is therefore immune to errors from them.

Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Fusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With Fusion devices, there is no power-on current surge and no high current transition, both of which occur on many FPGAs.

Fusion devices also have low dynamic power consumption and support both low power standby mode and very low power sleep mode, offering further power savings.

Advanced Flash Technology

The Fusion family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows very high logic utilization (much higher than competing SRAM technologies) without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary Fusion architecture provides granularity comparable to standard-cell ASICs. The Fusion device consists of several distinct and programmable architectural features, including the following (Figure 1-1 on page 1-5):

- Embedded memories
  - Flash memory blocks
  - FlashROM
  - SRAM and FIFO

Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

Z -Tristate: I/O is tristated

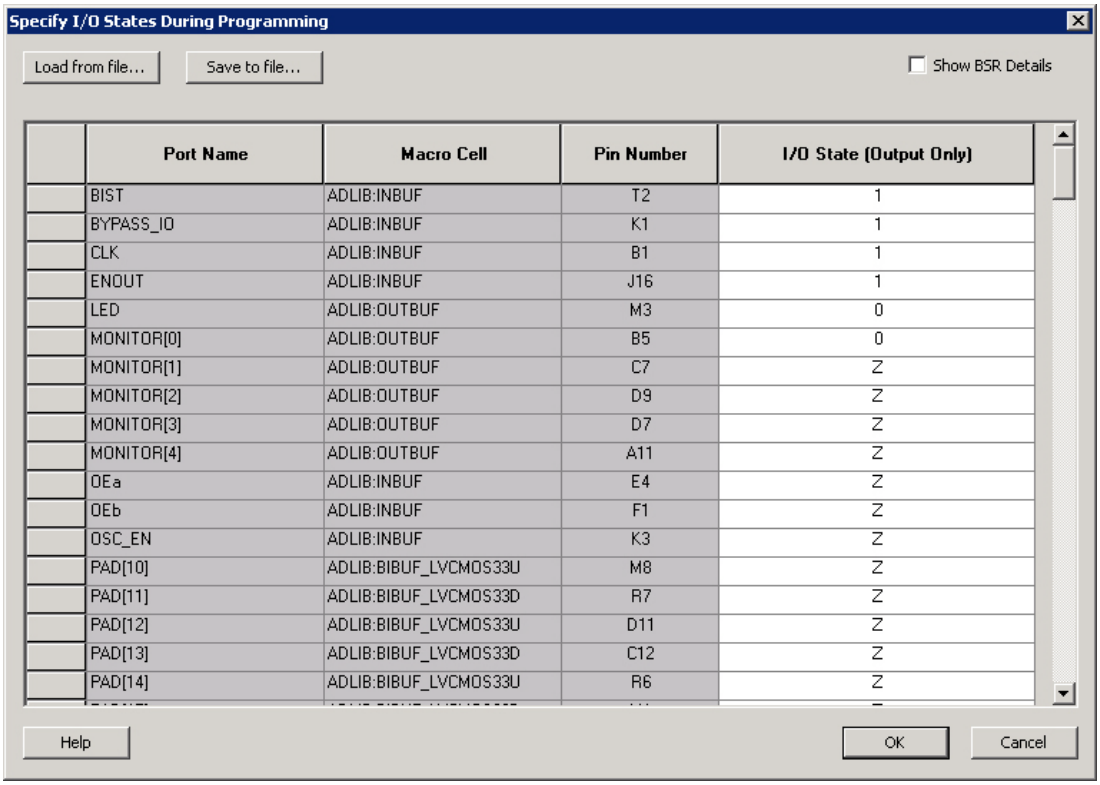


Figure 1-3 • **I/O States During Programming Window**

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

The system application, Level 3, is the larger user application that utilizes one or more applets. Designing at the highest level of abstraction supported by the Fusion technology stack, the application can be easily created in FPGA gates by importing and configuring multiple applets.

In fact, in some cases an entire FPGA system design can be created without any HDL coding.

An optional MCU enables a combination of software and HDL-based design methodologies. The MCU can be on-chip or off-chip as system requirements dictate. System portioning is very flexible, allowing the MCU to reside above the applets or to absorb applets, or applets and backbone, if desired.

The Fusion technology stack enables a very flexible design environment. Users can engage in design across a continuum of abstraction from very low to very high.

Core Architecture

VersaTile

Based upon successful ProASIC3/E logic architecture, Fusion devices provide granularity comparable to gate arrays. The Fusion device core consists of a sea-of-VersaTiles architecture.

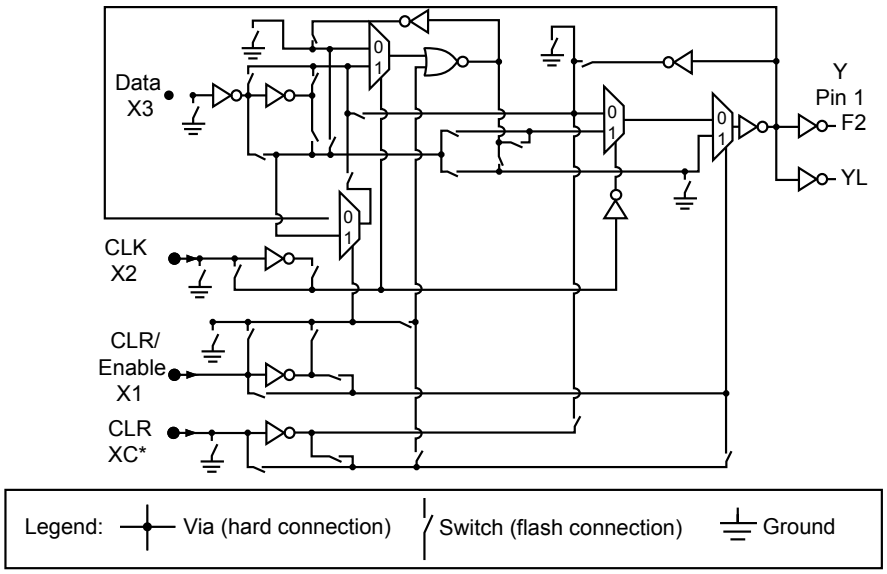
As illustrated in Figure 2-2, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a 4th input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR signal is supported by a fourth input, which can only be routed to the core cell over the VersaNet (global) network.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources (Figure 2-2).



*Note: *This input can only be connected to the global clock distribution network.*

Figure 2-2 • **Fusion Core VersaTile**

Read Operation

Read operations are designed to read data from the FB Array, Page Buffer, Block Buffer, or status registers. Read operations support a normal read and a read-ahead mode (done by asserting READNEXT). Also, the timing for Read operations is dependent on the setting of PIPE.

The following diagrams illustrate representative timing for Non-Pipe Mode (Figure 2-38) and Pipe Mode (Figure 2-39) reads of the flash memory block interface.

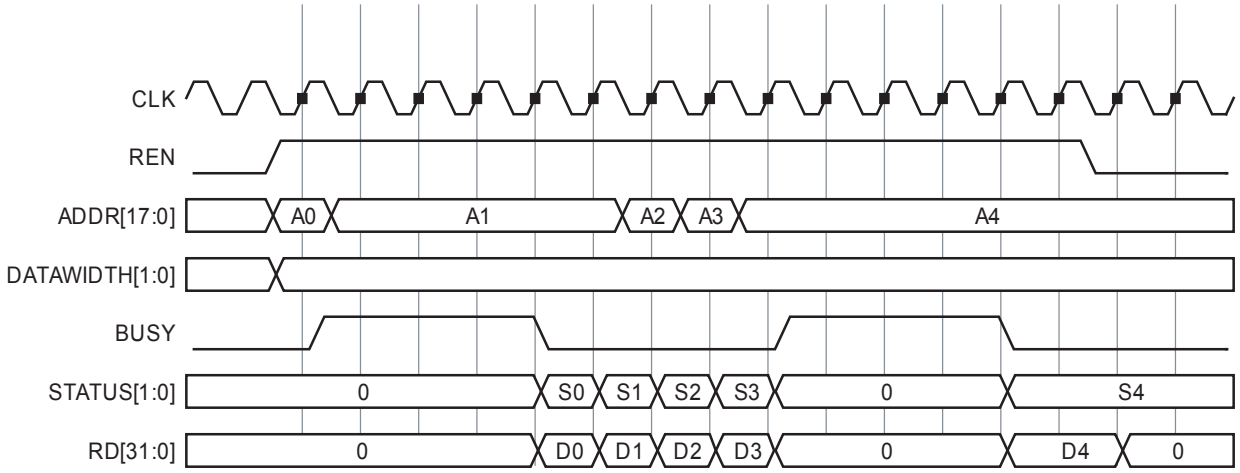


Figure 2-38 • **Read Waveform (Non-Pipe Mode, 32-bit access)**

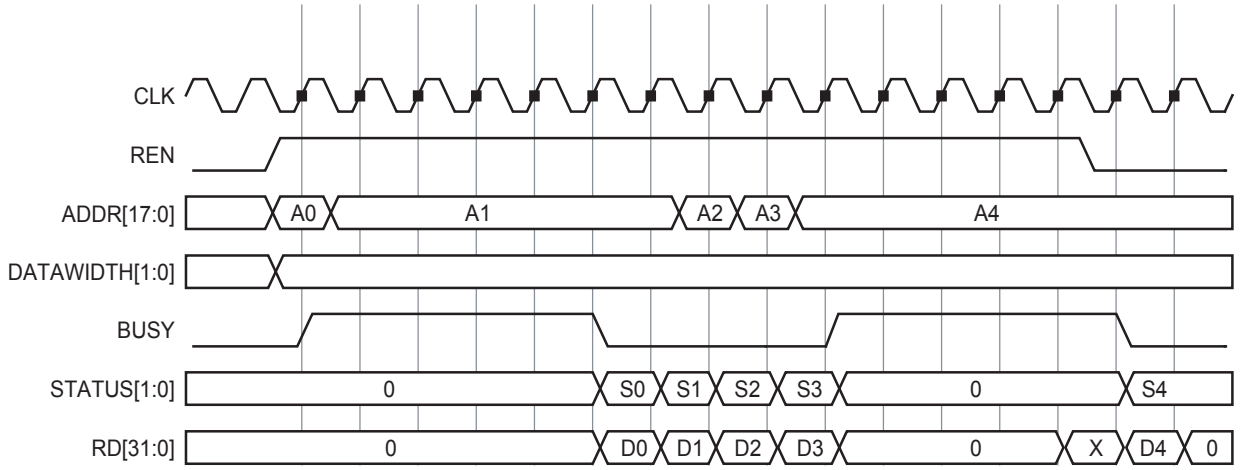


Figure 2-39 • **Read Waveform (Pipe Mode, 32-bit access)**

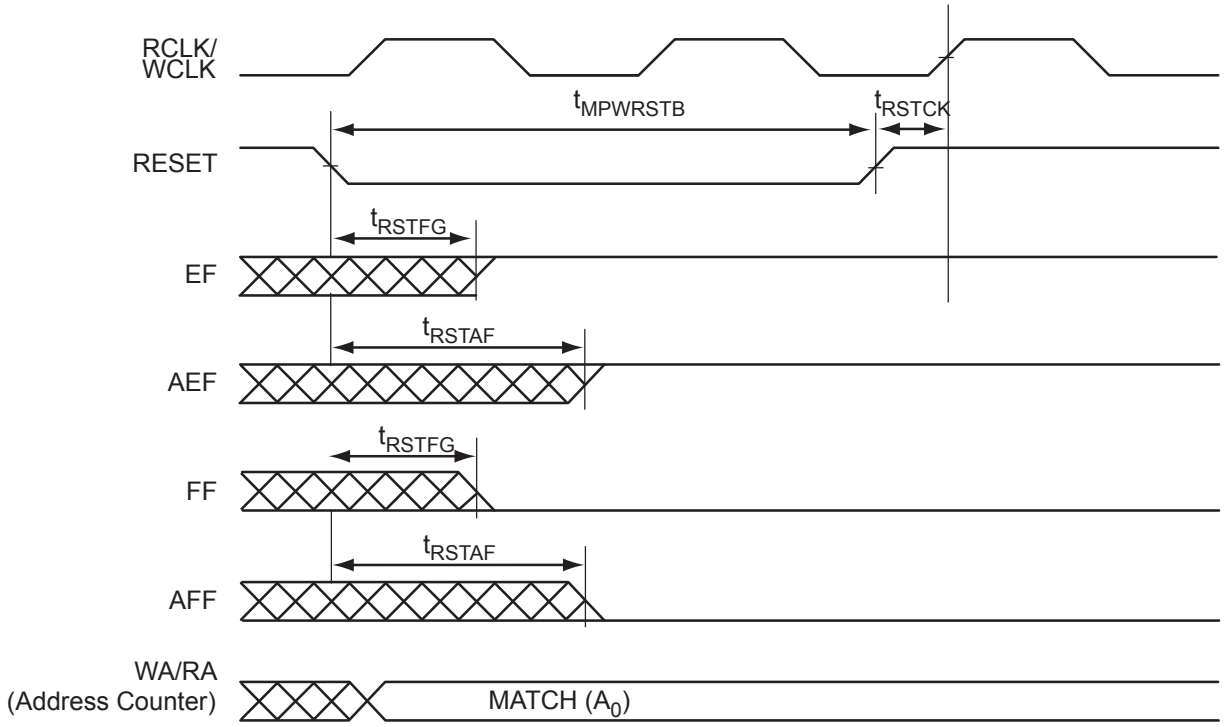


Figure 2-58 • **FIFO Reset**

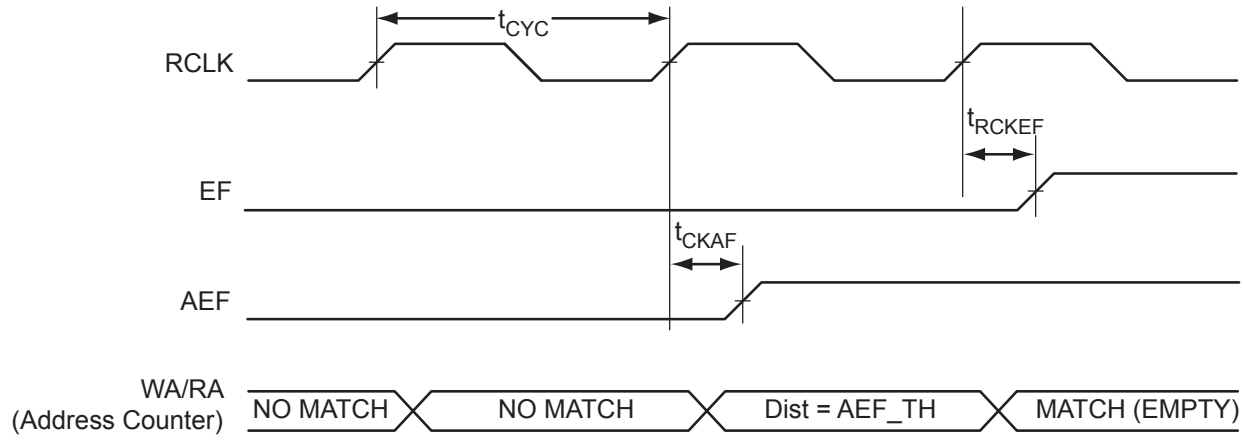


Figure 2-59 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

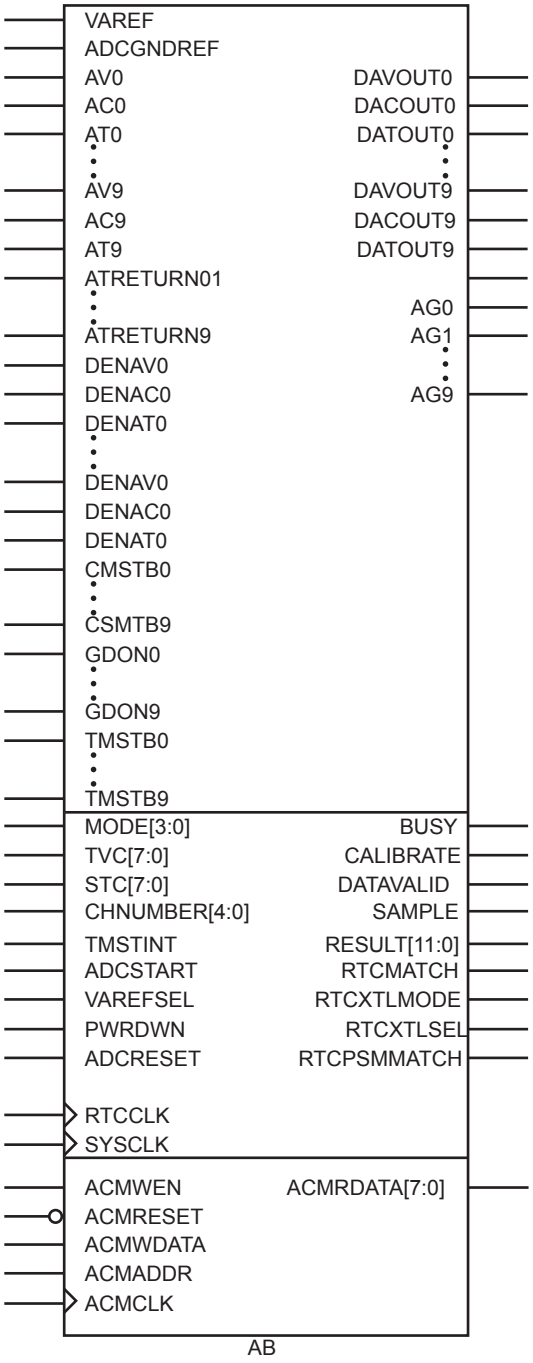


Figure 2-63 • **Analog Block Macro**

Analog-to-Digital Converter Block

At the heart of the Fusion analog system is a programmable Successive Approximation Register (SAR) ADC. The ADC can support 8-, 10-, or 12-bit modes of operation. In 12-bit mode, the ADC can resolve 500 ksps. All results are MSB-justified in the ADC. The input to the ADC is a large 32:1 analog input multiplexer. A simplified block diagram of the Analog Quads, analog input multiplexer, and ADC is shown in Figure 2-78 on page 2-96. The ADC offers multiple self-calibrating modes to ensure consistent high performance both at power-up and during runtime.

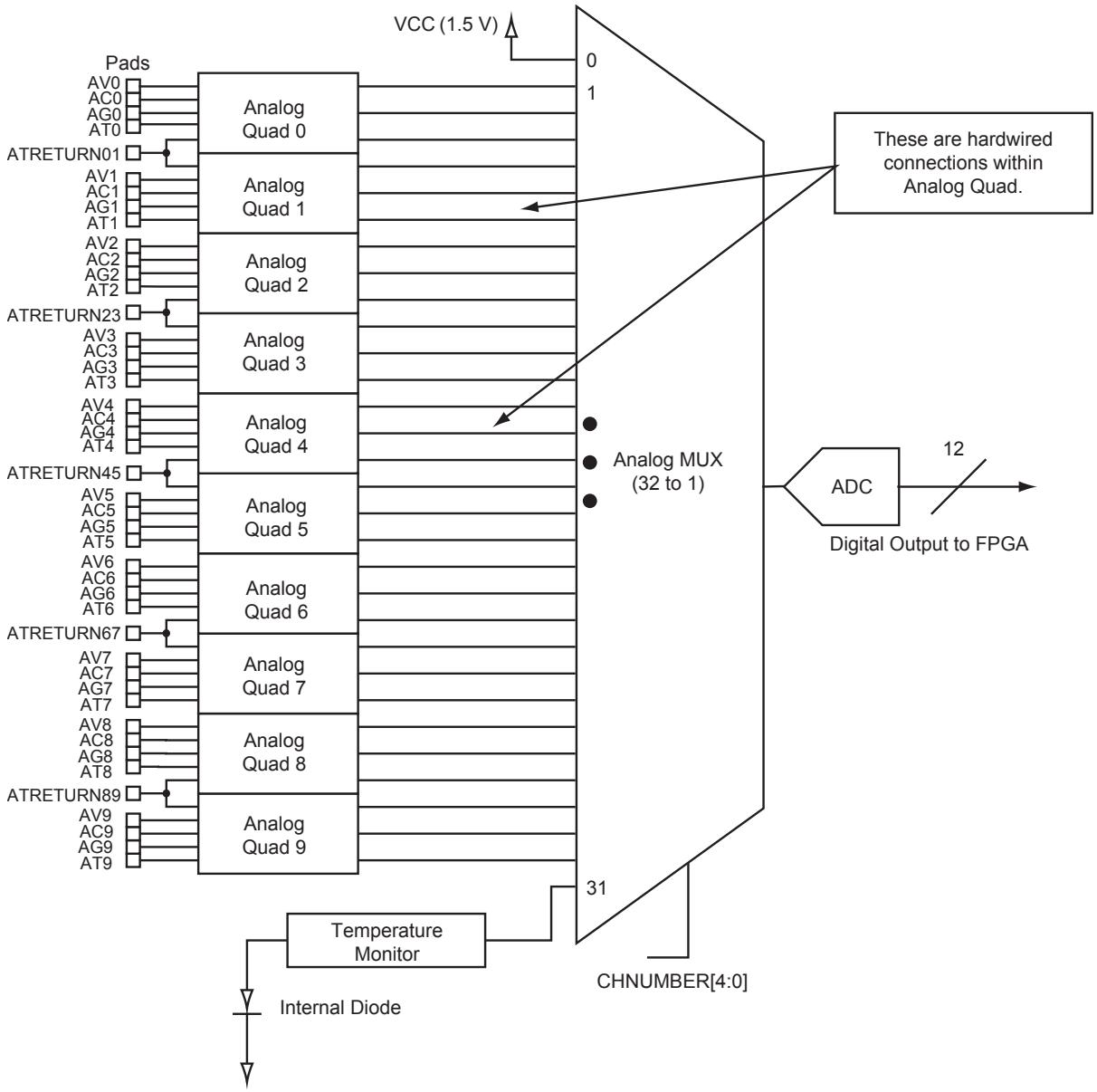


Figure 2-78 • **ADC Block Diagram**

TUE – Total Unadjusted Error

TUE is a comprehensive specification that includes linearity errors, gain error, and offset error. It is the worst-case deviation from the ideal device performance. TUE is a static specification (Figure 2-86).

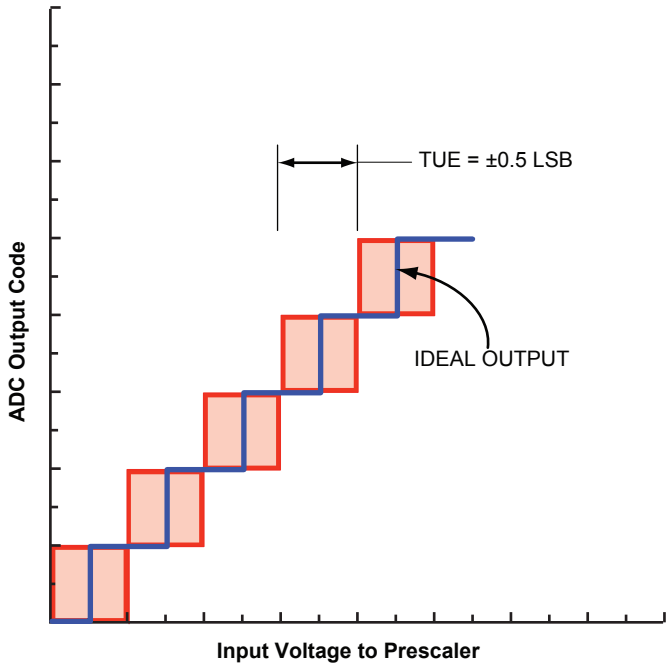


***Figure 2-86* • Total Unadjusted Error (TUE)**

ADC Operation

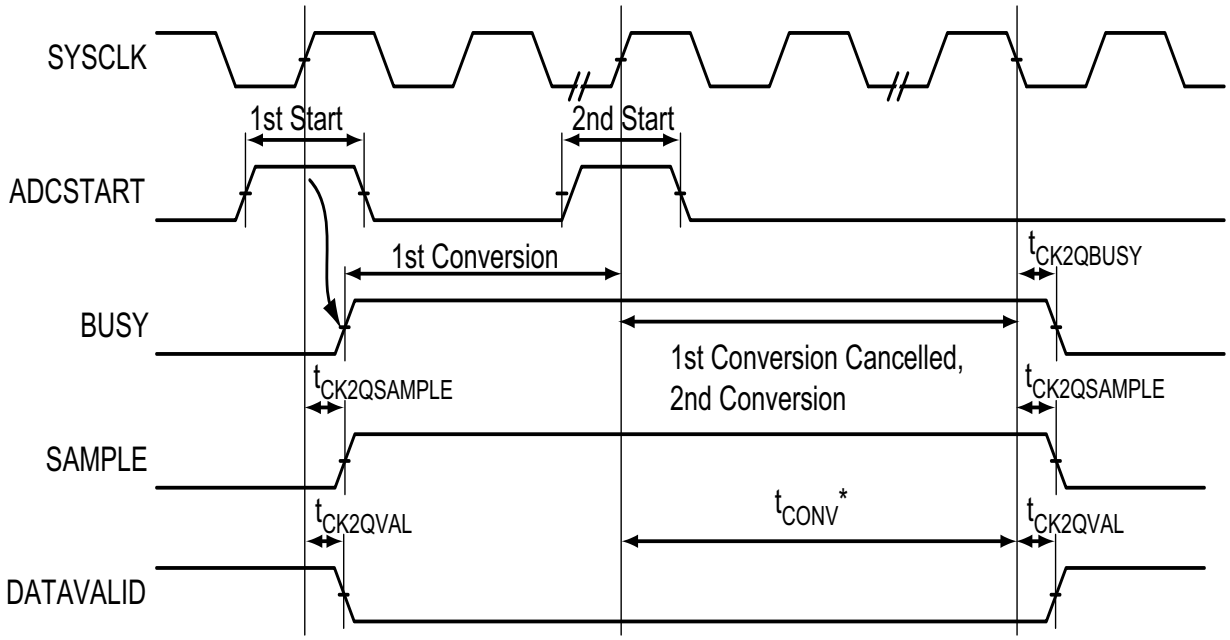
Once the ADC has powered up and been released from reset, ADCRESET, the ADC will initiate a calibration routine designed to provide optimal ADC performance. The Fusion ADC offers a robust calibration scheme to reduce integrated offset and linearity errors. The offset and linearity errors of the main capacitor array are compensated for with an 8-bit calibration capacitor array. The offset/linearity error calibration is carried out in two ways. First, a power-up calibration is carried out when the ADC comes out of reset. This is initiated by the CALIBRATE output of the Analog Block macro and is a fixed number of ADC_CLK cycles (3,840 cycles), as shown in Figure 2-88 on page 2-111. In this mode, the linearity and offset errors of the capacitors are calibrated.

To further compensate for drift and temperature-dependent effects, every conversion is followed by post-calibration of either the offset or a bit of the main capacitor array. The post-calibration ensures that, over time and with temperature, the ADC remains consistent.

After both calibration and the setting of the appropriate configurations, as explained above, the ADC is ready for operation. Setting the ADCSTART signal high for one clock period will initiate the sample and conversion of the analog signal on the channel as configured by CHNUMBER[4:0]. The status signals SAMPLE and BUSY will show when the ADC is sampling and converting (Figure 2-90 on page 2-112). Both SAMPLE and BUSY will initially go high. After the ADC has sampled and held the analog signal, SAMPLE will go low. After the entire operation has completed and the analog signal is converted, BUSY will go low and DATAVALID will go high. This indicates that the digital result is available on the RESULT[11:0] pins.

DATAVALID will remain high until a subsequent ADC_START is issued. The DATAVALID goes low on the rising edge of SYSCLK, as shown in Figure 2-89 on page 2-111. The RESULT signals will be kept constant until the ADC finishes the subsequent sample. The next sampled RESULT will be available when DATAVALID goes high again. It is ideal to read the RESULT when DATAVALID is '1'. The RESULT is latched and remains unchanged until the next DATAVLAID rising edge.

Injected Conversion



*Note: * See EQ 23 on page 2-109 for calculation on the conversion time, t_{CONV}.*

Figure 2-92 • **Injected-Conversion Timing Diagram**

Table 2-68 • I/O Bank Support by Device

I/O Bank	AFS600	AFS1500
Advanced I/O	E, W	E, W
Pro I/O	N	N
Analog Quad	S	S

Note: E = East side of the device
W = West side of the device
N = North side of the device
S = South side of the device

Table 2-69 • Fusion VCCI Voltages and Compatible Standards

VCCI (typical)	Compatible Standards
3.3 V	LVTTL/LVCMOS 3.3, PCI 3.3, SSTL3 (Class I and II),* GTL+ 3.3, GTL 3.3,* LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, SSTL2 (Class I and II),* GTL+ 2.5,* GTL 2.5,* LVDS, B-LVDS, M-LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5, HSTL (Class I),* HSTL (Class II)*

*Note: *I/O standard supported by Pro I/O banks.*

Table 2-70 • Fusion VREF Voltages and Compatible Standards*

VREF (typical)	Compatible Standards
1.5 V	SSTL3 (Class I and II)
1.25 V	SSTL2 (Class I and II)
1.0 V	GTL+ 2.5, GTL+ 3.3
0.8 V	GTL 2.5, GTL 3.3
0.75 V	HSTL (Class I), HSTL (Class II)

*Note: *I/O standards supported by Pro I/O banks.*

Double Data Rate (DDR) Support

Fusion Pro I/Os support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making it very efficient for implementing very high-speed systems.

DDR interfaces can be implemented using HSTL, SSTL, LVDS, and LVPECL I/O standards. In addition, high-speed DDR interfaces can be implemented using LVDS I/O.

Input Support for DDR

The basic structure to support a DDR input is shown in Figure 2-100. Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock.

Each I/O tile on Fusion devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in Figure 2-101 on page 2-141. New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

Refer to the application note *Using DDR for Fusion Devices* for more information.

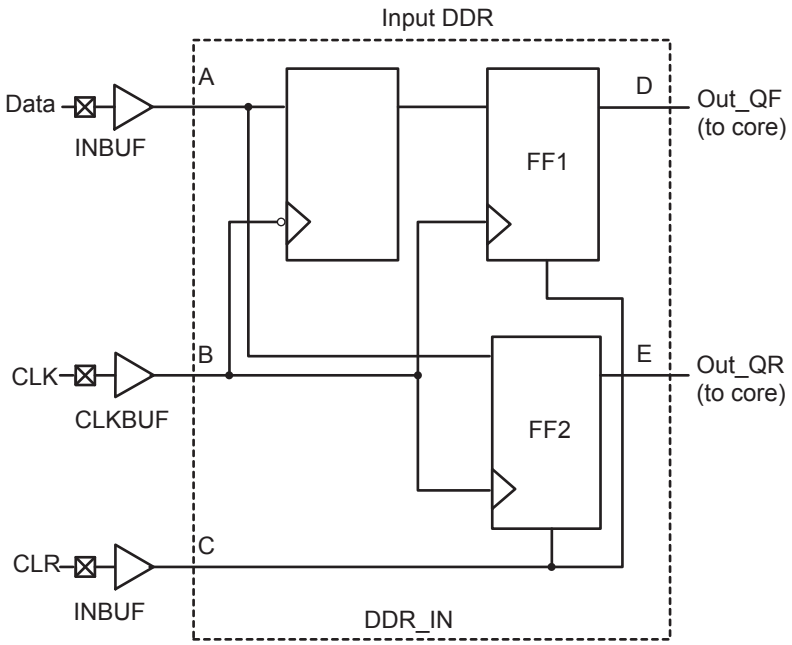


***Figure 2-100* • DDR Input Register Support in Fusion Devices**

Table 2-91 • Summary of I/O Timing Characteristics – Software Default Settings, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI as Per Configuration Applicable to Pro I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTL/ 3.3 V LVCMOS	12 mA	High	35	–	0.51	2.89	0.03	0.95	1.23	0.33	2.94	2.26	2.58	2.85	4.70	4.02	ns
2.5 V LVCMOS	12 mA	High	35	–	0.51	2.95	0.03	1.19	1.31	0.33	3.00	2.75	2.65	2.75	4.76	4.51	ns
1.8 V LVCMOS	12 mA	High	35	–	0.51	2.99	0.03	1.14	1.50	0.33	2.83	2.40	2.91	3.21	4.60	4.16	ns
1.5 V LVCMOS	12 mA	High	35	–	0.51	3.21	0.03	1.13	1.69	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns
3.3 V PCI	Per PCI spec	High	10	25 [2]	0.51	2.21	0.03	0.83	1.32	0.33	2.25	1.57	2.58	2.85	4.01	3.33	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 [2]	0.51	2.21	0.03	0.81	1.24	0.33	2.25	1.57	2.58	2.85	4.01	3.33	ns
3.3 V GTL	20 mA	High	10	25	0.51	1.63	0.03	2.31	–	0.33	1.60	1.63			3.36	3.40	ns
2.5 V GTL	20 mA	High	10	25	0.51	1.68	0.03	1.93	–	0.33	1.70	1.68			3.46	3.44	ns
3.3 V GTL+	35 mA	High	10	25	0.51	1.62	0.03	1.25	–	0.33	1.65	1.62			3.41	3.38	ns
2.5 V GTL+	33mA	High	10	25	0.51	1.74	0.03	1.19	–	0.33	1.77	1.65			3.53	3.41	ns
HSTL (I)	8 mA	High	20	50	0.51	2.50	0.03	1.67	–	0.33	2.55	2.48			4.31	4.24	ns
HSTL (II)	15 mA	High	20	25	0.51	2.38	0.03	1.67	–	0.33	2.43	2.14			4.19	3.90	ns
SSTL2 (I)	17 mA	High	30	50	0.51	1.68	0.03	1.05	–	0.33	1.71	1.45			3.47	3.22	ns
SSTL2 (II)	21 mA	High	30	25	0.51	1.71	0.03	1.05	–	0.33	1.74	1.39			3.50	3.15	ns
SSTL3 (I)	16 mA	High	30	50	0.51	1.82	0.03	0.99	–	0.33	1.85	1.45			3.61	3.21	ns
SSTL3 (II)	24 mA	High	30	25	0.51	1.63	0.03	0.99	–	0.33	1.66	1.32			3.42	3.08	ns
LVDS	24 mA	High	–	–	0.51	1.48	0.03	1.47	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.51	1.42	0.03	1.29	–	–	–	–	–	–	–	–	ns

Notes:

1. *For the derating values at specific junction temperature and voltage-supply levels, refer to Table 3-7 on page 3-10.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-100 on page 2-140 for connectivity. This resistor is not required during normal operation.*

Table 2-94 • I/O Output Buffer Maximum Resistances [1] (continued)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (ohms) [2]	$R_{PULL\text{-}UP}$ (ohms) [3]
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: www.microsemi.com/soc/techdocs/models/ibis.html.*
2. *R(PULL-DOWN-MAX) = VOLspec / IOLspec*
3. *R(PULL-UP-MAX) = (VCCImax – VOHspec) / IOHspec*

Table 2-95 • I/O Weak Pull-Up/Pull-Down Resistances, Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	$R_{(WEAK\ PULL\text{-}UP)}$ [1] (ohms)		$R_{(WEAK\ PULL\text{-}DOWN)}$ [2] (ohms)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / $I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / $I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

Table 2-96 • **I/O Short Currents IOSH/IOSL**

	Drive Strength	IOSH (mA)*	IOSL (mA)*
Applicable to Pro I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
Applicable to Advanced I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181

Note: *T_J = 100°C

Timing Characteristics

Table 2-102 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	11.61	0.05	1.27	1.65	0.44	11.82	9.55	2.84	2.58	14.18	11.90	ns
	–1	0.58	9.87	0.04	1.08	1.40	0.38	10.06	8.12	2.41	2.19	12.06	10.13	ns
	–2	0.51	8.67	0.03	0.95	1.23	0.33	8.83	7.13	2.12	1.92	10.59	8.89	ns
8 mA	Std.	0.68	8.29	0.05	1.27	1.65	0.44	8.45	6.79	3.20	3.23	10.80	9.15	ns
	–1	0.58	7.05	0.04	1.08	1.40	0.38	7.18	5.78	2.72	2.75	9.19	7.78	ns
	–2	0.51	6.19	0.03	0.95	1.23	0.33	6.31	5.07	2.39	2.41	8.07	6.83	ns
12 mA	Std.	0.68	6.35	0.05	1.27	1.65	0.44	6.47	5.29	3.45	3.66	8.83	7.65	ns
	–1	0.58	5.41	0.04	1.08	1.40	0.38	5.51	4.50	2.94	3.11	7.51	6.51	ns
	–2	0.51	4.75	0.03	0.95	1.23	0.33	4.83	3.95	2.58	2.73	6.59	5.71	ns
16 mA	Std.	0.68	5.93	0.05	1.27	1.65	0.44	6.04	4.98	3.50	3.77	8.39	7.34	ns
	–1	0.58	5.04	0.04	1.08	1.40	0.38	5.13	4.24	2.98	3.21	7.14	6.24	ns
	–2	0.51	4.42	0.03	0.95	1.23	0.33	4.51	3.72	2.62	2.82	6.27	5.48	ns
24 mA	Std.	0.68	5.53	0.05	1.27	1.65	0.44	5.63	4.95	3.57	4.18	7.99	7.31	ns
	–1	0.58	4.70	0.04	1.08	1.40	0.38	4.79	4.21	3.04	3.55	6.80	6.22	ns
	–2	0.51	4.13	0.03	0.95	1.23	0.33	4.21	3.70	2.67	3.12	5.97	5.46	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-114 • 1.8 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J =100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	12.76	0.05	1.53	2.01	0.44	10.11	12.76	2.93	1.73	12.47	15.12	ns
	–1	0.58	10.86	0.04	1.30	1.71	0.38	8.60	10.86	2.50	1.47	10.61	12.86	ns
	–2	0.51	9.53	0.03	1.14	1.50	0.33	7.55	9.53	2.19	1.29	9.31	11.29	ns
4 mA	Std.	0.68	7.44	0.05	1.53	2.01	0.44	6.54	7.44	3.43	3.02	8.90	9.79	ns
	–1	0.58	6.33	0.04	1.30	1.71	0.38	5.56	6.33	2.91	2.57	7.57	8.33	ns
	–2	0.51	5.55	0.03	1.14	1.50	0.33	4.88	5.55	2.56	2.26	6.64	7.31	ns
6 mA	Std.	0.68	4.77	0.05	1.53	2.01	0.44	4.71	4.77	3.76	3.66	7.07	7.13	ns
	–1	0.58	4.06	0.04	1.30	1.71	0.38	4.01	4.06	3.20	3.11	6.01	6.06	ns
	–2	0.51	3.56	0.03	1.14	1.50	0.33	3.52	3.56	2.81	2.73	5.28	5.32	ns
8 mA	Std.	0.68	4.35	0.05	1.53	2.01	0.44	4.43	4.21	3.83	3.82	6.79	6.57	ns
	–1	0.58	3.70	0.04	1.30	1.71	0.38	3.77	3.58	3.26	3.25	5.77	5.59	ns
	–2	0.51	3.25	0.03	1.14	1.50	0.33	3.31	3.14	2.86	2.85	5.07	4.91	ns
12 mA	Std.	0.68	4.00	0.05	1.53	2.01	0.44	3.80	3.21	3.90	4.30	6.15	5.57	ns
	–1	0.58	3.41	0.04	1.30	1.71	0.38	3.23	2.73	3.32	3.66	5.23	4.73	ns
	–2	0.51	2.99	0.03	1.14	1.50	0.33	2.83	2.40	2.91	3.21	4.60	4.16	ns
16 mA	Std.	0.68	4.00	0.035	1.53	2.01	0.44	3.80	3.21	3.90	4.30	6.15	5.57	ns
	–1	0.58	3.41	0.04	1.30	1.71	0.38	3.23	2.73	3.32	3.66	5.23	4.73	ns
	–2	0.51	2.99	0.03	1.14	1.50	0.33	2.83	2.40	2.91	3.21	4.60	4.16	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Table 2-122 • 1.5 V LVCMOS High Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.68	9.00	0.05	1.79	0.44	7.20	8.82	3.57	2.92	9.55	11.18	ns
	–1	0.58	7.65	0.04	1.52	0.38	6.12	7.50	3.04	2.48	8.13	9.51	ns
	–2	0.51	6.72	0.03	1.34	0.33	5.37	6.59	2.67	2.18	7.13	8.35	ns
4 mA	Std.	0.68	5.71	0.05	1.79	0.44	5.11	5.60	3.94	3.59	7.47	7.96	ns
	–1	0.58	4.85	0.04	1.52	0.38	4.35	4.77	3.36	3.05	6.36	6.77	ns
	–2	0.51	4.26	0.03	1.34	0.33	3.82	4.18	2.95	2.68	5.58	5.95	ns
6 mA	Std.	0.68	5.07	0.05	1.79	0.44	4.80	4.92	4.03	3.76	7.15	7.28	ns
	–1	0.58	4.31	0.04	1.52	0.38	4.08	4.19	3.43	3.20	6.09	6.19	ns
	–2	0.51	3.78	0.03	1.34	0.33	3.58	3.68	3.01	2.81	5.34	5.44	ns
8 mA	Std.	0.68	4.66	0.05	1.79	0.44	4.38	3.77	4.16	4.43	6.74	6.13	ns
	–1	0.58	3.96	0.04	1.52	0.38	3.73	3.21	3.54	3.77	5.73	5.21	ns
	–2	0.51	3.48	0.03	1.34	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns
12 mA	Std.	0.68	4.66	0.05	1.79	0.44	4.38	3.77	4.16	4.43	6.74	6.13	ns
	–1	0.58	3.96	0.04	1.52	0.38	3.73	3.21	3.54	3.77	5.73	5.21	ns
	–2	0.51	3.48	0.03	1.34	0.33	3.27	2.82	3.11	3.31	5.03	4.58	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND. Note: In FG256, FG484, and FG676 packages, GNDQ and GND pins are connected within the package and are labeled as GND pins in the respective package pin assignment tables.

ADCGNDREF **Analog Reference Ground**

Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.

GNDA **Ground (analog)**

Quiet ground supply voltage to the Analog Block of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation.

GNDAQ **Ground (analog quiet)**

Quiet ground supply voltage to the analog I/O of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation. Note: In FG256, FG484, and FG676 packages, GNDAQ and GNDA pins are connected within the package and are labeled as GNDA pins in the respective package pin assignment tables.

GNDNVM **Flash Memory Ground**

Ground supply used by the Fusion device's flash memory block module(s).

GNDOSC **Oscillator Ground**

Ground supply for both integrated RC oscillator and crystal oscillator circuit.

VCC15A **Analog Power Supply (1.5 V)**

1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry.

VCC33A **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the 3.3 V portion of the analog circuitry.

VCC33N **Negative 3.3 V Output**

This is the –3.3 V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to ground.

VCC33PMP **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the analog charge pump. To avoid high current draw, VCC33PMP should be powered up simultaneously with or after VCC33A.

VCCNVM **Flash Memory Block Power Supply (1.5 V)**

1.5 V power supply input used by the Fusion device's flash memory block module(s). To avoid high current draw, VCC should be powered up before or simultaneously with VCCNVM.

VCCOSC **Oscillator Power Supply (3.3 V)**

Power supply for both integrated RC oscillator and crystal oscillator circuit. The internal 100 MHz oscillator, powered by the VCCOSC pin, is needed for device programming, operation of the VDDN33

FG484		
Pin Number	AFS600 Function	AFS1500 Function
E9	NC	IO08PDB0V1
E10	GND	GND
E11	IO15NDB1V0	IO22NDB1V0
E12	IO15PDB1V0	IO22PDB1V0
E13	GND	GND
E14	NC	IO32PPB1V1
E15	NC	IO36NPB1V2
E16	VCCIB1	VCCIB1
E17	GND	GND
E18	NC	IO47NPB2V0
E19	IO33PDB2V0	IO49PDB2V0
E20	VCCIB2	VCCIB2
E21	IO32NDB2V0	IO46NDB2V0
E22	GBC2/IO32PDB2V0	GBC2/IO46PDB2V0
F1	IO80NDB4V0	IO118NDB4V0
F2	IO80PDB4V0	IO118PDB4V0
F3	NC	IO119NSB4V0
F4	IO84NDB4V0	IO124NDB4V0
F5	GND	GND
F6	VCOMPLA	VCOMPLA
F7	VCCPLA	VCCPLA
F8	VCCIB0	VCCIB0
F9	IO08NDB0V1	IO12NDB0V1
F10	IO08PDB0V1	IO12PDB0V1
F11	VCCIB0	VCCIB0
F12	VCCIB1	VCCIB1
F13	IO22NDB1V0	IO30NDB1V1
F14	IO22PDB1V0	IO30PDB1V1
F15	VCCIB1	VCCIB1
F16	NC	IO36PPB1V2
F17	NC	IO38NPB1V2
F18	GND	GND
F19	IO33NDB2V0	IO49NDB2V0
F20	IO34PDB2V0	IO50PDB2V0
F21	IO34NDB2V0	IO50NDB2V0

FG484		
Pin Number	AFS600 Function	AFS1500 Function
F22	IO35PDB2V0	IO51PDB2V0
G1	IO77PDB4V0	IO115PDB4V0
G2	GND	GND
G3	IO78NDB4V0	IO116NDB4V0
G4	IO78PDB4V0	IO116PDB4V0
G5	VCCIB4	VCCIB4
G6	NC	IO117PDB4V0
G7	VCCIB4	VCCIB4
G8	GND	GND
G9	IO04NDB0V0	IO06NDB0V1
G10	IO04PDB0V0	IO06PDB0V1
G11	IO12NDB0V1	IO16NDB0V2
G12	IO12PDB0V1	IO16PDB0V2
G13	NC	IO28NDB1V1
G14	NC	IO28PDB1V1
G15	GND	GND
G16	NC	IO38PPB1V2
G17	NC	IO53PDB2V0
G18	VCCIB2	VCCIB2
G19	IO36PDB2V0	IO52PDB2V0
G20	IO36NDB2V0	IO52NDB2V0
G21	GND	GND
G22	IO35NDB2V0	IO51NDB2V0
H1	IO77NDB4V0	IO115NDB4V0
H2	IO76PDB4V0	IO113PDB4V0
H3	VCCIB4	VCCIB4
H4	IO79NDB4V0	IO114NDB4V0
H5	IO79PDB4V0	IO114PDB4V0
H6	NC	IO117NDB4V0
H7	GND	GND
H8	VCC	VCC
H9	VCCIB0	VCCIB0
H10	GND	GND
H11	VCCIB0	VCCIB0
H12	VCCIB1	VCCIB1