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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	119
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-fgg256k

Flash Memory Block Addressing

Figure 2-34 shows a graphical representation of the flash memory block.

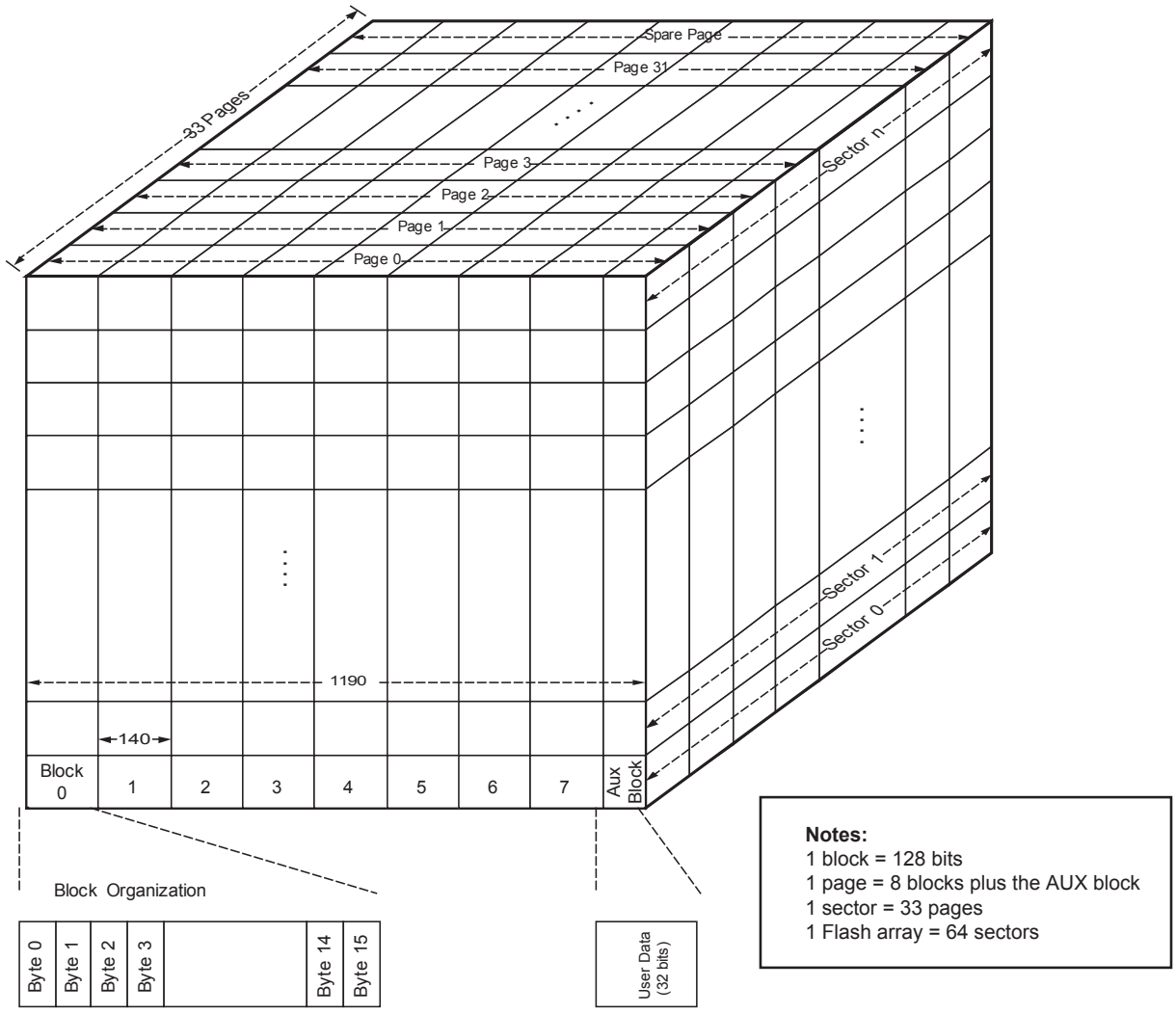

Figure 2-34 • **Flash Memory Block Organization**

Each FB is partitioned into sectors, pages, blocks, and bytes. There are 64 sectors in an FB, and each sector contains 32 pages and 1 spare page. Each page contains 8 data blocks and 1 auxiliary block. Each data block contains 16 bytes of user data, and the auxiliary block contains 4 bytes of user data.

Addressing for the FB is shown in Table 2-19.

Table 2-19 • **FB Address Bit Allocation ADDR[17:0]**

17	12	11	7	6	4	3	0
Sector		Page		Block		Byte	

When the spare page of a sector is addressed (SPAREPAGE active), ADDR[11:7] are ignored.

When the Auxiliary block is addressed (AUXBLOCK active), ADDR[6:2] are ignored.

Note: The spare page of sector 0 is unavailable for any user data. Writes to this page will return an error, and reads will return all zeroes.

DINA and DINB

These are the input data signals, and they are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded (Table 2-28).

DOUTA and DOUTB

These are the nine-bit output data signals. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits may not be used (Table 2-28). The output data on unused pins is undefined.

Table 2-28 • **Unused/Used Input and Output Data Pins for Various Supported Bus Widths**

	DINx/DOUTx	
D×W	**Unused**	**Used**
4k×1	[8:1]	[0]
2k×2	[8:2]	[1:0]
1k×4	[8:4]	[3:0]
512×9	None	[8:0]

Note: The "x" in DINx and DOUTx implies A or B.

SRAM Characteristics

Timing Waveforms

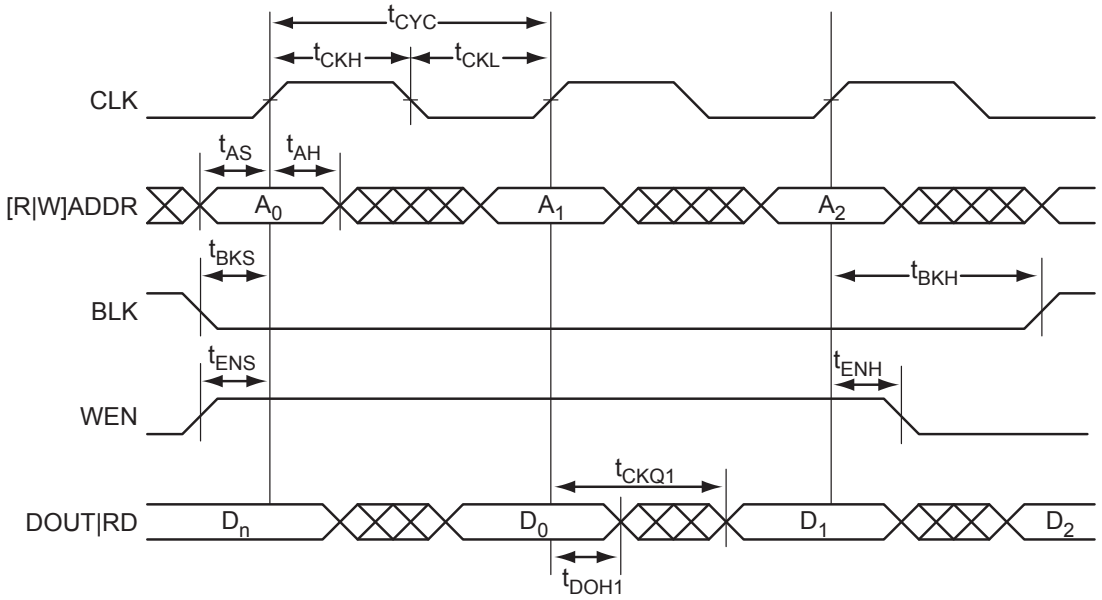

Figure 2-50 • **RAM Read for Flow-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

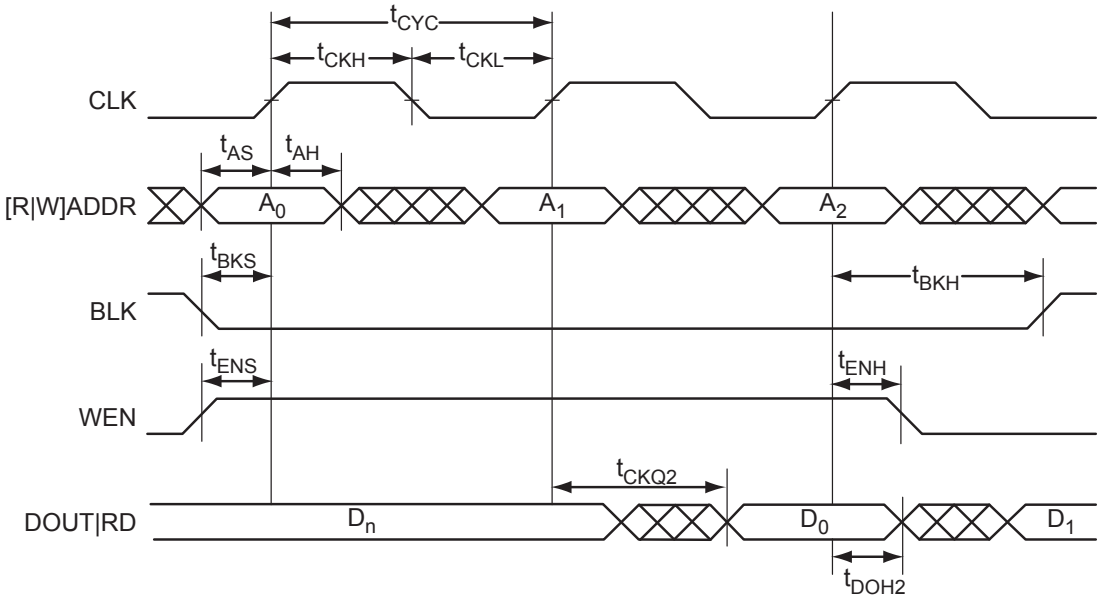

Figure 2-51 • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

Table 2-35 • **Analog Block Pin Description (continued)**

Signal Name	Number of Bits	Direction	Function	Location of Details
AG6	1	Output		Analog Quad
AT6	1	Input		Analog Quad
ATRETURN67	1	Input	Temperature monitor return shared by Analog Quads 6 and 7	Analog Quad
AV7	1	Input	Analog Quad 7	Analog Quad
AC7	1	Input		Analog Quad
AG7	1	Output		Analog Quad
AT7	1	Input		Analog Quad
AV8	1	Input	Analog Quad 8	Analog Quad
AC8	1	Input		Analog Quad
AG8	1	Output		Analog Quad
AT8	1	Input		Analog Quad
ATRETURN89	1	Input	Temperature monitor return shared by Analog Quads 8 and 9	Analog Quad
AV9	1	Input	Analog Quad 9	Analog Quad
AC9	1	Input		Analog Quad
AG9	1	Output		Analog Quad
AT9	1	Input		Analog Quad
RTCMATCH	1	Output	MATCH	RTC
RTCPSMMATCH	1	Output	MATCH connected to VRPSM	RTC
RTCXTLMODE[1:0]	2	Output	Drives XTLOSC RTCMODE[1:0] pins	RTC
RTCXTLSEL	1	Output	Drives XTLOSC MODESEL pin	RTC
RTCCLK	1	Input	RTC clock input	RTC

Analog Quad

With the Fusion family, Microsemi introduces the Analog Quad, shown in Figure 2-64 on page 2-81, as the basic analog I/O structure. The Analog Quad is a four-channel system used to precondition a set of analog signals before sending it to the ADC for conversion into a digital signal. To maximize the usefulness of the Analog Quad, the analog input signals can also be configured as LVTTL digital input signals. The Analog Quad is divided into four sections.

The first section is called the Voltage Monitor Block, and its input pin is named AV. It contains a two-channel analog multiplexer that allows an incoming analog signal to be routed directly to the ADC or allows the signal to be routed to a prescaler circuit before being sent to the ADC. The prescaler can be configured to accept analog signals between –12 V and 0 or between 0 and +12 V. The prescaler circuit scales the voltage applied to the ADC input pad such that it is compatible with the ADC input voltage range. The AV pin can also be used as a digital input pin.

The second section of the Analog Quad is called the Current Monitor Block. Its input pin is named AC. The Current Monitor Block contains all the same functions as the Voltage Monitor Block with one addition, which is a current monitoring function. A small external current sensing resistor (typically less than 1 Ω) is connected between the AV and AC pins and is in series with a power source. The Current Monitor Block contains a current monitor circuit that converts the current through the external resistor to a voltage that can then be read using the ADC.

(conversion that starts before a previously started conversion is finished). The total time for calibration still remains 3,840 ADCCLK cycles.

ADC Configuration Example

This example shows how to choose the correct settings to achieve the fastest sample time in 10-bit mode for a system that runs at 66 MHz. Assume the acquisition times defined in Table 2-43 on page 2-108 for 10-bit mode, which gives 0.549 µs as a minimum hold time.

The period of SYSCLK: t_{SYSCLK} = 1/66 MHz = 0.015 µs

Choosing TVC between 1 and 33 will meet the maximum and minimum period for the ADCCLK requirement. A higher TVC leads to a higher ADCCLK period.

The minimum TVC is chosen so that $t_{distrib}$ and $t_{post\text{-}cal}$ can be run faster. The period of ADCCLK with a TVC of 1 can be computed by EQ 24.

$$t_{ADCCLK} = 4 \times (1 + TVC) \times t_{SYSCLK} = 4 \times (1 + 1) \times 0.015\ \mu s = 0.12\ \mu s$$

EQ 24

The STC value can now be computed by using the minimum sample/hold time from Table 2-43 on page 2-108, as shown in EQ 25.

$$STC = \frac{t_{sample}}{t_{ADCCLK}} - 2 = \frac{0.549\ \mu s}{0.12\ \mu s} - 2 = 4.575 - 2 = 2.575$$

EQ 25

You must round up to 3 to accommodate the minimum sample time requirement. The actual sample time, t_{sample}, with an STC of 3, is now equal to 0.6 µs, as shown in EQ 26

$$t_{sample} = (2 + STC) \times t_{ADCCLK} = (2 + 3) \times t_{ADCCLK} = 5 \times 0.12\ \mu s = 0.6\ \mu s$$

EQ 26

Microsemi recommends post-calibration for temperature drift over time, so post-calibration is enabled.

The post-calibration time, $t_{post\text{-}cal}$, can be computed by EQ 27. The post-calibration time is 0.24 µs.

$$t_{post\text{-}cal} = 2 \times t_{ADCCLK} = 0.24\ \mu s$$

EQ 27

The distribution time, $t_{distrib}$, is equal to 1.2 µs and can be computed as shown in EQ 28 (N is number of bits, referring back to EQ 8 on page 2-94).

$$t_{distrib} = N \times t_{ADCCLK} = 10 \times 0.12 = 1.2\ \mu s$$

EQ 28

The total conversion time can now be summated, as shown in EQ 29 (referring to EQ 23 on page 2-109).

$$t_{sync\_read} + t_{sample} + t_{distrib} + t_{post\text{-}cal} + t_{sync\_write} = (0.015 + 0.60 + 1.2 + 0.24 + 0.015)\ \mu s = 2.07\ \mu s$$

EQ 29

The optimal setting for the system running at 66 MHz with an ADC for 10-bit mode chosen is shown in Table 2-46:

***Table 2-46* • Optimal Setting at 66 MHz in 10-Bit Mode**

TVC[7:0]	= 1	= 0x01
STC[7:0]	= 3	= 0x03
MODE[3:0]	= b'0100	= 0x4*

Note: No power-down after every conversion is chosen in this case; however, if the application is power-sensitive, the MODE[2] can be set to '0', as described above, and it will not affect any performance.

Table 2-51 • Uncalibrated Analog Channel Accuracy*
Worst-Case Extended Temperature Conditions, T_J = 100°C

		Total Channel Error (LSB)			Channel Input Offset Error (LSB)			Channel Input Offset Error (mV)			Channel Gain Error (%FSR)		
Analog Pad	Prescaler Range (V)	Neg. Max.	Med.	Pos. Max.	Neg Max	Med.	Pos. Max.	Neg. Max.	Med.	Pos. Max.	Min.	Typ.	Max.
Positive Range		**ADC in 10-Bit Mode**											
AV, AC	16	–22	–2	12	–11	–2	14	–169	–32	224	3	0	–3
	8	–40	–5	17	–11	–5	21	–87	–40	166	2	0	–4
	4	–45	–9	24	–16	–11	36	–63	–43	144	2	0	–4
	2	–70	–19	33	–33	–20	66	–66	–39	131	2	0	–4
	1	–25	–7	5	–11	–3	26	–11	–3	26	3	–1	–3
	0.5	–41	–12	8	–12	–7	38	–6	–4	19	3	–1	–3
	0.25	–53	–14	19	–20	–14	40	–5	–3	10	5	0	–4
	0.125	–89	–29	24	–40	–28	88	–5	–4	11	7	0	–5
AT	16	–3	9	15	–4	0	4	–64	5	64	1	0	–1
	4	–10	2	15	–11	–2	11	–44	–8	44	1	0	–1
Negative Range		**ADC in 10-Bit Mode**											
AV, AC	16	–35	–10	9	–24	–6	9	–383	–96	148	5	–1	–6
	8	–65	–19	12	–34	–12	9	–268	–99	75	5	–1	–5
	4	–86	–28	21	–64	–24	19	–254	–96	76	5	–1	–6
	2	–136	–53	37	–115	–42	39	–230	–83	78	6	–2	–7
	1	–98	–35	8	–39	–8	15	–39	–8	15	10	–3	–10
	0.5	–121	–46	7	–54	–14	18	–27	–7	9	10	–4	–11
	0.25	–149	–49	19	–72	–16	40	–18	–4	10	14	–4	–12
	0.125	–188	–67	38	–112	–27	56	–14	–3	7	16	–5	–14

*Note: *Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Gain remains the same.*

Table 2-60 • **Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)***

Control Lines Bx[6]	Input Signal Polarity
1 [2]	Negative

Notes:

1. *The B3[6] signal for the AT pad should be kept at logic 0 to accept only positive voltages.*
2. *Negative input is not supported between –40°C and –55°C.*

Table 2-61 details the settings available to either power down or enable the prescaler associated with the analog inputs AV, AC, and AT.

Table 2-61 • **Prescaler Op Amp Power-Down Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)**

Control Lines Bx[7]	Prescaler Op Amp
0	Power-down
1	Operational

Table 2-62 details the settings available to enable the Current Monitor Block associated with the AC pin.

Table 2-62 • **Current Monitor Input Switch Control Truth Table—AV (x = 0)**

Control Lines B0[4]	Current Monitor Input Switch
0	Off
1 *	On

Note: Current monitor is not supported between –40°C and –55°C.

Table 2-63 details the settings available to configure the drive strength of the gate drive when not in high-drive mode.

Table 2-63 • **Low-Drive Gate Driver Current Truth Table (AG)**

Control Lines B2[3]	Control Lines B2[2]	Current (µA)
0	0	1
0	1	3
1	0	10
1	1	30

Table 2-64 details the settings available to set the polarity of the gate driver (either p-channel- or n-channel-type devices).

Table 2-64 • **Gate Driver Polarity Truth Table (AG)**

Control Lines B2[6]	Gate Driver Polarity
0	Positive
1	Negative

Table 2-65 details the settings available to turn on the Gate Driver and set whether high-drive mode is on or off.

Table 2-65 • **Gate Driver Control Truth Table (AG)**

Control Lines B2[7]	GDON	Gate Driver
0	0	Off
0	1	Low drive on
1	0	Off
1	1	High drive on

Table 2-66 details the settings available to turn on and off the chip internal temperature monitor.

Table 2-73 • Maximum I/O Frequency for Single-Ended, Voltage-Referenced, and Differential I/Os; All I/O Bank Types (maximum drive strength and high slew selected)

Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	200 MHz
LVCMOS 2.5 V	250 MHz
LVCMOS 1.8 V	200 MHz
LVCMOS 1.5 V	130 MHz
PCI	200 MHz
PCI-X	200 MHz
HSTL-I	300 MHz
HSTL-II	300 MHz
SSTL2-I	300 MHz
SSTL2-II	300 MHz
SSTL3-I	300 MHz
SSTL3-II	300 MHz
GTL+ 3.3 V	300 MHz
GTL+ 2.5 V	300 MHz
GTL 3.3 V	300 MHz
GTL 2.5 V	300 MHz
LVDS	350 MHz
LVPECL	300 MHz

Table 2-74 • Maximum I/O Frequency for Single-Ended and Differential I/Os for Advanced I/Os (maximum drive strength and high slew selected)

Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	250 MHz
LVCMOS 2.5 V	300 MHz
LVCMOS 1.8 V	250 MHz
LVCMOS 1.5 V	180 MHz
PCI	300 MHz
PCI-X	300 MHz
LVDS	350 MHz
LVPECL	300 MHz

At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss or transmitter overstress due to transmitter-to-transmitter current shorts. Figure 2-109 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 2-110 shows how bus contention is created, and Figure 2-111 on page 2-152 shows how it can be avoided with the skew circuit.

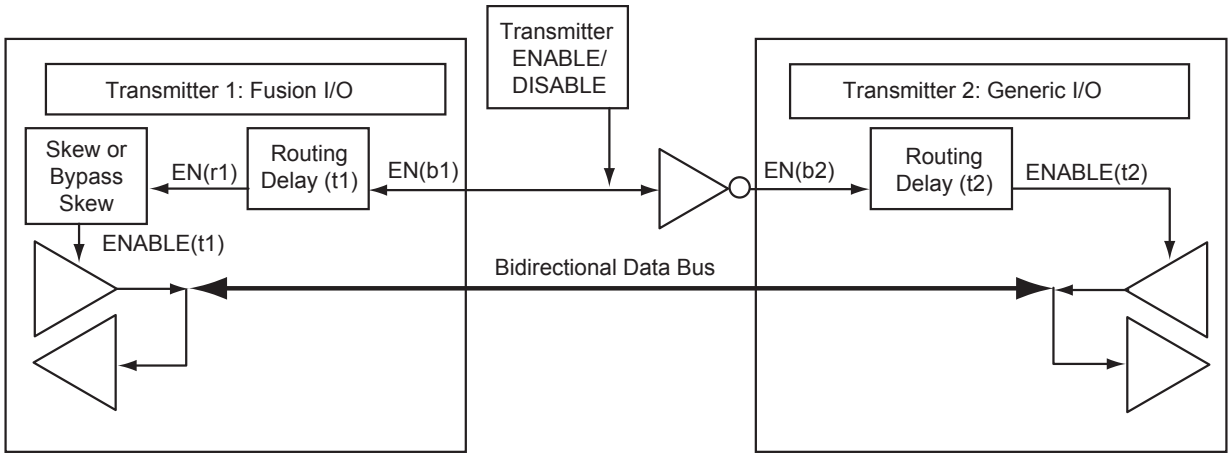

Figure 2-109 • **Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using Fusion Devices**

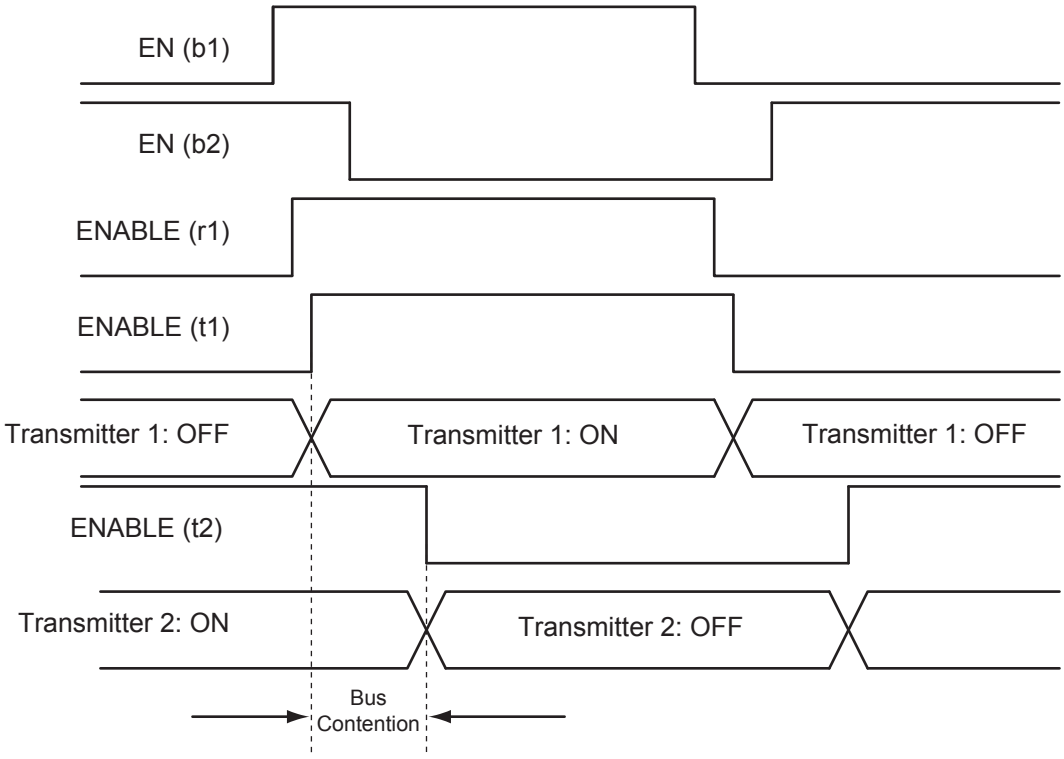

Figure 2-110 • **Timing Diagram (bypasses skew circuit)**

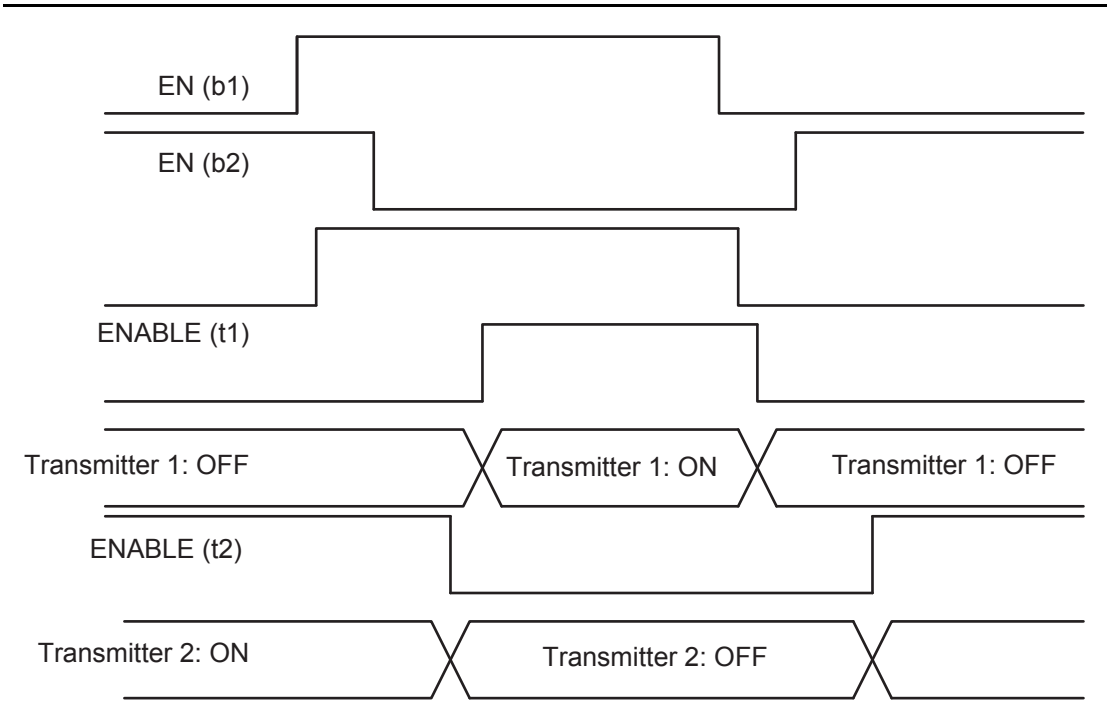

Figure 2-111 • **Timing Diagram (with skew circuit selected)**

Weak Pull-Up and Weak Pull-Down Resistors

Fusion devices support optional weak pull-up and pull-down resistors for each I/O pin. When the I/O is pulled up, it is connected to the VCCI of its corresponding I/O bank. When it is pulled down, it is connected to GND. Refer to Table 2-95 on page 2-171 for more information.

Slew Rate Control and Drive Strength

Fusion devices support output slew rate control: high and low. The high slew rate option is recommended to minimize the propagation delay. This high-speed option may introduce noise into the system if appropriate signal integrity measures are not adopted. Selecting a low slew rate reduces this kind of noise but adds some delays in the system. Low slew rate is recommended when bus transients are expected. Drive strength should also be selected according to the design requirements and noise immunity of the system.

The output slew rate and multiple drive strength controls are available in LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V, LVCMOS 2.5 V / 5.0 V input, LVCMOS 1.8 V, and LVCMOS 1.5 V. All other I/O standards have a high output slew rate by default.

For Fusion slew rate and drive strength specifications, refer to the appropriate I/O bank table:

- Fusion Advanced I/O (Table 2-79 on page 2-153)
- Fusion Pro I/O (Table 2-80 on page 2-153)

Table 2-83 on page 2-156 lists the default values for the above selectable I/O attributes as well as those that are preset for each I/O standard.

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Extended Temperature Conditions Applicable to Pro I/Os

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	IOL	IOH
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
2.5 V GTL	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
3.3 V GTL+	35 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33
HSTL (I)	8 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8
HSTL (II)	15 mA[2]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *Currents are measured at 100°C junction temperature.*
2. *Output drive strength is below JEDEC specification.*
3. *Output slew rate can be extracted by the IBIS models.*

Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Extended Temperature Conditions Applicable to Advanced I/Os

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: Currents are measured at 100°C junction temperature.

Table 2-109 • 2.5 V LVCMOS Low Slew, Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.68	12.02	0.05	1.38	0.44	11.83	12.02	2.82	2.33	14.19	14.38	ns
	–1	0.58	10.22	0.04	1.18	0.38	10.06	10.22	2.40	1.98	12.07	12.23	ns
	–2	0.51	8.97	0.03	1.03	0.33	8.83	8.97	2.11	1.74	10.59	10.74	ns
8 mA	Std.	0.68	8.39	0.05	1.38	0.44	8.55	8.24	3.22	3.05	10.91	10.60	ns
	–1	0.58	7.14	0.04	1.18	0.38	7.27	7.01	2.74	2.59	9.28	9.02	ns
	–2	0.51	6.27	0.03	1.03	0.33	6.38	6.15	2.40	2.28	8.15	7.91	ns
12 mA	Std.	0.68	6.52	0.05	1.38	0.44	6.64	6.24	3.48	3.50	8.99	8.60	ns
	–1	0.58	5.54	0.04	1.18	0.38	5.65	5.31	2.96	2.98	7.65	7.31	ns
	–2	0.51	4.87	0.03	1.03	0.33	4.96	4.66	2.60	2.62	6.72	6.42	ns
16 mA	Std.	0.68	6.08	0.05	1.38	0.44	6.19	5.83	3.54	3.63	8.55	8.18	ns
	–1	0.58	5.17	0.04	1.18	0.38	5.27	4.96	3.01	3.08	7.27	6.96	ns
	–2	0.51	4.54	0.03	1.03	0.33	4.62	4.35	2.65	2.71	6.38	6.11	ns
24 mA	Std.	0.68	5.81	0.05	1.38	0.44	5.80	5.81	3.62	4.08	8.16	8.16	ns
	–1	0.58	4.94	0.04	1.18	0.38	4.94	4.94	3.08	3.47	6.94	6.95	ns
	–2	0.51	4.34	0.03	1.03	0.33	4.33	4.34	2.70	3.05	6.09	6.10	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 2-130 • Minimum and Maximum DC Input and Output Levels

2.5 GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[4]	IIH[5]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
20 mA[3]	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20	124	169	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*
4. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
5. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

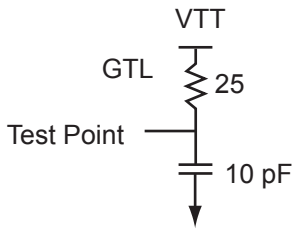

Figure 2-123 • AC Loading

Table 2-131 • 2.5 GTL AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

*Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

Table 2-132 • 2.5 V GTL
Extended Temperature Case Conditions: T_J = 100°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.24	0.05	2.59	0.44	2.28	2.24			4.64	4.60	ns
–1	0.58	1.91	0.04	2.20	0.38	1.94	1.91			3.95	3.91	ns
–2	0.51	1.68	0.03	1.93	0.33	1.70	1.68			3.46	3.44	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-136 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
33 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33	124	169	15	15

Notes:

1. *I_{IL} is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

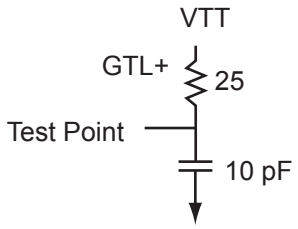

Figure 2-125 • AC Loading

Table 2-137 • 2.5 V GTL+ AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	CLOAD (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-80 on page 2-153 for a complete table of trip points.*

Timing Characteristics

Table 2-138 • 2.5 V GTL+
Extended Temperature Case Conditions: T_J = 100°C, Worst Case VCC = 1.425 V, Worst Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.68	2.33	0.05	1.60	0.44	2.37	2.21			4.73	4.57	ns
–1	0.58	1.98	0.04	1.36	0.38	2.02	1.88			4.02	3.89	ns
–2	0.51	1.74	0.03	1.19	0.33	1.77	1.65			3.53	3.41	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-10.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

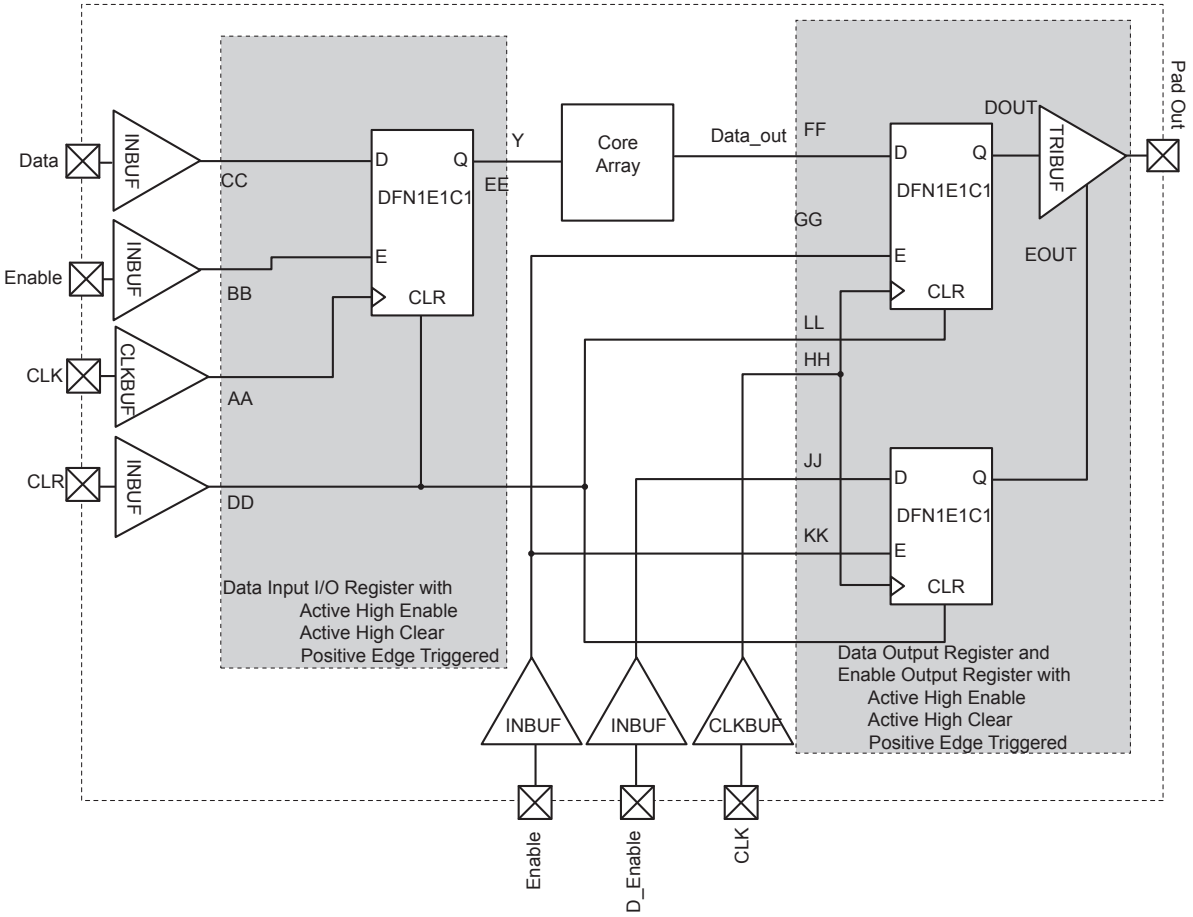

Figure 2-136 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

RC Oscillator Dynamic Contribution—$P_{RC\text{-}OSC}$

Operating Mode

$P_{RC\text{-}OSC}$ = PAC19

Standby Mode and Sleep Mode

$P_{RC\text{-}OSC}$ = 0 W

Analog System Dynamic Contribution—P_{AB}

Operating Mode

P_{AB} = PAC20

Standby Mode and Sleep Mode

P_{AB} = 0 W

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

Table 3-14 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 3-15 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%
β_4	NVM enable rate for read operations	0%

Standby Mode and Sleep Mode

$P_{S\text{-}CELL}$ = 0 W

$P_{C\text{-}CELL}$ = 0 W

P_{NET} = 0 W

P_{LOGIC} = 0 W

I/O Input and Output Buffer Contribution—$P_{I/O}$

This example uses LVTTL 3.3 V I/O cells. The output buffers are 12 mA–capable, configured with high output slew and driving a 35 pF output load.

F_{CLK} = 50 MHz

Number of input pins used: N_{INPUTS} = 30

Number of output pins used: $N_{OUTPUTS}$ = 40

Estimated I/O buffer toggle rate: α_2 = 0.1 (10%)

Estimated IO buffer enable rate: β_1 = 1 (100%)

Operating Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * PAC9 * F_{CLK}$

$P_{INPUTS} = 30 * (0.1 / 2) * 0.01739 * 50$

P_{INPUTS} = 1.30 mW

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * PAC10 * F_{CLK}$

$P_{OUTPUTS} = 40 * (0.1 / 2) * 1 * 0.4747 * 50$

$P_{OUTPUTS}$ = 47.47 mW

$P_{I/O} = P_{INPUTS} + P_{OUTPUTS}$

$P_{I/O}$ = 1.30 mW + 47.47 mW

$P_{I/O}$ = 48.77 mW

Standby Mode and Sleep Mode

P_{INPUTS} = 0 W

$P_{OUTPUTS}$ = 0 W

$P_{I/O}$ = 0 W

RAM Contribution—P_{MEMORY}

Frequency of Read Clock: $F_{READ\text{-}CLOCK}$ = 10 MHz

Frequency of Write Clock: $F_{WRITE\text{-}CLOCK}$ = 10 MHz

Number of RAM blocks: N_{BLOCKS} = 20

Estimated RAM Read Enable Rate: β_2 = 0.125 (12.5%)

Estimated RAM Write Enable Rate: β_3 = 0.125 (12.5%)

Operating Mode

$P_{MEMORY} = (N_{BLOCKS} * P_{AC11} * \beta_2 * F_{READ\text{-}CLOCK}) + (N_{BLOCKS} * P_{AC12} * \beta_3 * F_{WRITE\text{-}CLOCK})$

$P_{MEMORY} = (20 * 0.025 * 0.125 * 10) + (20 * 0.030 * 0.125 * 10)$

P_{MEMORY} = 1.38 mW

Standby Mode and Sleep Mode

P_{MEMORY} = 0 W

FG484		
Pin Number	AFS600 Function	AFS1500 Function
E9	NC	IO08PDB0V1
E10	GND	GND
E11	IO15NDB1V0	IO22NDB1V0
E12	IO15PDB1V0	IO22PDB1V0
E13	GND	GND
E14	NC	IO32PPB1V1
E15	NC	IO36NPB1V2
E16	VCCIB1	VCCIB1
E17	GND	GND
E18	NC	IO47NPB2V0
E19	IO33PDB2V0	IO49PDB2V0
E20	VCCIB2	VCCIB2
E21	IO32NDB2V0	IO46NDB2V0
E22	GBC2/IO32PDB2V0	GBC2/IO46PDB2V0
F1	IO80NDB4V0	IO118NDB4V0
F2	IO80PDB4V0	IO118PDB4V0
F3	NC	IO119NSB4V0
F4	IO84NDB4V0	IO124NDB4V0
F5	GND	GND
F6	VCOMPLA	VCOMPLA
F7	VCCPLA	VCCPLA
F8	VCCIB0	VCCIB0
F9	IO08NDB0V1	IO12NDB0V1
F10	IO08PDB0V1	IO12PDB0V1
F11	VCCIB0	VCCIB0
F12	VCCIB1	VCCIB1
F13	IO22NDB1V0	IO30NDB1V1
F14	IO22PDB1V0	IO30PDB1V1
F15	VCCIB1	VCCIB1
F16	NC	IO36PPB1V2
F17	NC	IO38NPB1V2
F18	GND	GND
F19	IO33NDB2V0	IO49NDB2V0
F20	IO34PDB2V0	IO50PDB2V0
F21	IO34NDB2V0	IO50NDB2V0

FG484		
Pin Number	AFS600 Function	AFS1500 Function
F22	IO35PDB2V0	IO51PDB2V0
G1	IO77PDB4V0	IO115PDB4V0
G2	GND	GND
G3	IO78NDB4V0	IO116NDB4V0
G4	IO78PDB4V0	IO116PDB4V0
G5	VCCIB4	VCCIB4
G6	NC	IO117PDB4V0
G7	VCCIB4	VCCIB4
G8	GND	GND
G9	IO04NDB0V0	IO06NDB0V1
G10	IO04PDB0V0	IO06PDB0V1
G11	IO12NDB0V1	IO16NDB0V2
G12	IO12PDB0V1	IO16PDB0V2
G13	NC	IO28NDB1V1
G14	NC	IO28PDB1V1
G15	GND	GND
G16	NC	IO38PPB1V2
G17	NC	IO53PDB2V0
G18	VCCIB2	VCCIB2
G19	IO36PDB2V0	IO52PDB2V0
G20	IO36NDB2V0	IO52NDB2V0
G21	GND	GND
G22	IO35NDB2V0	IO51NDB2V0
H1	IO77NDB4V0	IO115NDB4V0
H2	IO76PDB4V0	IO113PDB4V0
H3	VCCIB4	VCCIB4
H4	IO79NDB4V0	IO114NDB4V0
H5	IO79PDB4V0	IO114PDB4V0
H6	NC	IO117NDB4V0
H7	GND	GND
H8	VCC	VCC
H9	VCCIB0	VCCIB0
H10	GND	GND
H11	VCCIB0	VCCIB0
H12	VCCIB1	VCCIB1

FG484		
Pin Number	AFS600 Function	AFS1500 Function
V3	VCCIB4	VCCIB4
V4	GEA1/IO61PDB4V0	GEA1/IO88PDB4V0
V5	GEA0/IO61NDB4V0	GEA0/IO88NDB4V0
V6	GND	GND
V7	VCC33PMP	VCC33PMP
V8	NC	NC
V9	VCC33A	VCC33A
V10	AG4	AG4
V11	AT4	AT4
V12	ATRTN2	ATRTN2
V13	AT5	AT5
V14	VCC33A	VCC33A
V15	NC	NC
V16	VCC33A	VCC33A
V17	GND	GND
V18	TMS	TMS
V19	VJTAG	VJTAG
V20	VCCIB2	VCCIB2
V21	TRST	TRST
V22	TDO	TDO
W1	NC	IO93PDB4V0
W2	GND	GND
W3	NC	IO93NDB4V0
W4	GEB2/IO59PDB4V0	GEB2/IO86PDB4V0
W5	IO59NDB4V0	IO86NDB4V0
W6	AV0	AV0
W7	GNDA	GNDA
W8	AV1	AV1
W9	AV2	AV2
W10	GNDA	GNDA
W11	AV3	AV3
W12	AV6	AV6
W13	GNDA	GNDA
W14	AV7	AV7
W15	AV8	AV8

FG484		
Pin Number	AFS600 Function	AFS1500 Function
W16	GNDA	GNDA
W17	AV9	AV9
W18	VCCIB2	VCCIB2
W19	NC	IO68PPB2V0
W20	TCK	TCK
W21	GND	GND
W22	NC	IO76PPB2V0
Y1	GEC2/IO60PDB4V0	GEC2/IO87PDB4V0
Y2	IO60NDB4V0	IO87NDB4V0
Y3	GEA2/IO58PDB4V0	GEA2/IO85PDB4V0
Y4	IO58NDB4V0	IO85NDB4V0
Y5	NCAP	NCAP
Y6	AC0	AC0
Y7	VCC33A	VCC33A
Y8	AC1	AC1
Y9	AC2	AC2
Y10	VCC33A	VCC33A
Y11	AC3	AC3
Y12	AC6	AC6
Y13	VCC33A	VCC33A
Y14	AC7	AC7
Y15	AC8	AC8
Y16	VCC33A	VCC33A
Y17	AC9	AC9
Y18	ADCGNDREF	ADCGNDREF
Y19	PTBASE	PTBASE
Y20	GNDNVM	GNDNVM
Y21	VCCNVM	VCCNVM
Y22	VPUMP	VPUMP

Revision	Changes	Page
Revision 1 (continued)	The following information was added before Figure 2-17 • XTLOSC Macro: In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating (SAR 34900).	2-19
	Table 2-11 • Fusion CCC/PLL Specification was updated. A note was added indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34815).	2-28
	A note was added to Figure 2-27 • Real-Time Counter System (not all the signals are shown for the AB macro) stating that the user is only required to instantiate the VRPSM macro if the user wishes to specify PUPO behavior of the voltage regulator to be different from the default, or employ user logic to shut the voltage regulator off (SAR 34897).	2-31
	VPUMP was incorrectly represented as VPP in several places. This was corrected to VPUMP in the "Standby and Sleep Mode Circuit Implementation" section, Table 3-8 • AFS1500 Quiescent Supply Current Characteristics, and Table 3-9 • AFS600 Quiescent Supply Current Characteristics (SAR 34922).	2-32, 3-11, 3-13
	Additional information was added to the Flash Memory Block "Write Operation" section, including an explanation of the fact that a copy-page operation takes no less than 55 cycles (SAR 34924).	2-45
	The "FlashROM" section was revised to refer to Figure 2-46 • FlashROM Timing Diagram and Table 2-25 • FlashROM Access Time, Extended Temperature Conditions: TJ = 100°C, Worst-Case VCC = 1.425 V rather than stating 20 MHz as the maximum FlashROM access clock and 10 ns as the time interval for D0 to become valid or invalid (SAR 34923).	2-54
	Figure 2-54 • One Port Write / Other Port Read Same was deleted. Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34864). The port names in the "SRAM Characteristics" section, Figure 2-58 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SARs 35745, 38235).	2-63, 2-73, 2-75
	Figure 2-56 • FIFO Read and Figure 2-57 • FIFO Write were added (SAR 34839).	2-72
	In several places throughout the datasheet, GNDREF was corrected to ADCGNDREF (SAR 38698): Figure 2-63 • Analog Block Macro Table 2-35 • Analog Block Pin Description "ADC Operation" section	2-77, 2-78, 2-104
	The following note was added below Figure 2-77 • Timing Diagram for the Temperature Monitor Strobe Signal: When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a 1 µA sink into the Fusion device (SAR 34901).	2-93
	Table 2-49 • Analog Channel Specifications was modified to include calibrated and uncalibrated values for offset (AFS090 and AFS250) for the external and internal temperature monitors. The "Offset" section was revised accordingly and now references Table 2-49 • Analog Channel Specifications (SARs 34898, 34902).	2-95, 2-117
	The "Analog-to-Digital Converter Block" section was extensively revised, reorganizing the information and adding the "ADC Theory of Operation" section and "Acquisition Time or Sample Time Control" section. The "ADC Configuration Example" section was reworked and corrected (SAR 34918).	2-96