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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	172
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-fgg484k">https://www.e-xfl.com/product-detail/microchip-technology/m1afs600-fgg484k</a>

## **Instant On**

Flash-based Fusion devices are Level 0 Instant On. Instant On Fusion devices greatly simplify total system design and reduce total system cost by eliminating the need for CPLDs. The Fusion Instant On clocking (PLLs) replaces off-chip clocking resources. The Fusion mix of Instant On clocking and analog resources makes these devices an excellent choice for both system supervisor and system management functions. Instant On from a single 3.3 V source enables Fusion devices to initiate, control, and monitor multiple voltage supplies while also providing system clocks. In addition, glitches and brownouts in system power will not corrupt the Fusion device flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design. Flash-based Fusion devices simplify total system design and reduce cost and design risk, while increasing system reliability.

## **Firm Errors**

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. Another source of radiation-induced firm errors is alpha particles. For an alpha to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in Fusion flash-based FPGAs. Once it is programmed, the flash cell configuration element of Fusion FPGAs cannot be altered by high-energy neutrons and is therefore immune to errors from them.

Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

## **Low Power**

Flash-based Fusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With Fusion devices, there is no power-on current surge and no high current transition, both of which occur on many FPGAs.

Fusion devices also have low dynamic power consumption and support both low power standby mode and very low power sleep mode, offering further power savings.

## **Advanced Flash Technology**

The Fusion family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows very high logic utilization (much higher than competing SRAM technologies) without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

## **Advanced Architecture**

The proprietary Fusion architecture provides granularity comparable to standard-cell ASICs. The Fusion device consists of several distinct and programmable architectural features, including the following (Figure 1-1 on page 1-5):

- Embedded memories
  - Flash memory blocks
  - FlashROM
  - SRAM and FIFO

## 2 – Device Architecture

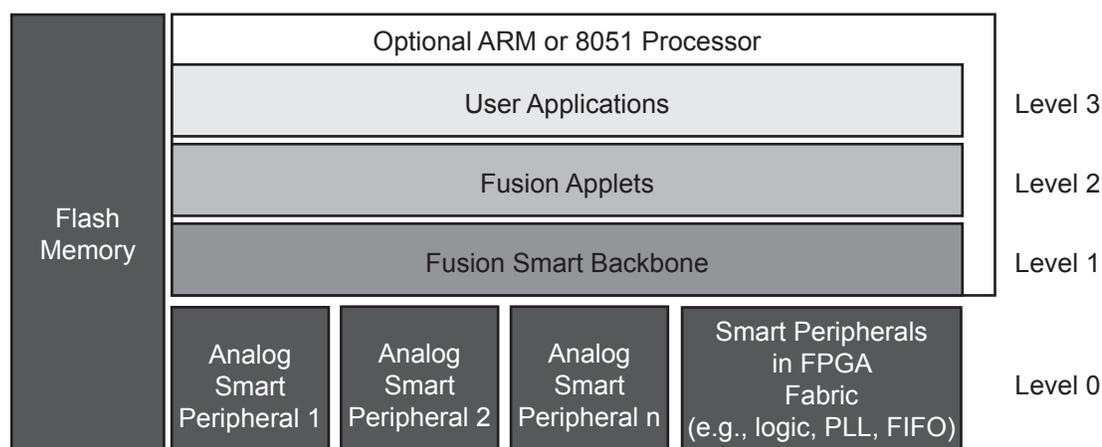
### Fusion Stack Architecture

To manage the unprecedented level of integration in Fusion devices, Microsemi developed the Fusion technology stack (Figure 2-1). This layered model offers a flexible design environment, enabling design at very high and very low levels of abstraction. Fusion peripherals include hard analog IP and hard and soft digital IP. Peripherals communicate across the FPGA fabric via a layer of soft gates—the Fusion backbone. Much more than a common bus interface, this Fusion backbone integrates a micro-sequencer within the FPGA fabric and configures the individual peripherals and supports low-level processing of peripheral data. Fusion applets are application building blocks that can control and respond to peripherals and other system signals. Applets can be rapidly combined to create large applications. The technology is scalable across devices, families, design types, and user expertise, and supports a well-defined interface for external IP and tool integration.

At the lowest level, Level 0, are Fusion peripherals. These are configurable functional blocks that can be hardwired structures such as a PLL or analog input channel, or soft (FPGA gate) blocks such as a UART or two-wire serial interface. The Fusion peripherals are configurable and support a standard interface to facilitate communication and implementation.

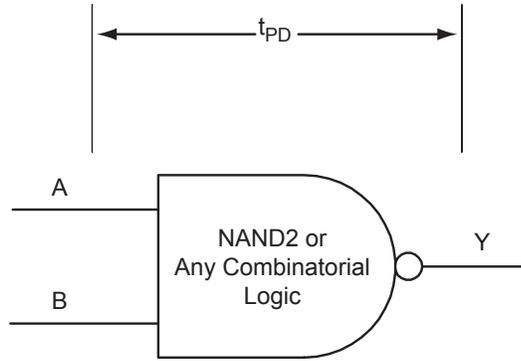
Connecting and controlling access to the peripherals is the Fusion backbone, Level 1. The backbone is a soft-gate structure, scalable to any number of peripherals. The backbone is a bus and much more; it manages peripheral configuration to ensure proper operation. Leveraging the common peripheral interface and a low-level state machine, the backbone efficiently offloads peripheral management from the system design. The backbone can set and clear flags based upon peripheral behavior and can define performance criteria. The flexibility of the stack enables a designer to configure the silicon, directly bypassing the backbone if that level of control is desired.

One step up from the backbone is the Fusion applet, Level 2. The applet is an application building block that implements a specific function in FPGA gates. It can react to stimuli and board-level events coming through the backbone or from other sources, and responds to these stimuli by accessing and manipulating peripherals via the backbone or initiating some other action. An applet controls or responds to the peripheral(s). Applets can be easily imported or exported from the design environment. The applet structure is open and well-defined, enabling users to import applets from Microsemi, system developers, third parties, and user groups.



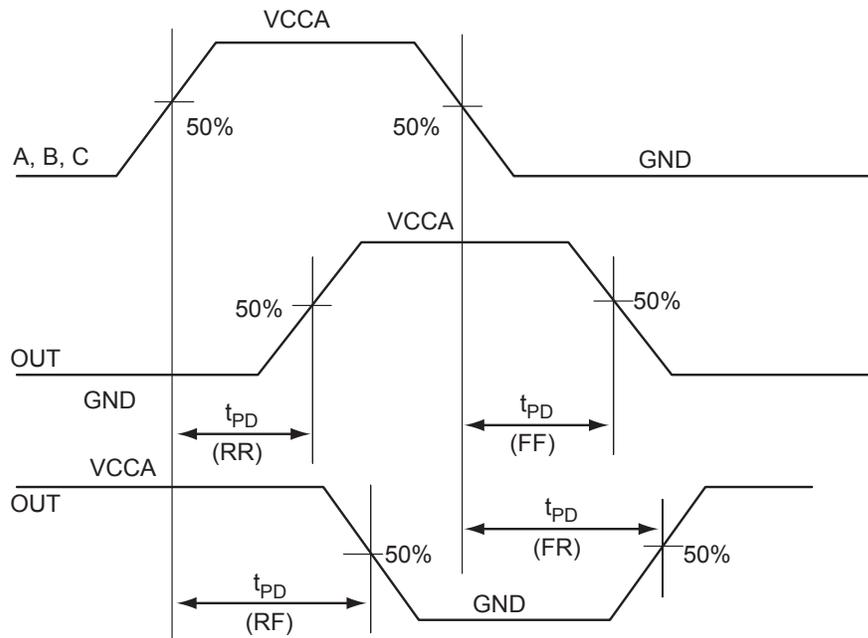
*Note:* Levels 1, 2, and 3 are implemented in FPGA logic gates.

**Figure 2-1 • Fusion Architecture Stack**



$$t_{PD} = \text{MAX}(t_{PD(RR)}, t_{PD(RF)}, t_{PD(FF)}, t_{PD(FR)})$$

where edges are applicable for the particular combinatorial cell



**Figure 2-4 • Combinatorial Timing Model and Waveforms**

## Global Resources (VersaNets)

Fusion devices offer powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has six CCCs. The west CCC also contains a PLL core. In the AFS600 and AFS1500, the west and the east CCCs each contain a PLL. The PLLs include delay lines, a phase shifter (0°, 90°, 180°, 270°), and clock multipliers/dividers. Each CCC has all the circuitry needed for the selection and interconnection of inputs to the VersaNet global network. The east and west CCCs each have access to three VersaNet global lines on each side of the chip (six lines total). The CCCs at the four corners each have access to three quadrant global lines on each quadrant of the chip.

### Advantages of the VersaNet Approach

One of the architectural benefits of Fusion is the set of powerful and low-delay VersaNet global networks. Fusion offers six chip (main) global networks that are distributed from the center of the FPGA array (Figure 2-11). In addition, Fusion devices have three regional globals (quadrant globals) in each of the four chip quadrants. Each core VersaTile has access to nine global network resources: three quadrant and six chip (main) global networks. There are a total of 18 global networks on the device. Each of these networks contains spines and ribs that reach all VersaTiles in all quadrants (Figure 2-12 on page 2-12). This flexible VersaNet global network architecture allows users to map up to 180 different internal/external clocks in a Fusion device. Details on the VersaNet networks are given in Table 2-4 on page 2-12. The flexibility of the Fusion VersaNet global network allows the designer to address several design requirements. User applications that are clock-resource-intensive can easily route external or gated internal clocks using VersaNet global routing networks. Designers can also drastically reduce delay penalties and minimize resource usage by mapping critical, high-fanout nets to the VersaNet global network.

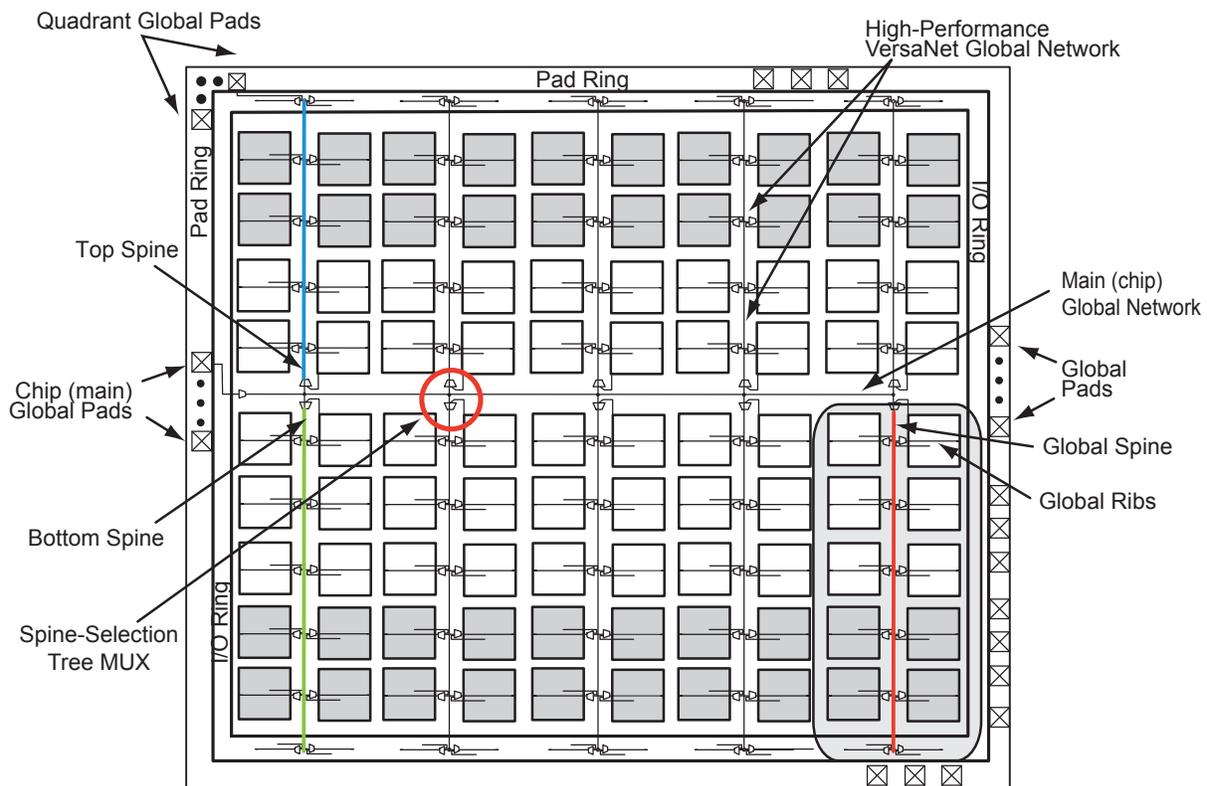


Figure 2-11 • Overview of Fusion VersaNet Global Network

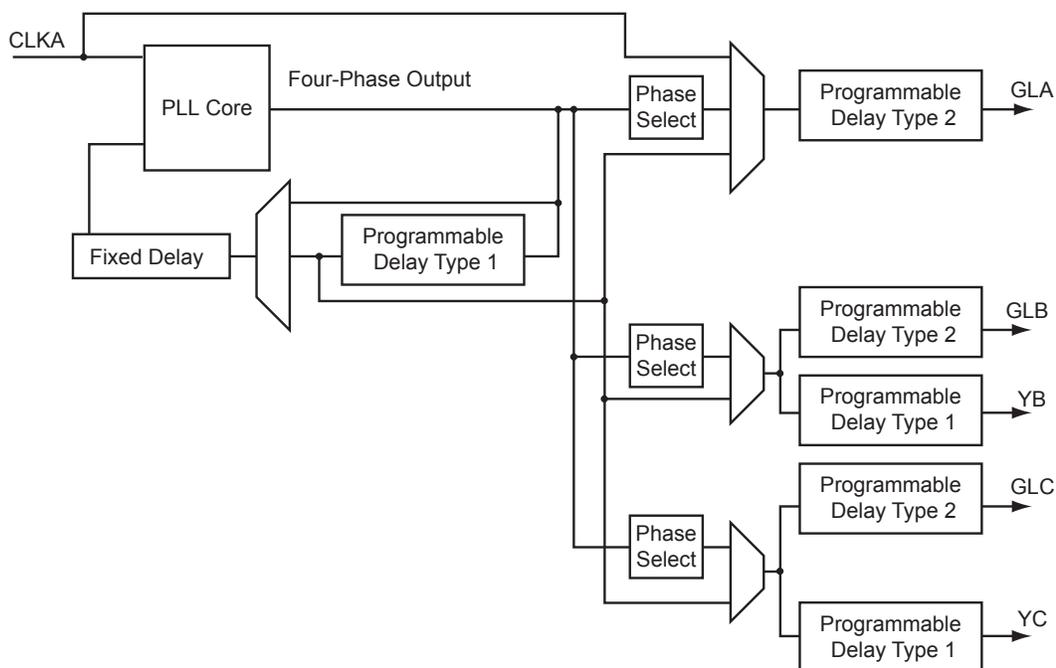
## CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

### CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



*Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.*

**Figure 2-23 • PLL Block**

## FlashROM

Fusion devices have 1 kbit of on-chip nonvolatile flash memory that can be read from the FPGA core fabric. The FlashROM is arranged in eight banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read-back of the FlashROM from the FPGA core (Figure 2-45).

The FlashROM can only be programmed via the IEEE 1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the eight 128-bit banks can be selectively reprogrammed. The FlashROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FlashROM supports a synchronous read and can be read on byte boundaries. The upper three bits of the FlashROM address from the FPGA core define the bank that is being accessed. The lower four bits of the FlashROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

The maximum FlashROM access clock is given in Table 2-25 on page 2-55. Figure 2-46 on page 2-55 shows the timing behavior of the FlashROM access cycle—the address has to be set up on the rising edge of the clock for DOUT to be valid on the next falling edge of the clock.

If the address is unchanged for two cycles:

If the address is unchanged for two cycles:

- D0 becomes invalid  $t_{CK2Q}$  ns after the second rising edge of the clock.
- D0 becomes valid again  $t_{CK2Q}$  ns after the second falling edge.

If the address unchanged for three cycles:

- D0 becomes invalid  $t_{CK2Q}$  ns after the second rising edge of the clock.
- D0 becomes valid again  $t_{CK2Q}$  ns after the second falling edge.
- D0 becomes invalid  $t_{CK2Q}$  ns after the third rising edge of the clock.
- D0 becomes valid again  $t_{CK2Q}$  ns after the third falling edge.

		Byte Number in Bank															
		4 LSB of ADDR (READ)															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bank Number 3 MSB of ADDR (READ)	7																
	6																
	5																
	4																
	3																
	2																
	1																
	0																

Figure 2-45 • FlashROM Architecture

## SRAM and FIFO

All Fusion devices have SRAM blocks along the north side of the device. Additionally, AFS600 and AFS1500 devices have an SRAM block on the south side of the device. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz. The following configurations are available:

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—two read, two write or one read, one write)
- 512×9, 256×18 (two-port RAM—one read and one write)
- Sync write, sync pipelined/nonpipelined read

The Fusion SRAM memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY).

During RAM operation, addresses are sourced by the user logic, and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to [Figure 2-47](#) for more information about the implementation of the embedded FIFO controller.

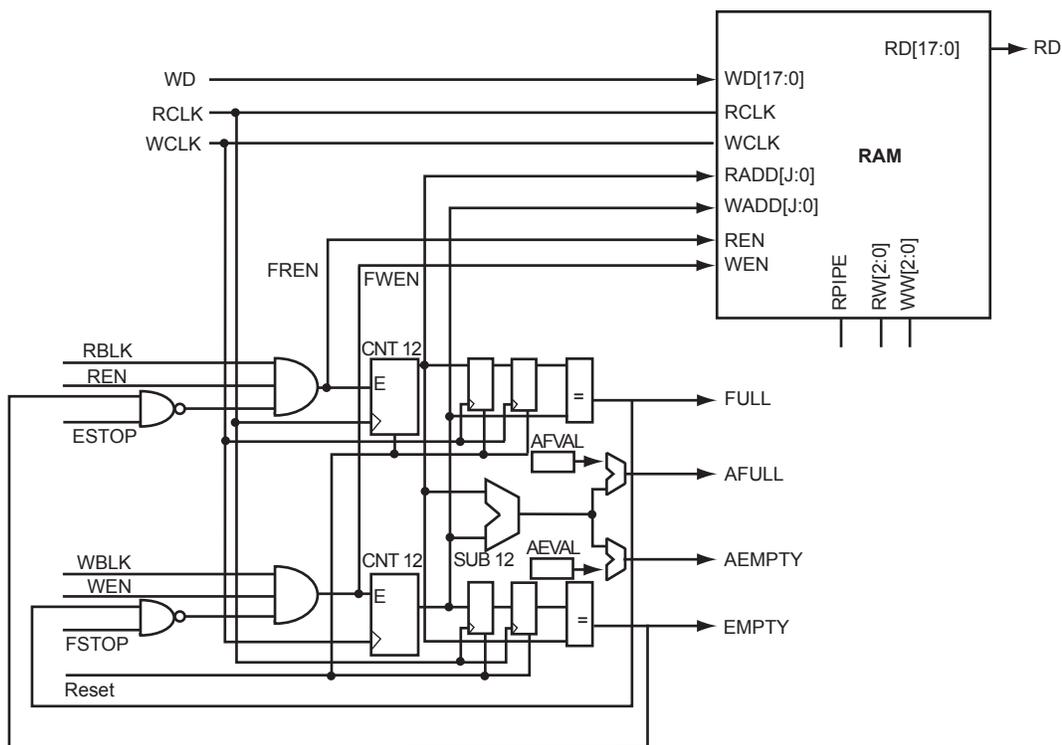
The Fusion architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. This is done with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1. For example, the write size can be set to 256×18 and the read size to 512×9.

Both the write and read widths for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in [Table 2-26](#) on [page 2-58](#).

When a width of one, two, or four is selected, the ninth bit is unused. For example, when writing 9-bit values and reading 4-bit values, only the first four bits and the second four bits of each 9-bit value are addressable for read operations. The ninth bit is not accessible.

Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.



**Figure 2-47 • Fusion RAM Block with Embedded FIFO Controller**

### **Modes of Operation**

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—1 clock edge): In the standard read mode, new data is driven onto the RD bus in the same clock cycle following RA and REN valid. The read address is registered on the read port clock active edge, and data appears at RD after the RAM access time. Setting PIPE to OFF enables this mode.
- Read Pipelined (synchronous—2 clock edges): The pipelined mode incurs an additional clock delay from the address to the data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.
- Write (synchronous—1 clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is High. The setup times of the write address, write enables, and write data are minimal with respect to the write clock. Write and read transfers are described with timing requirements in the "SRAM Characteristics" section on page 2-63 and the "FIFO Characteristics" section on page 2-72.

### **RAM Initialization**

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism (refer to the "JTAG IEEE 1532" section on page 2-227 and the *Fusion SRAM/FIFO Blocks* application note). The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.

**Table 2-51 • Uncalibrated Analog Channel Accuracy\***  
**Worst-Case Extended Temperature Conditions, T<sub>J</sub> = 100°C**

		Total Channel Error (LSB)			Channel Input Offset Error (LSB)			Channel Input Offset Error (mV)			Channel Gain Error (%FSR)		
Analog Pad	Prescaler Range (V)	Neg. Max.	Med.	Pos. Max.	Neg. Max	Med.	Pos. Max.	Neg. Max.	Med.	Pos. Max.	Min.	Typ.	Max.
<b>Positive Range</b>		<b>ADC in 10-Bit Mode</b>											
AV, AC	16	-22	-2	12	-11	-2	14	-169	-32	224	3	0	-3
	8	-40	-5	17	-11	-5	21	-87	-40	166	2	0	-4
	4	-45	-9	24	-16	-11	36	-63	-43	144	2	0	-4
	2	-70	-19	33	-33	-20	66	-66	-39	131	2	0	-4
	1	-25	-7	5	-11	-3	26	-11	-3	26	3	-1	-3
	0.5	-41	-12	8	-12	-7	38	-6	-4	19	3	-1	-3
	0.25	-53	-14	19	-20	-14	40	-5	-3	10	5	0	-4
	0.125	-89	-29	24	-40	-28	88	-5	-4	11	7	0	-5
AT	16	-3	9	15	-4	0	4	-64	5	64	1	0	-1
	4	-10	2	15	-11	-2	11	-44	-8	44	1	0	-1
<b>Negative Range</b>		<b>ADC in 10-Bit Mode</b>											
AV, AC	16	-35	-10	9	-24	-6	9	-383	-96	148	5	-1	-6
	8	-65	-19	12	-34	-12	9	-268	-99	75	5	-1	-5
	4	-86	-28	21	-64	-24	19	-254	-96	76	5	-1	-6
	2	-136	-53	37	-115	-42	39	-230	-83	78	6	-2	-7
	1	-98	-35	8	-39	-8	15	-39	-8	15	10	-3	-10
	0.5	-121	-46	7	-54	-14	18	-27	-7	9	10	-4	-11
	0.25	-149	-49	19	-72	-16	40	-18	-4	10	14	-4	-12
	0.125	-188	-67	38	-112	-27	56	-14	-3	7	16	-5	-14

*Note:* \*Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Gain remains the same.

## Analog Configuration MUX

The ACM is the interface between the FPGA, the Analog Block configurations, and the real-time counter. Libero SoC will generate IP that will load and configure the Analog Block via the ACM. However, users are not limited to using the Libero SoC IP. This section provides a detailed description of the ACM's register map, truth tables for proper configuration of the Analog Block and RTC, as well as timing waveforms so users can access and control the ACM directly from their designs.

The Analog Block contains four 8-bit latches per Analog Quad that are initialized through the ACM. These latches act as configuration bits for Analog Quads. The ACM block runs from the core voltage supply (1.5 V).

Access to the ACM is achieved via 8-bit address and data busses with enables. The pin list is provided in [Table 2-35 on page 2-78](#). The ACM clock speed is limited to a maximum of 10 MHz, more than sufficient to handle the low-bandwidth requirements of configuring the Analog Block and the RTC (sub-block of the Analog Block).

[Table 2-54](#) decodes the ACM address space and maps it to the corresponding Analog Quad and configuration byte for that quad.

**Table 2-54 • ACM Address Decode Table for Analog Quad**

ACMADDR [7:0] in Decimal	Name	Description	Associated Peripheral
0	–	–	Analog Quad
1	AQ0	Byte 0	Analog Quad
2	AQ0	Byte 1	Analog Quad
3	AQ0	Byte 2	Analog Quad
4	AQ0	Byte 3	Analog Quad
5	AQ1	Byte 0	Analog Quad
⋮	⋮	⋮	Analog Quad
36	AQ8	Byte 3	Analog Quad
37	AQ9	Byte 0	Analog Quad
38	AQ9	Byte 1	Analog Quad
39	AQ9	Byte 2	Analog Quad
40	AQ9	Byte 3	Analog Quad
41		Undefined	Analog Quad
⋮	⋮	Undefined	Analog Quad
63		Undefined	RTC
64	COUNTER0	Counter bits 7:0	RTC
65	COUNTER1	Counter bits 15:8	RTC
66	COUNTER2	Counter bits 23:16	RTC
67	COUNTER3	Counter bits 31:24	RTC
68	COUNTER4	Counter bits 39:32	RTC
72	MATCHREG0	Match register bits 7:0	RTC
73	MATCHREG1	Match register bits 15:8	RTC
74	MATCHREG2	Match register bits 23:16	RTC
75	MATCHREG3	Match register bits 31:24	RTC
76	MATCHREG4	Match register bits 39:32	RTC
80	MATCHBITS0	Individual match bits 7:0	RTC

For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.

**Table 2-66 • Internal Temperature Monitor Control Truth Table**

Control Lines B2[0]	PDTMB	Chip Internal Temperature Monitor
0	0	Off
1	1	On

## Features Supported on Pro I/Os

Table 2-72 lists all features supported by transmitter/receiver for single-ended and differential I/Os.

**Table 2-72 • Fusion Pro I/O Features**

Feature	Description
Single-ended and voltage-referenced transmitter features	<ul style="list-style-type: none"> <li>• Hot insertion in every mode except PCI or 5 V input tolerant (these modes use clamp diodes and do not allow hot insertion)</li> <li>• Activation of hot insertion (disabling the clamp diode) is selectable by I/Os.</li> <li>• Weak pull-up and pull-down</li> <li>• Two slew rates</li> <li>• Skew between output buffer enable/disable time: 2 ns delay (rising edge) and 0 ns delay (falling edge); see <a href="#">"Selectable Skew between Output Buffer Enable/Disable Time"</a> on page 2-150 for more information</li> <li>• Five drive strengths</li> <li>• 5 V–tolerant receiver (<a href="#">"5 V Input Tolerance"</a> section on page 2-145)</li> <li>• LVTTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs (<a href="#">"5 V Output Tolerance"</a> section on page 2-149)</li> <li>• High performance (<a href="#">Table 2-77 on page 2-144</a>)</li> </ul>
Single-ended receiver features	<ul style="list-style-type: none"> <li>• Schmitt trigger option</li> <li>• ESD protection</li> <li>• Programmable delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)</li> <li>• High performance (<a href="#">Table 2-77 on page 2-144</a>)</li> <li>• Separate ground planes, GND/GNDQ, for input buffers only to avoid output-induced noise in the input circuitry</li> </ul>
Voltage-referenced differential receiver features	<ul style="list-style-type: none"> <li>• Programmable Delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)</li> <li>• High performance (<a href="#">Table 2-77 on page 2-144</a>)</li> <li>• Separate ground planes, GND/GNDQ, for input buffers only to avoid output-induced noise in the input circuitry</li> </ul>
CMOS-style LVDS, B-LVDS, M-LVDS, or LVPECL transmitter	<ul style="list-style-type: none"> <li>• Two I/Os and external resistors are used to provide a CMOS-style LVDS, B-LVDS, M-LVDS, or LVPECL transmitter solution.</li> <li>• Activation of hot insertion (disabling the clamp diode) is selectable by I/Os.</li> <li>• Weak pull-up and pull-down</li> <li>• Fast slew rate</li> </ul>
LVDS/LVPECL differential receiver features	<ul style="list-style-type: none"> <li>• ESD protection</li> <li>• High performance (<a href="#">Table 2-77 on page 2-144</a>)</li> <li>• Programmable delay: 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)</li> <li>• Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry</li> </ul>



**Table 2-88 • Summary of Maximum and Minimum DC Input Levels Applicable to Extended Temperature Conditions in all I/O Bank Types**

DC I/O Standards	Extended Temperature (K) <sup>1</sup>	
	IIL <sup>2</sup>	IIL <sup>3</sup>
	μA	μA
3.3 V LVTTTL / 3.3 V LVCMOS	15	15
2.5 V LVCMOS	15	15
1.8 V LVCMOS	15	15
1.5 V LVCMOS	15	15
3.3 V PCI	15	15
3.3 V PCI-X	15	15
3.3 V GTL	15	15
2.5 V GTL	15	15
3.3 V GTL+	15	15
2.5 V GTL+	15	15
HSTL (I)	15	15
HSTL (II)	15	15
SSTL2 (I)	15	15
SSTL2 (II)	15	15
SSTL3 (I)	15	15
SSTL3 (II)	15	15

**Notes:**

1. Extended Temperature range ( $-55^{\circ}\text{C} < T_J < 100^{\circ}\text{C}$ )
2. IIL is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
3. IIH is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.

## Single-Ended I/O Characteristics

### 3.3 V LVTTTL / 3.3 V LVCMOS

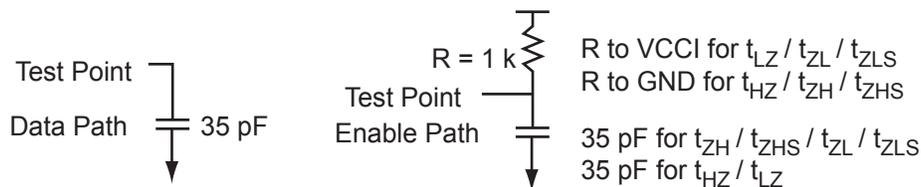
Low-Voltage Transistor–Transistor Logic is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTTL support.

**Table 2-100 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Pro I/O banks

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
<b>Applicable to Pro I/O Banks</b>												
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	15	15
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	15	15
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	15	15
24 mA	-0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	15	15
<b>Applicable to Advanced I/O Banks</b>												
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	15	15
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	15	15
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	15	15
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	15	15
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	15	15
24 mA	-0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	15	15

**Notes:**

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.



**Figure 2-117 • AC Loading**

**Table 2-101 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	$V_{REF}$ (typ.) (V)	$C_{LOAD}$ (pF)
0	3.3	1.4	-	35

Note: \*Measuring point =  $V_{trip}$ . See Table 2-89 on page 2-166 for a complete table of trip points.

### 2.5 V LVCMOS

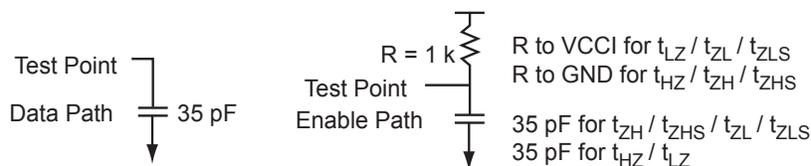
Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

#### Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
<b>Applicable to Pro I/O Banks</b>												
4 mA	-0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	-0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	-0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	-0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	-0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10
<b>Applicable to Advanced I/O Banks</b>												
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	10	10
16 mA	-0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	10	10
24 mA	-0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	10	10

**Notes:**

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.



**Figure 2-118 • AC Loading**

**Table 2-106 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C <sub>LOAD</sub> (pF)
0	2.5	1.2	–	35

**Note:** \*Measuring point =  $V_{trip}$ . See Table 2-89 on page 2-166 for a complete table of trip points.

### 1.8 V LVCMOS

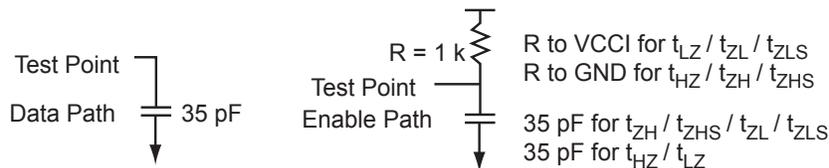
Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and push-pull output buffer.

**Table 2-111 • Minimum and Maximum DC Input and Output Levels**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	II <sub>L</sub> <sup>1</sup>	II <sub>H</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
<b>Applicable to Pro I/O Banks</b>												
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	2	2	11	9	15	15
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	4	4	22	17	15	15
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	6	6	44	35	15	15
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	8	8	51	45	15	15
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	12	12	74	91	15	15
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	16	16	74	91	15	15
<b>Applicable to Advanced I/O Banks</b>												
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	2	2	11	9	15	15
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	4	4	22	17	15	15
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	6	6	44	35	15	15
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	8	8	51	45	15	15
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	12	12	74	91	15	15
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	16	16	74	91	15	15

**Notes:**

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.



**Figure 2-119 • AC Loading**

**Table 2-112 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input Low (V)	Measuring Point* (V)	VREF (typ.) (V)	C <sub>LOAD</sub> (pF)
0	1.8	0.9	-	35

*Note:* \*Measuring point =  $V_{trip}$ . See Table 2-89 on page 2-166 for a complete table of trip points.

## Differential I/O Characteristics

Configuration of the I/O modules as a differential pair is handled by the Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

### LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-132](#). The building blocks of the LVDS transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

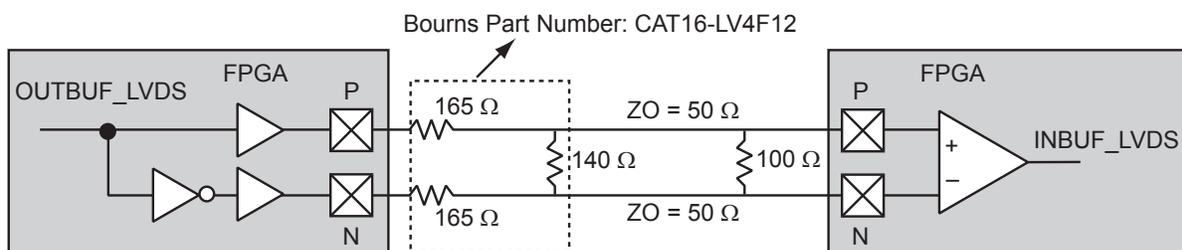


Figure 2-132 • LVDS Circuit Diagram and Board-Level Implementation

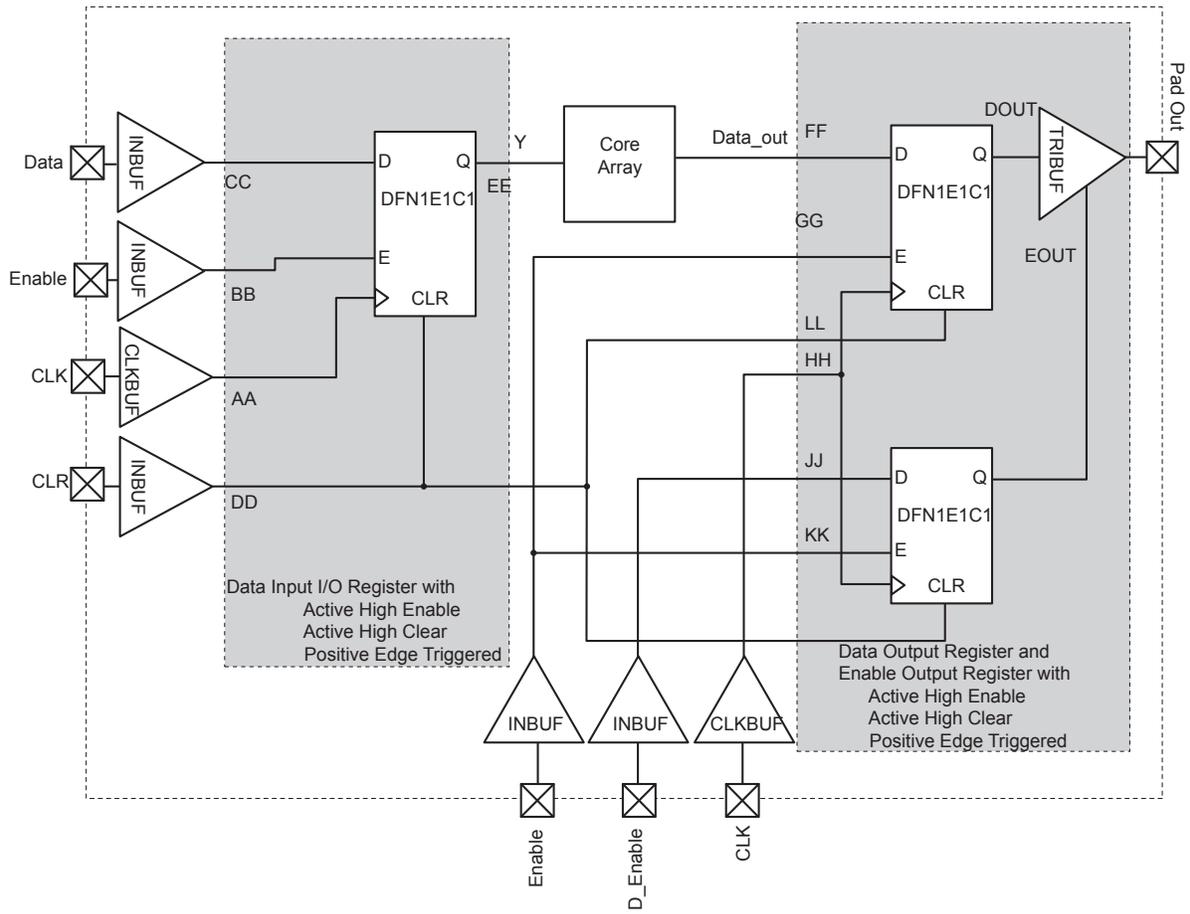
Table 2-157 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL <sup>1</sup>	Output Lower Current	0.65	0.91	1.16	mA
IOH <sup>1</sup>	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIL <sup>2,3</sup>	Input High Leakage Current			10	μA
IIH <sup>2,4</sup>	Input Low Leakage Current			10	μA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350		mV

#### Notes:

1. IOL/IOH defined by I/O diff/(Resistor Network)
2. Currents are measured at 85°C junction temperature.
3. IIL is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
4. IIH is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.

**Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**



**Figure 2-136 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

pump, and eNVM operation. VCCOSC is off only when VCCA is off. VCCOSC must be powered whenever the Fusion device needs to function.

**VCC**                      **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a Fusion device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the Fusion device.

**VCCIBx**                      **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are five (AFS600 and AFS1500) I/O banks on the Fusion devices plus a dedicated VJTAG bank.

Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

**VCCPLA/B**                      **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V, where A and B refer to the PLL. The AFS600 and AFS1500 devices each have two PLLs. Microsemi recommends tying VCCPLX to VCC and using proper filtering circuits to decouple VCC noise from PLL.

If unused, VCCPLA/B should be tied to GND.

**VCOMPLA/B**                      **Ground for West and East PLL**

VCOMPLA is the ground of the west PLL (CCC location F) and VCOMPLB is the ground of the east PLL (CCC location C).

**VJTAG**                      **JTAG Supply Voltage**

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a Fusion device is in a JTAG chain of interconnected boards and it is desired to power down the board containing the Fusion device, this may be done provided both VJTAG and VCC to the Fusion part remain powered; otherwise, JTAG signals will not be able to transition the Fusion device, even in bypass mode.

**VPUMP**                      **Programming Supply Voltage**

Fusion devices support single-voltage ISP programming of the configuration flash and FlashROM. For programming, VPUMP should be in the 3.3 V +/-5% range. During normal device operation, VPUMP can be left floating or can be tied to any voltage between 0 V and 3.6 V.

When the VPUMP pin is tied to ground, it shuts off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01  $\mu$ F and 0.33  $\mu$ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

## User-Defined Supply Pins

**VREF**                      **I/O Voltage Reference**

Reference voltage for I/O minibanks. Both AFS600 and AFS1500 (north bank only) support Microsemi Pro I/Os. These I/O banks support voltage reference standard I/O. The  $V_{REF}$  pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated as the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One  $V_{REF}$  pin can support the number of I/Os available in its minibank.