



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, SCI, SPI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51111adfm-3a

Table 1.1 Outline of Specifications (3/3)

Classification	Module/Function	Description
Communication function	USB 2.0 host/function module (USBc)	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. • Host (32-Kbyte or more ROM)/function module: 1 port • Compliant with USB version 2.0 • Transfer speed: Full-speed (12 Mbps), low-speed (1.5 Mbps) • OTG (On-The-Go) is supported. • Isochronous transfer is supported. • BC (Battery Charger) is supported.
12-bit A/D converter (S12ADb)		• 1 unit (1 unit × 14 channels) • 12-bit resolution • Minimum conversion time: 1.0 μs per channel when the ADCLK is operating at 32 MHz • Operating modes - Scan mode (single scan mode, continuous scan mode, and group scan mode) • Double trigger mode (duplication of A/D conversion data) • A/D conversion start conditions - A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC
Temperature sensor (TEMPSA)		• 1 channel • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter.
D/A converter (DA)		• 2 channels • 8-bit resolution • Output voltage: 0 V to VCC
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB first or MSB first communications is selectable.
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Unique ID		32-byte ID code for the MCU
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 3.6 V: 32 MHz
Supply current		3.2 mA at 32 MHz (typ.)
Operating temperature range		D version: -40 to +85°C, G version: -40 to +105°C
Packages		64-pin LFQFP (PLQP0064KB-A) 10 × 10 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch 64-pin WFLGA (PWLGA0064KA-A) 5 × 5 mm, 0.5 mm pitch 48-pin LFQFP (PLQP0048KB-A) 7 × 7 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch 40-pin HWQFN (PWQN0040KC-A) 6 × 6 mm, 0.50 mm pitch 36-pin WFLGA (PWLGA0036KA-A) 4 × 4 mm, 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Table 1.4 Pin Functions (3/3)

Classifications	Pin Name	I/O	Description
USB 2.0 host/ function module	USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver.
	USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver.
	USB0_VBUS	Input	USB cable connection monitor pin.
	USB0_EXICEN	Output	Low-power control signal for the OTG chip.
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for the OTG chip.
	USB0_OVRCURA, USB0_OVRCURB	Input	External overcurrent detection pins.
	USB0_ID	Input	Mini-AB connector ID input pin during operation in OTG mode.
12-bit A/D converter	AN000 to AN004, AN006, AN008 to AN015	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.
I/O ports	P03, P05	I/O	2-bit input/output pins.
	P14 to P17	I/O	4-bit input/output pins.
	P26, P27	I/O	2-bit input/output pins.
	P30 to P32, P35	I/O	4-bit input/output pins (P35 input pin).
	P40 to P44, P46	I/O	6-bit input/output pins.
	P54, P55	I/O	2-bit input/output pins.
	PA0, PA1, PA3, PA4, PA6	I/O	5-bit input/output pins.
	PB0, PB1, PB3, PB5 to PB7	I/O	6-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH7	Input	1-bit input pin.
	PJ6, PJ7	I/O	2-bit input/output pins.

Note 1. For external clock input.

Table 1.8 List of Pins and Pin Functions (40-Pin HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC)	Communication (SCle, SCIf, RSPI, RIIC, USB)	Others
40	AVCC0				

Note 1. Not 5 V tolerant.

Note 2. The power source of the I/O buffer for these pins is AVCC0.

2. CPU

Figure 2.1 shows the register set of the CPU.

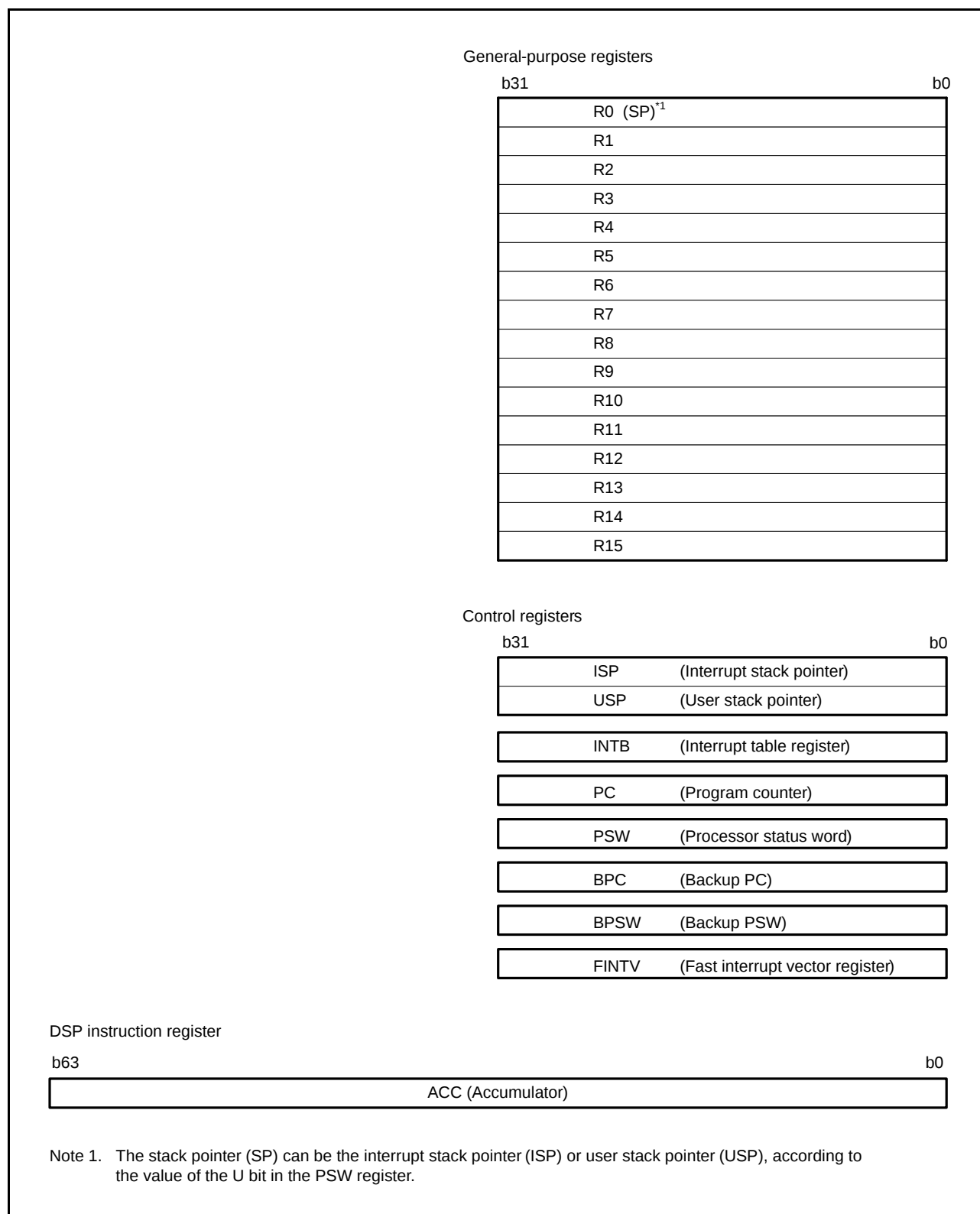


Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (2/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 7026h	ICU	Interrupt Request Register 038	IR038	8	8	2 ICLK
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK
0008 703Fh	ICU	Interrupt Request Register 063	IR063	8	8	2 ICLK
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK
0008 7058h	ICU	Interrupt Request Register 088	IR088	8	8	2 ICLK
0008 7059h	ICU	Interrupt Request Register 089	IR089	8	8	2 ICLK
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8	2 ICLK
0008 705Ch	ICU	Interrupt Request Register 092	IR092	8	8	2 ICLK
0008 705Dh	ICU	Interrupt Request Register 093	IR093	8	8	2 ICLK
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (15/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2 or 3 PCLKB
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3 or 4 PCLKB
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLK or more
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLK or more
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	16	3 or 4 PCLKB
000A 0018h	USB0	D0FIFO Port Register	D0FIFO	16	16	3 or 4 PCLKB
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	16	3 or 4 PCLKB
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3 or 4 PCLKB
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3 or 4 PCLKB
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3 or 4 PCLKB
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3 or 4 PCLKB
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3 or 4 PCLKB
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3 or 4 PCLKB
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more
000A 0090h	USB0	PIPE1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more
000A 0092h	USB0	PIPE1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more
000A 0094h	USB0	PIPE2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more
000A 0096h	USB0	PIPE2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $2.7\text{ V} \leq AV_{SS0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	$V_{CC} \times 0.7$	—	5.8	V	
	Ports P16, P17, port PA6, port PB0 (5 V tolerant)		$V_{CC} \times 0.8$	—	5.8		
	Ports P03, P05, ports P14, P15, ports P26, P27, ports P30 to P32, P35, ports P54, P55, ports PA0, PA1, PA3, PA4, ports PB1, PB3, PB5 to PB7, ports PC2 to PC7, ports PE0 to PE7, port PH7, RES#		$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$		
	RIIC input pin (except for SMBus)	V_{IL}	-0.3	—	$V_{CC} \times 0.3$		
	Other than RIIC input pin		-0.3	—	$V_{CC} \times 0.2$		
	RIIC input pin (except for SMBus)	ΔV_T	$V_{CC} \times 0.05$	—	—		
	Other than RIIC input pin		$V_{CC} \times 0.1$	—	—		
Input voltage (except for Schmitt trigger input pins)	MD	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	XTAL (external clock input)		$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$		
	Ports P40 to P44, P46, ports PJ6, PJ7		$AV_{CC0} \times 0.7$	—	$AV_{CC0} + 0.3$		
	RIIC input pin (SMBus)		2.1	—	$V_{CC} + 0.3$		
	MD	V_{IL}	-0.3	—	$V_{CC} \times 0.1$		
	XTAL (external clock input)		-0.3	—	$V_{CC} \times 0.2$		
	Ports P40 to P44, P46, ports PJ6, PJ7		-0.3	—	$AV_{CC0} \times 0.3$		
	RIIC input pin (SMBus)		-0.3	—	0.8		

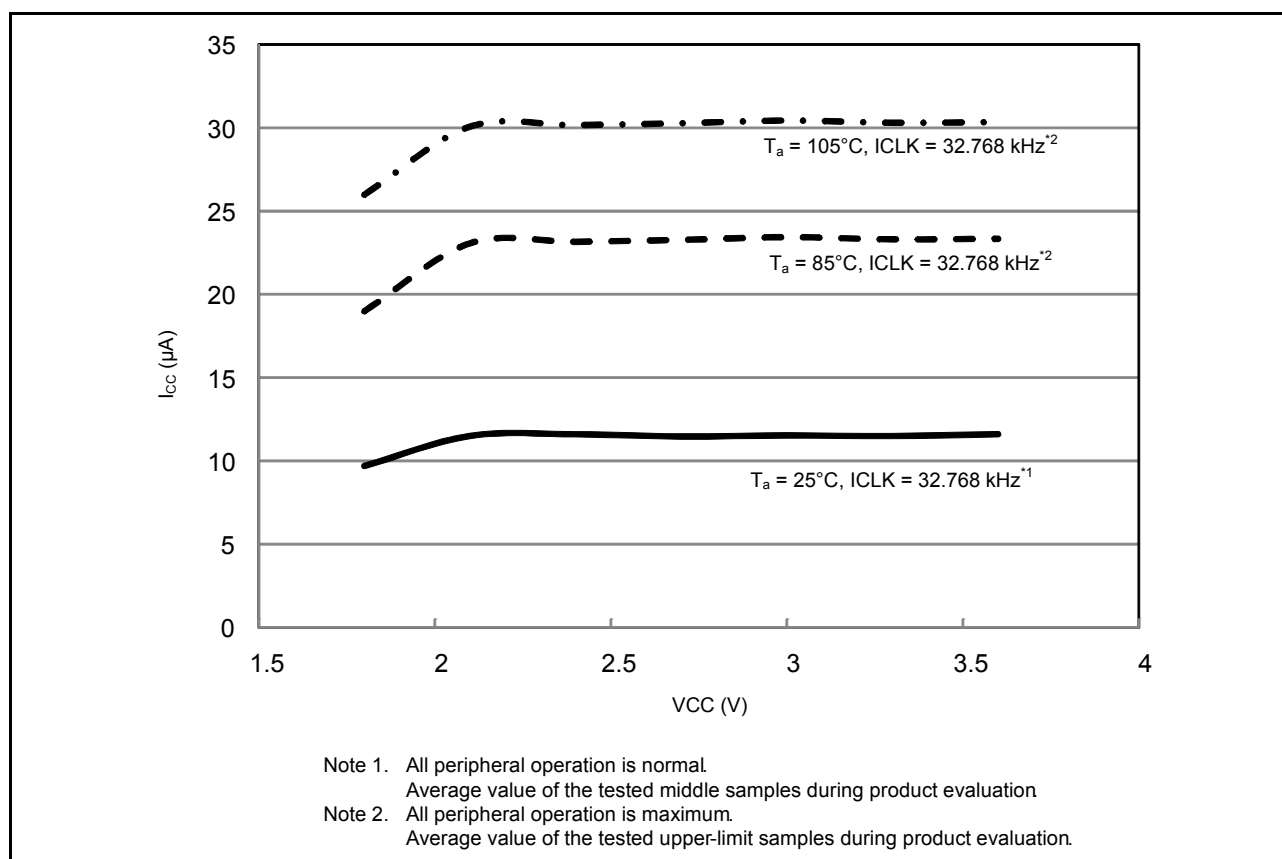


Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

[128-Kbyte or less flash memory]

Table 5.9 DC Characteristics (7)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $V_{SS} = AVSS0 = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

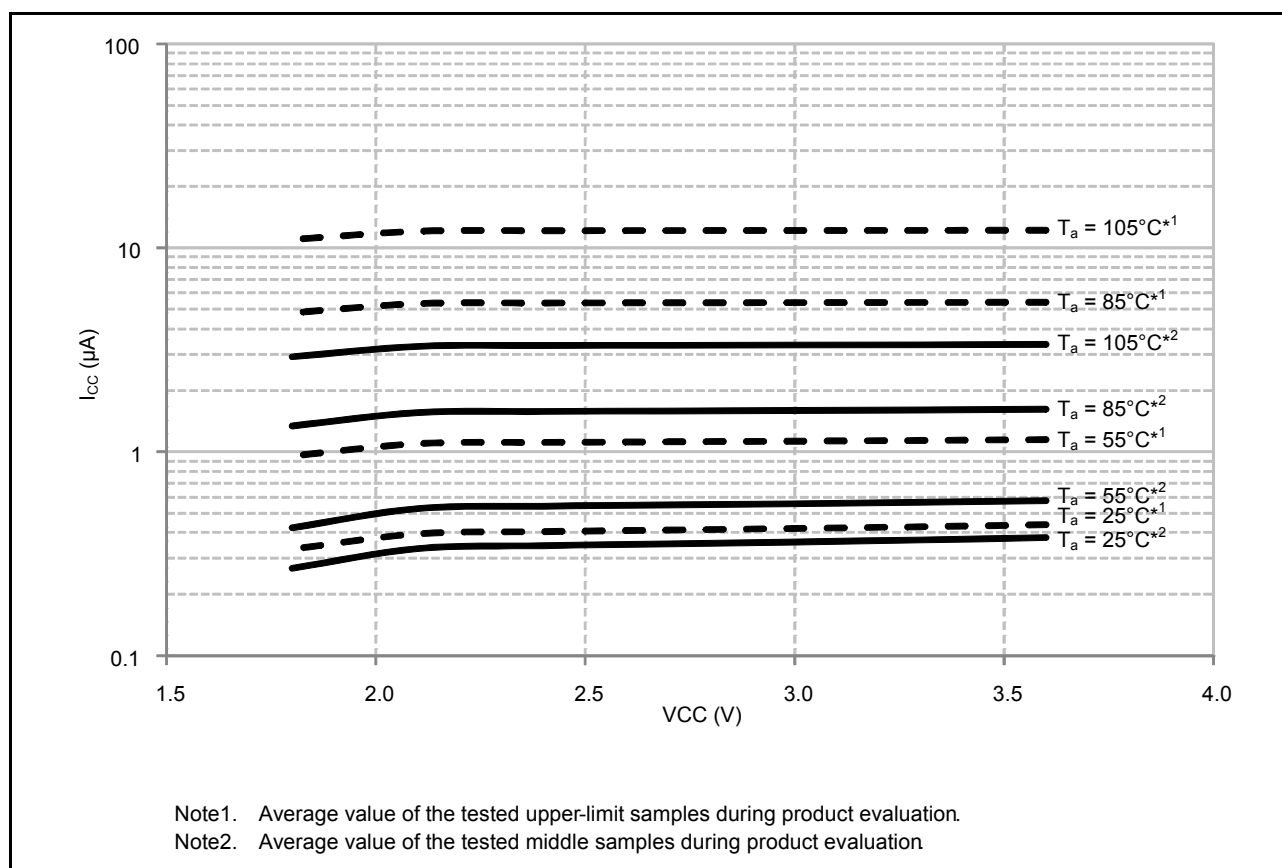
Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	$T_a = 25^\circ\text{C}$	I_{CC}	0.35	0.53	μA	
		$T_a = 55^\circ\text{C}$		0.58	1.45		
		$T_a = 85^\circ\text{C}$		1.60	7.30		
		$T_a = 105^\circ\text{C}$		3.30	16.50		
	Increment for RTC operation*4			0.31	—		RCR3.RTCDV[2:0] = 010b
				1.09	—		RCR3.RTCDV[2:0] = 100b
	Increment for IWDG operation			0.37	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. The IWDG and LVD are stopped.

Note 3. $V_{CC} = 3.3\text{ V}$.

Note 4. Includes the oscillation circuit.

**Figure 5.7 Voltage Dependency in Software Standby Mode (Reference Data)**

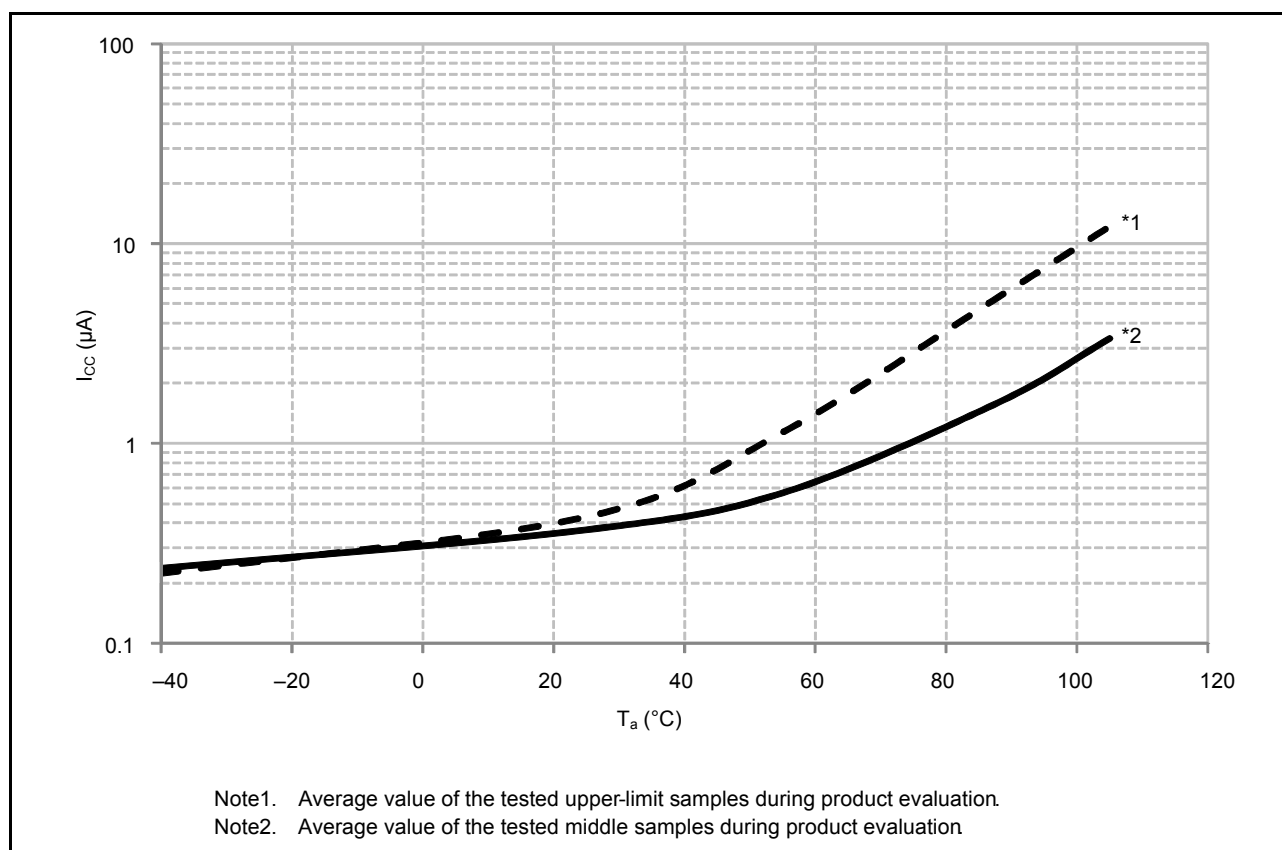


Figure 5.8 Temperature Dependency in Software Standby Mode (Reference Data)

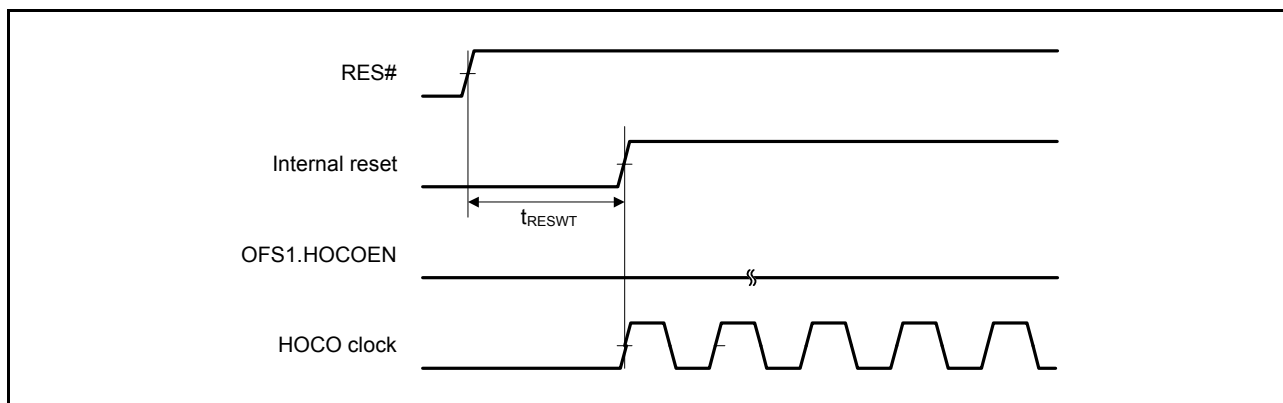


Figure 5.27 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

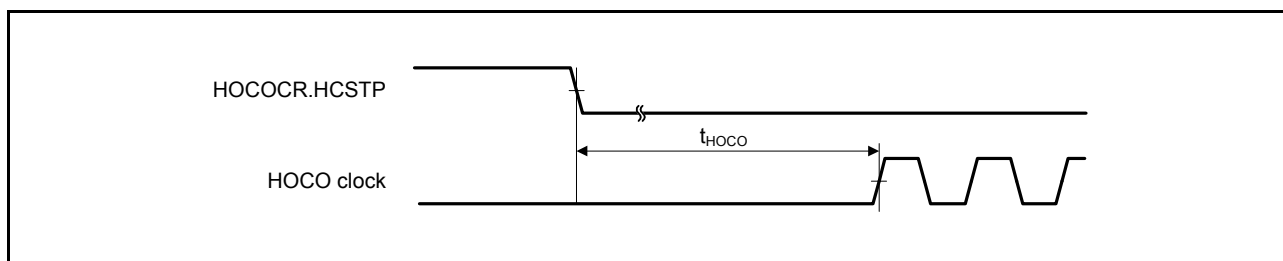


Figure 5.28 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

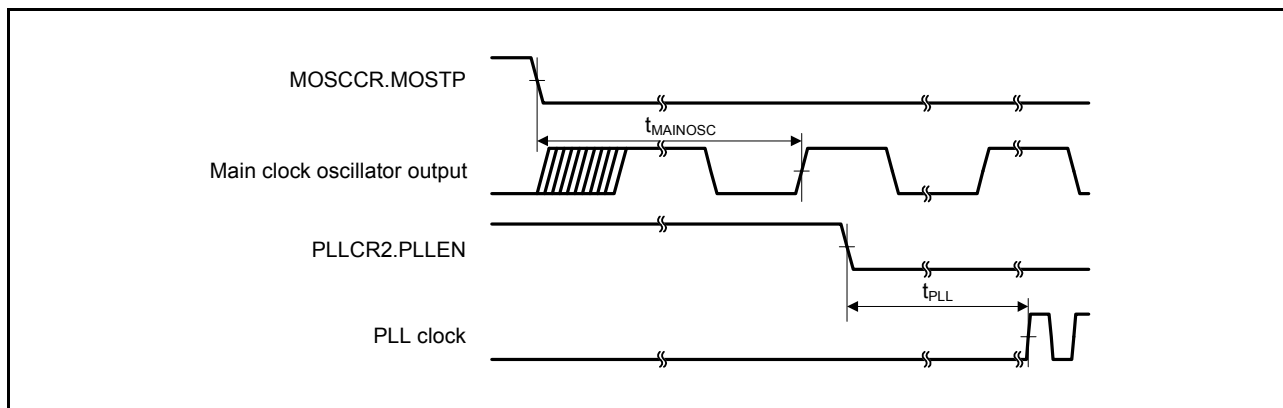


Figure 5.29 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

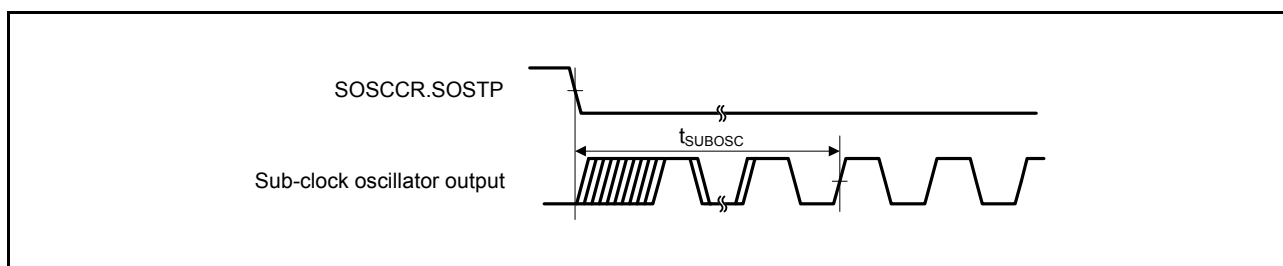


Figure 5.30 Sub-Clock Oscillation Start Timing

Table 5.27 Timing of Recovery from Low Power Consumption Modes (2)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.34
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	3	4	μs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	65	85	μs	
		Sub-clock oscillator operating		t_{SBYSC}	—	600	750	μs	
		HOCO clock oscillator operating*6		t_{SBYHO}	—	40	50	μs	
		LOCO clock oscillator operating		t_{SBYLO}	—	4.8	7	μs	

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. This applies when only the oscillator listed in each item is operating and the other oscillators are stopped.

Note 2. When the frequency of the crystal is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 3. When the frequency of PLL is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 4. When the frequency of the external clock is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 5. When the frequency of PLL is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 6. When the frequency of HOCO is 8 MHz.

When the high-speed clock oscillator wait control register (HOCOWTCR) is set to 05h.

Table 5.28 Timing of Recovery from Low Power Consumption Modes (3)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	μs	Figure 5.34

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

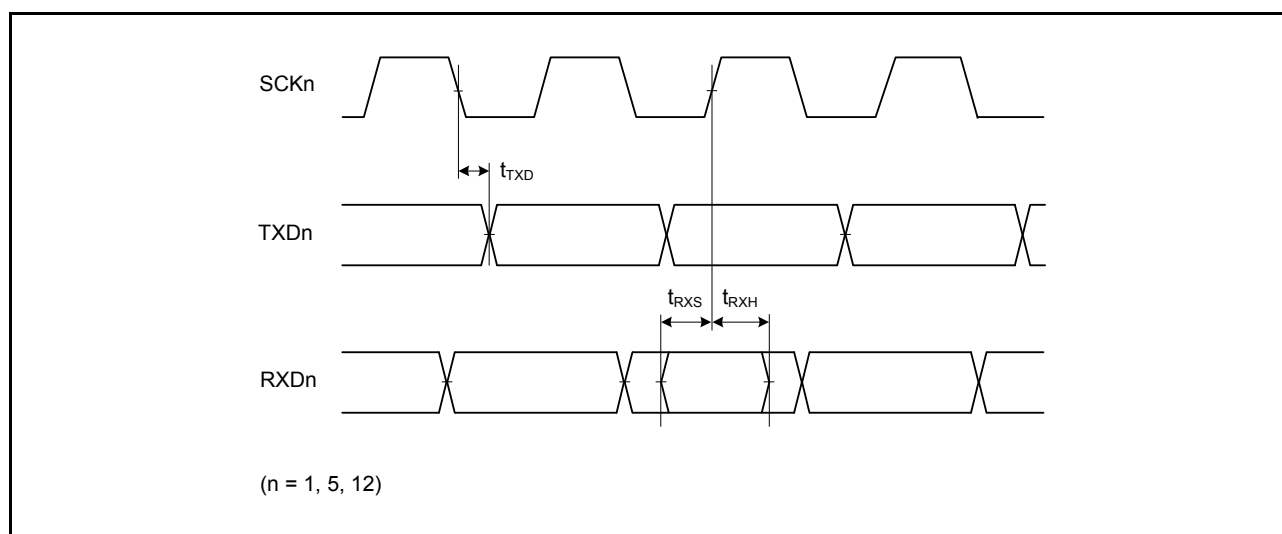


Figure 5.43 SCI Input/Output Timing: Clock Synchronous Mode

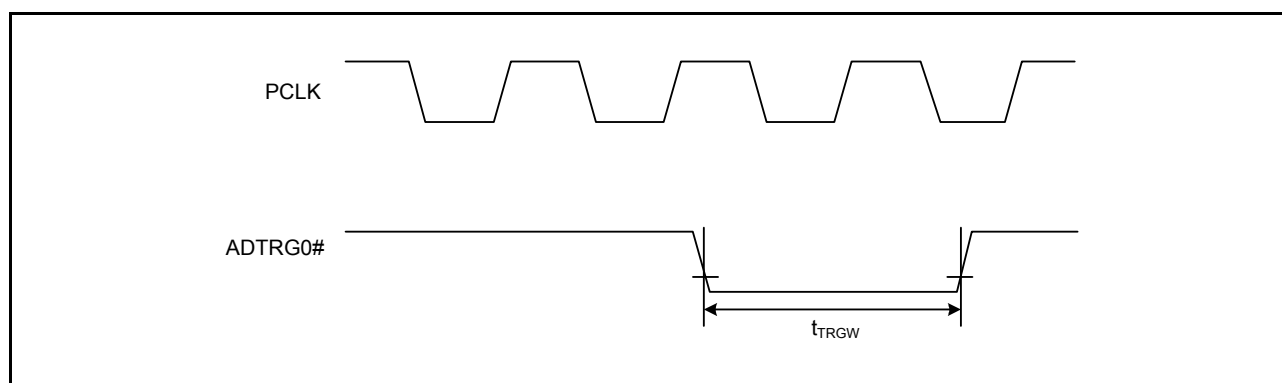


Figure 5.44 A/D Converter External Trigger Input Timing

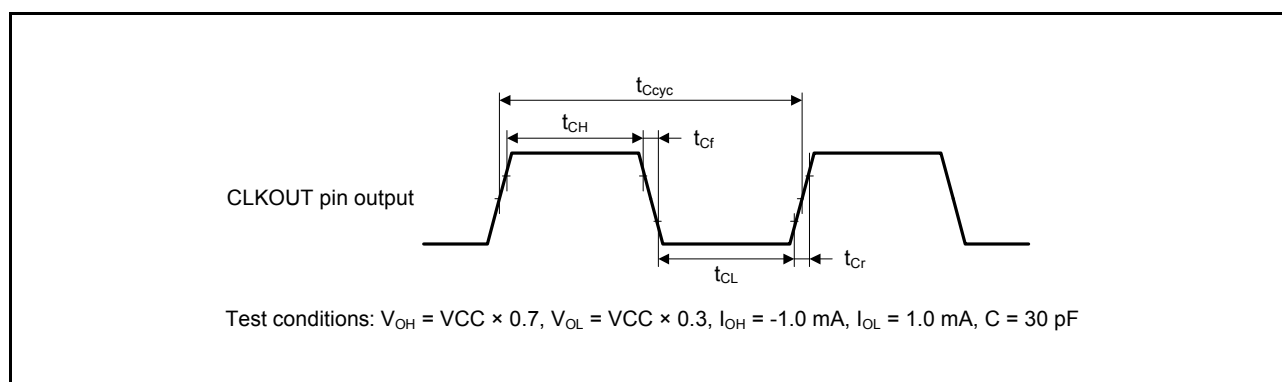


Figure 5.45 CLKOUT Output Timing

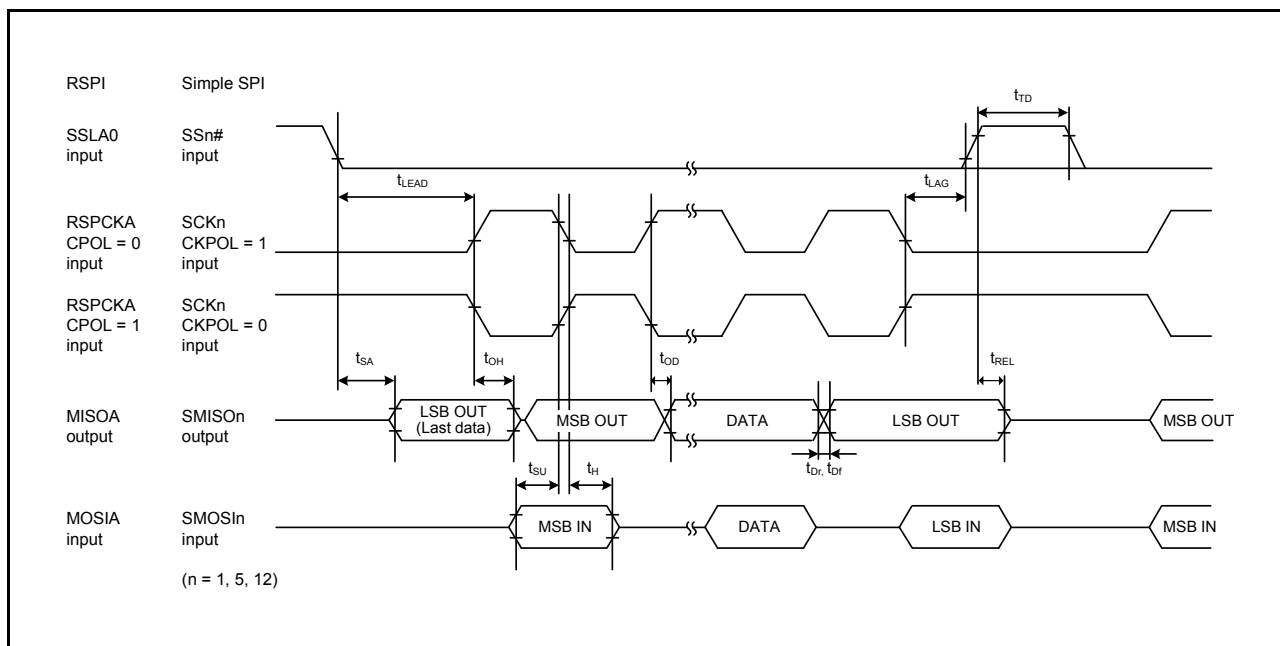


Figure 5.52 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

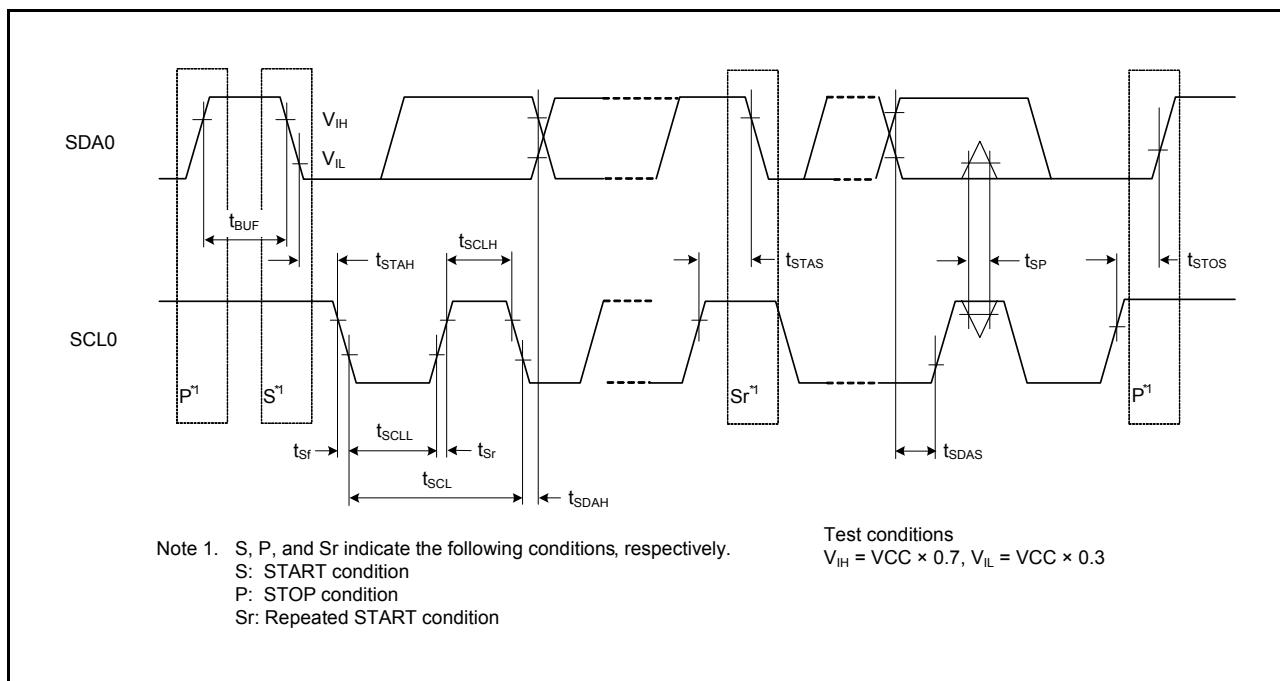


Figure 5.53 I2C Bus Interface Input/Output Timing and Simple I2C Bus Interface Input/Output Timing

Table 5.39 A/D Conversion Characteristics (2)

Conditions: $2.4\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $2.4\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $2.4\text{ V} \leq V_{REFH0} \leq AV_{CC0}$, $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		4	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 1.0 kΩ	2.062 (0.625)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 09h
		2.750 (1.313)*2	—	—	μs	Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±6.0	LSB	
Full-scale error		—	±1.25	±6.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.40 A/D Conversion Characteristics (3)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $1.8\text{ V} \leq V_{REFH0} \leq AV_{CC0}$, $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5.0 kΩ	4.875 (1.250)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 09h
		6.250 (2.625)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±24.0	LSB	
Full-scale error		—	±1.25	±24.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.75	±32.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.25	±12.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

5.8 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.45 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	1.35	1.50	1.65	V	Figure 5.58, Figure 5.59
	Voltage detection circuit (LVD1)*1	V _{det1_4}	3.00	3.10	3.20	V	Figure 5.60 At falling edge VCC
		V _{det1_5}	2.91	3.00	3.09		
		V _{det1_6}	2.81	2.90	2.99		
		V _{det1_7}	2.70	2.79	2.88		
		V _{det1_8}	2.60	2.68	2.76		
		V _{det1_9}	2.50	2.58	2.66		
		V _{det1_A}	2.40	2.48	2.56		
		V _{det1_B}	1.99	2.06	2.13		
		V _{det1_C}	1.90	1.96	2.02		
		V _{det1_D}	1.80	1.86	1.92		

Note: • These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol $V_{\text{det1_n}}$ denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Table 5.46 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Voltage detection circuit (LVD2)*1	V _{det2_0}	2.71	2.90	3.09	V	Figure 5.61 At falling edge VCC
		V _{det2_1}	2.43	2.60	2.77		
		V _{det2_2}	1.87	2.00	2.13		
		V _{det2_3} *2	1.69	1.80	1.91		
Wait time after power-on reset cancellation	At normal startup*3	t _{POR}	—	9.1	—	ms	Figure 5.59
	During fast startup time*4	t _{POR}	—	1.6	—		
Wait time after voltage monitoring 1 reset cancellation	Power-on voltage monitoring 1 reset disabled*3	t _{LVD1}	—	568	—	μs	Figure 5.60
	Power-on voltage monitoring 1 reset enabled*4		—	100	—		
Wait time after voltage monitoring 2 reset cancellation		t _{LVD2}	—	100	—	μs	Figure 5.61
Response delay time		t _{det}	—	—	350	μs	Figure 5.58
Minimum VCC down time*5		t _{VOFF}	350	—	—	μs	Figure 5.58, VCC = 1.0 V or above
Power-on reset enable time		t _{W(POR)}	1	—	—	ms	Figure 5.59, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		T _{d(E-A)}	—	—	300	μs	Figure 5.60, Figure 5.61
Hysteresis width (LVD1 and LVD2)		V _{LVH}	—	70	—	mV	Vdet1_4 selected
			—	60	—		Vdet1_5 to 9, LVD2 selected
			—	50	—		When selection is from among Vdet1_A to B.
			—	40	—		When selection is from among Vdet1_C to D.

Note: • These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol $V_{\text{det2_n}}$ denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.

Note 2. $V_{\text{det2_3}}$ selection can be used only when the CMPA2 pin input voltage is selected and cannot be used when the power supply voltage (VCC) is selected.

Note 3. When OFS1.(STUPLVD1REN, FASTSTUP) = 11b.

Note 4. When OFS1.(STUPLVD1REN, FASTSTUP) $\neq$ 11b.

Note 5. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det0} , V_{det1} , and V_{det2} for the POR/LVD.

5.9 Oscillation Stop Detection Timing

Table 5.47 Oscillation Stop Detection Circuit Characteristics

Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.62

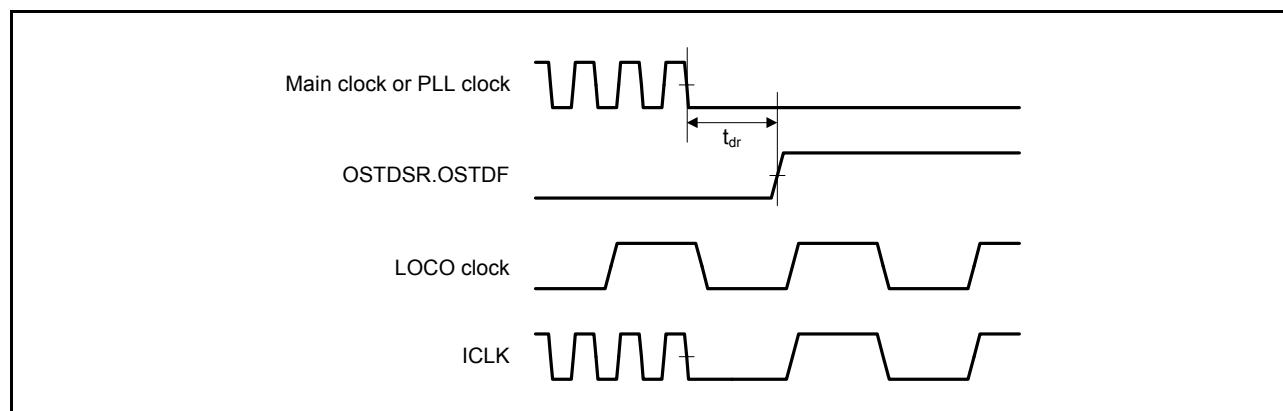


Figure 5.62 Oscillation Stop Detection Timing

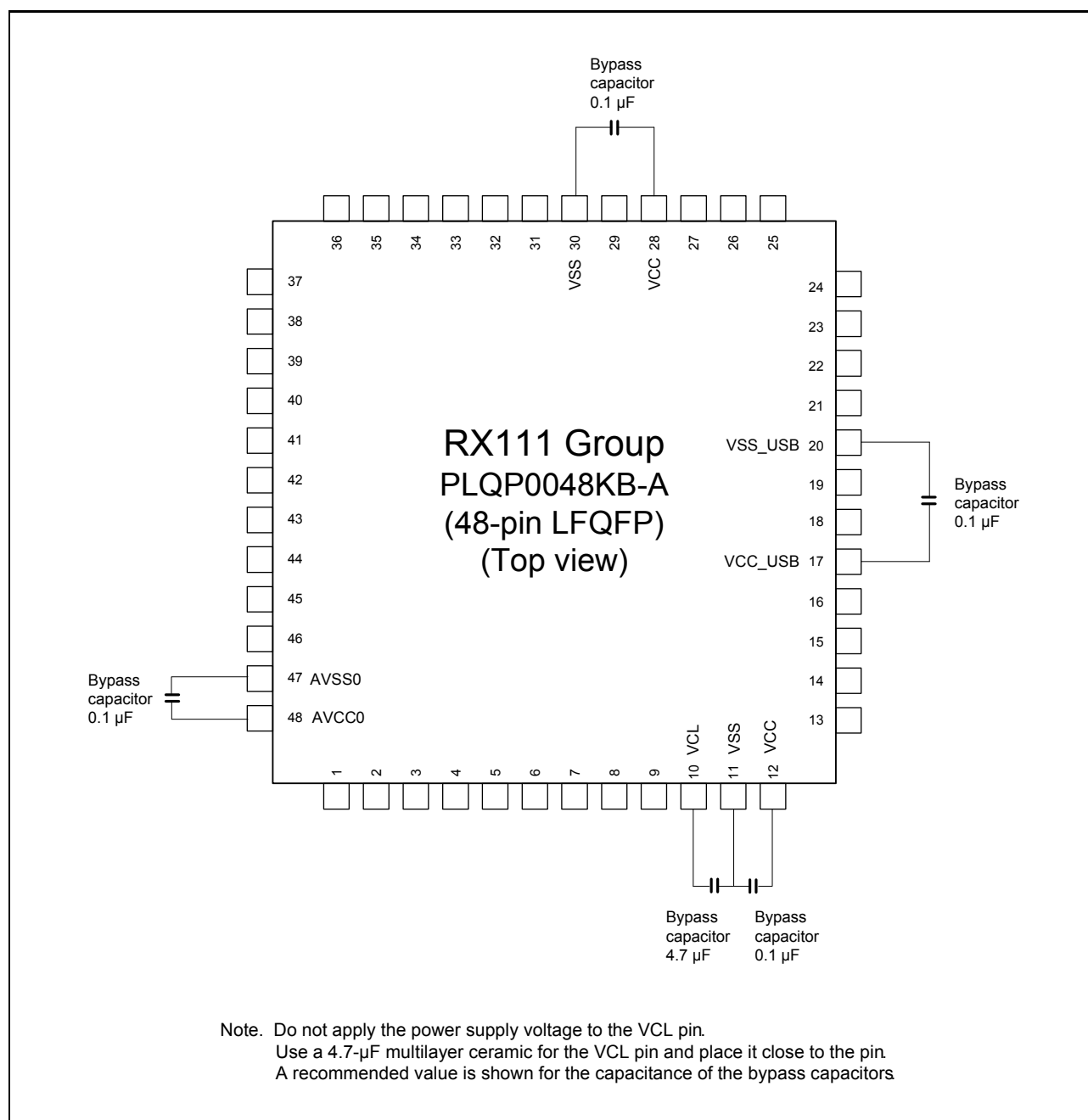


Figure 5.64 Connecting Capacitors (48-pin LQFP)

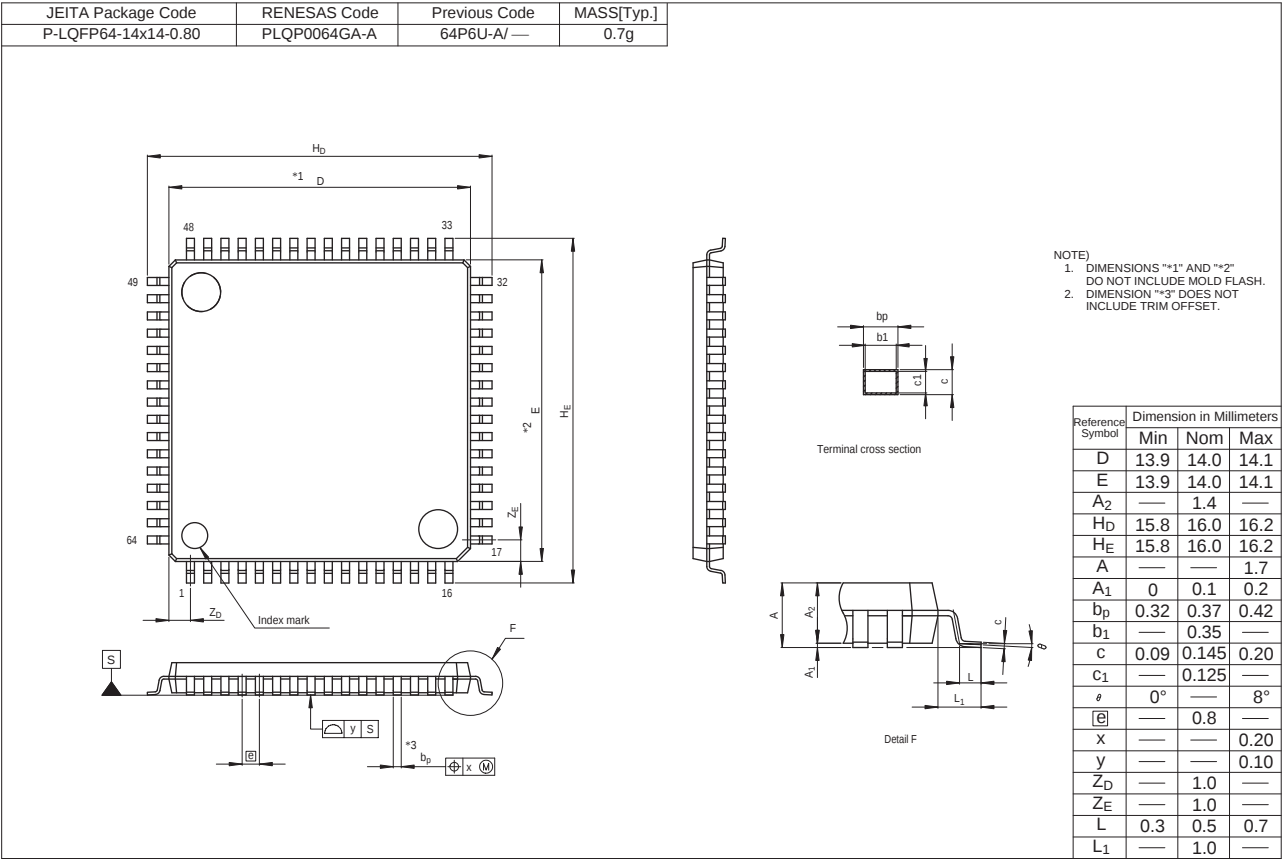


Figure B 64-Pin LQFP (PLQP0064GA-A)

NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.