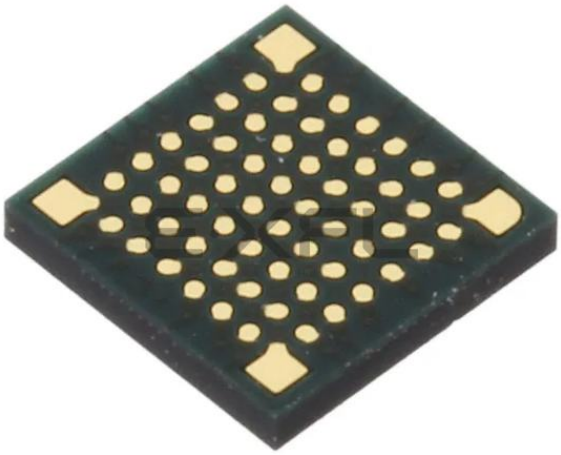
# Renesas Electronics America Inc - R5F51111ADLF#UA Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, SCI, SPI, USB OTG |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 46 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 10K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 14x12b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-WFLGA |
| Supplier Device Package | 64-FLGA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51111adlf-ua |

## 1.4 Pin Functions

Table 1.4 lists the pin functions.

**Table 1.4 Pin Functions (1/3)**

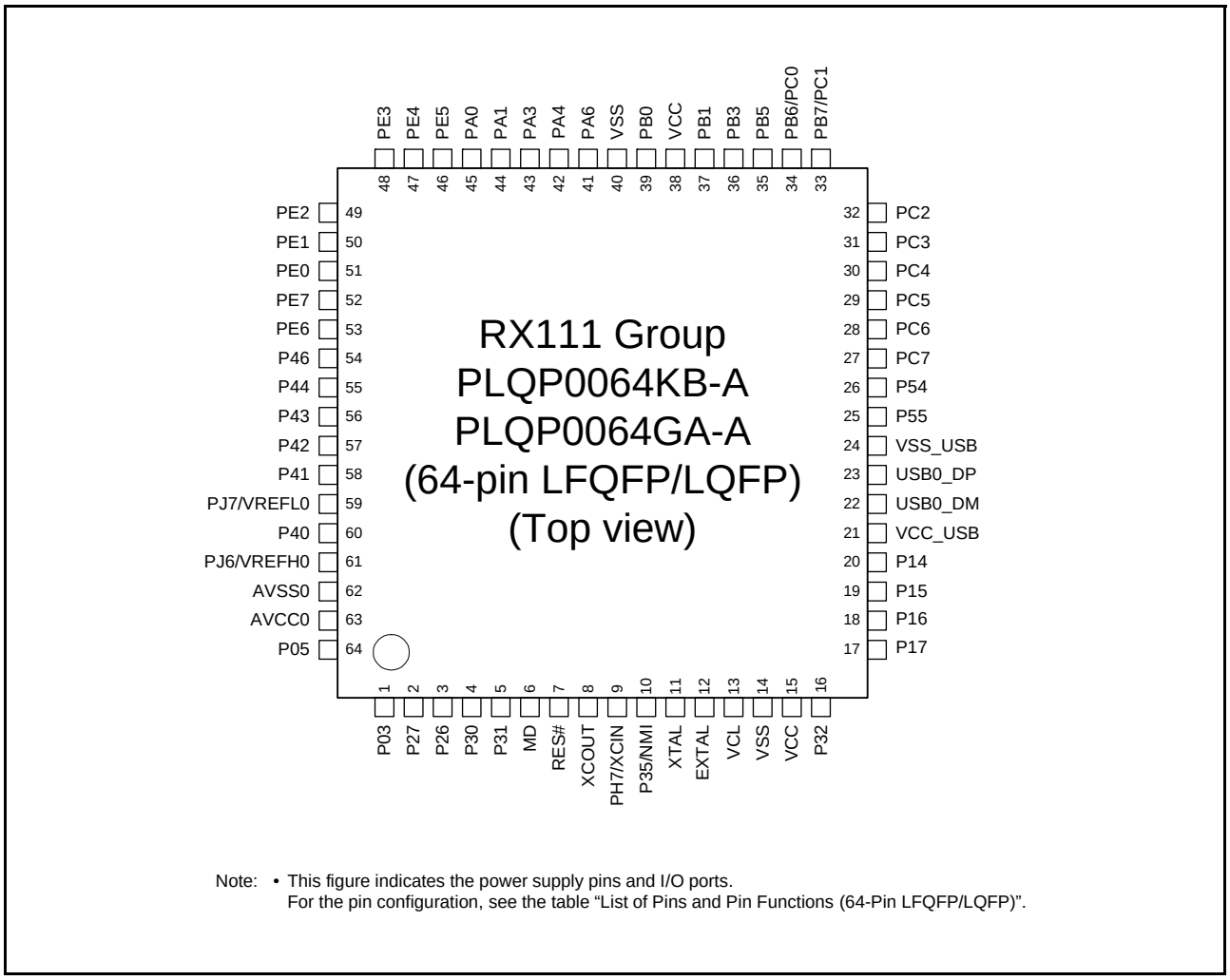
| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Power supply | VCC | Input | Power supply pin. Connect it to the system power supply. |
| | VCL | — | Connect this pin to the VSS pin via the 4.7 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| | VCC_USB | Input | Power supply pin for USB. Connect this pin to VCC. |
| | VSS_USB | Input | Ground pin for USB. Connect this pin to VSS. |
| Analog power supply | AVCC0 | Input | Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC when not using the 12-bit A/D converter. |
| | AVSS0 | Input | Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS when not using the 12-bit A/D converter. |
| | VREFH0 | Input | Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC when not using the 12-bit A/D converter. |
| | VREFL0 | Input | Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS when not using the 12-bit A/D converter. |
| Clock | XTAL | Output/ Input *1 | Pins for connecting a crystal. An external clock can be input through the XTAL pin. |
| | EXTAL | Input | |
| | XCIN | Input | Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT. |
| | XCOUT | Output | |
| | CLKOUT | Output | Clock output pin. |
| Operating mode control | MD | Input | Pin for setting the operating mode. The signal levels on this pin must not be changed during operation. |
| | UB# | Input | Pin used for boot mode (USB interface). |
| | UPSEL | Input | Pin used for boot mode (USB interface). |
| System control | RES# | Input | Reset pin. This MCU enters the reset state when this signal goes low. |
| CAC | CACREF | Input | Input pin for the clock frequency accuracy measurement circuit. |
| On-chip emulator | FINED | I/O | FINE interface pin. |
| LVD | CMPA2 | Input | Detection target voltage pin for voltage detection 2 |
| Interrupts | NMI | Input | Non-maskable interrupt request pin. |
| | IRQ0 to IRQ7 | Input | Interrupt request pins. |
| Multi-function timer pulse unit 2 | MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins. |
| | MTIOC1A, MTIOC1B | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins. |
| | MTIOC2A, MTIOC2B | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins. |
| | MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins. |
| | MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D | I/O | The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins. |
| | MTIC5U, MTIC5V, MTIC5W | Input | The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins. |
| | MTCLKA, MTCLKB, MTCLKC, MTCLKD | Input | Input pins for the external clock. |
| Port output enable 2 | POE0# to POE3#, POE8# | Input | Input pins for request signals to place the MTU pins in the high impedance state. |

**Table 1.4 Pin Functions (2/3)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Realtime clock | RTCOUT | Output | Output pin for the 1-Hz/64-Hz clock. |
| Serial communications interface (SCIe) | • Asynchronous mode/clock synchronous mode | | |
| | SCK1, SCK5 | I/O | Input/output pins for the clock. |
| | RXD1, RXD5 | Input | Input pins for received data. |
| | TXD1, TXD5 | Output | Output pins for transmitted data. |
| | CTS1#, CTS5# | Input | Input pins for controlling the start of transmission and reception. |
| | RTS1#, RTS5# | Output | Output pins for controlling the start of transmission and reception. |
| Serial communications interface (SCIe) | • Simple $I^2C$ mode | | |
| | SSCL1, SSCL5 | I/O | Input/output pins for the $I^2C$ clock. |
| | SSDA1, SSDA5 | I/O | Input/output pins for the $I^2C$ data. |
| | • Simple SPI mode | | |
| | SCK1, SCK5 | I/O | Input/output pins for the clock. |
| | SMISO1, SMISO5 | I/O | Input/output pins for slave transmit data. |
| | SMOSI1, SMOSI5 | I/O | Input/output pins for master transmit data. |
| | SS1#, SS5# | Input | Chip-select input pins. |
| Serial communications interface (SCIf) | • Asynchronous mode/clock synchronous mode | | |
| | SCK12 | I/O | Input/output pin for the clock. |
| | RXD12 | Input | Input pin for receiving data. |
| | TXD12 | Output | Output pin for transmitting data. |
| | CTS12# | Input | Input pin for controlling the start of transmission and reception. |
| | RTS12# | Output | Output pin for controlling the start of transmission and reception. |
| | • Simple $I^2C$ mode | | |
| | SSCL12 | I/O | Input/output pin for the $I^2C$ clock. |
| | SSDA12 | I/O | Input/output pin for the $I^2C$ data. |
| | • Simple SPI mode | | |
| | SCK12 | I/O | Input/output pin for the clock. |
| | SMISO12 | I/O | Input/output pin for slave transmit data. |
| | SMOSI12 | I/O | Input/output pin for master transmit data. |
| | SS12# | Input | Chip-select input pin. |
| | • Extended serial mode | | |
| | RXDX12 | Input | Input pin for data reception by SCIf. |
| | TXDX12 | Output | Output pin for data transmission by SCIf. |
| | SIOX12 | I/O | Input/output pin for data reception or transmission by SCIf. |
| $I^2C$ bus interface | SCL0 | I/O | Input/output pin for $I^2C$ bus interface clocks. Bus can be directly driven by the N-channel open drain output. |
| | SDA0 | I/O | Input/output pin for $I^2C$ bus interface data. Bus can be directly driven by the N-channel open drain output. |
| Serial peripheral interface | RSPCKA | I/O | Input/output pin for the RSPI clock. |
| | MOSIA | I/O | Input/output pin for transmitting data from the RSPI master. |
| | MISOA | I/O | Input/output pin for transmitting data from the RSPI slave. |
| | SSLA0 | I/O | Input/output pin to select the slave for the RSPI. |
| | SSLA1 to SSLA3 | Output | Output pins to select the slave for the RSPI. |

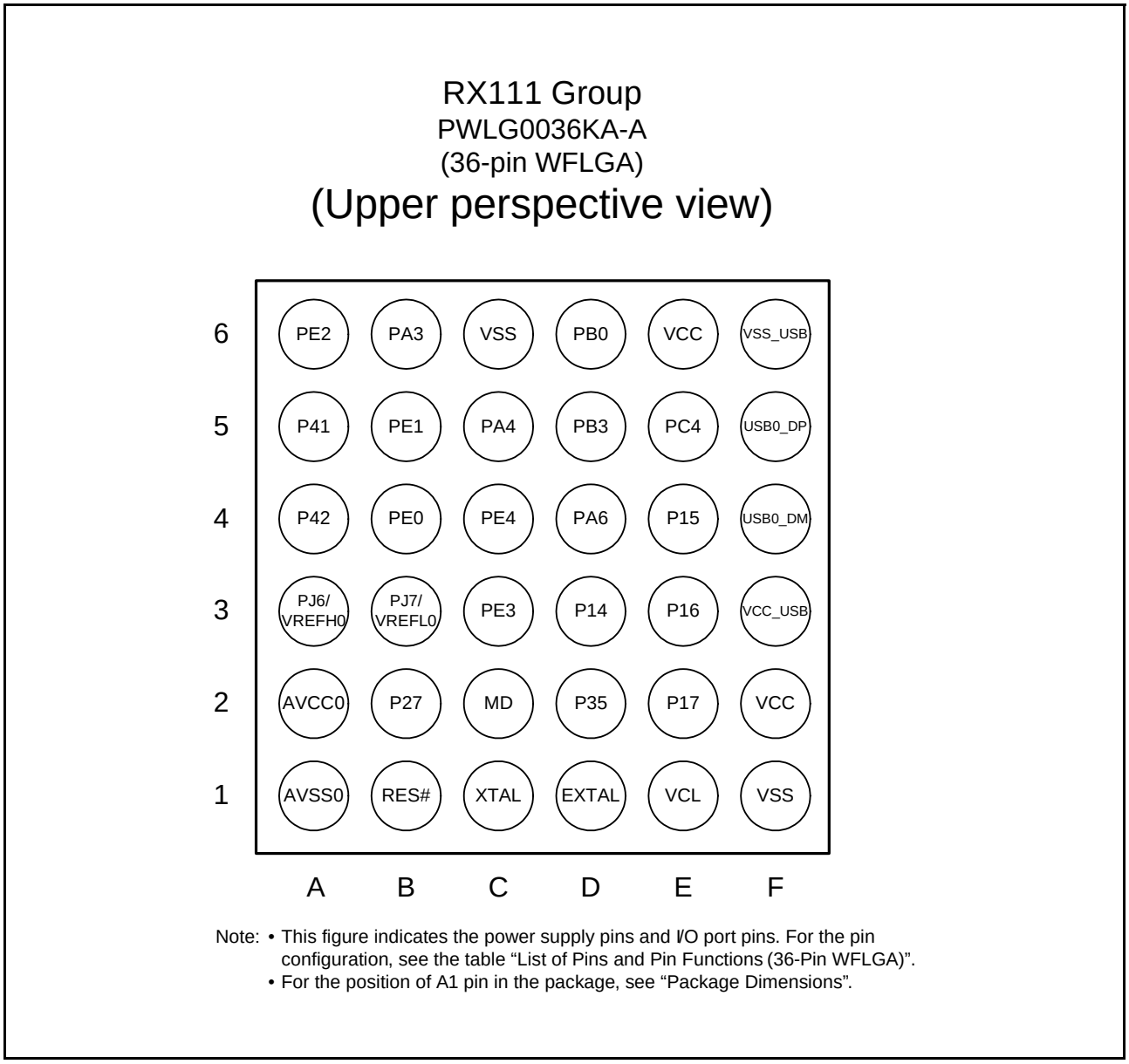
## 1.5 Pin Assignments

Figure 1.3 to Figure 1.7 show the pin assignments. Table 1.5 to Table 1.9 show the lists of pins and pin functions.




Note: • This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LFQFP/LQFP)”.

**Figure 1.3 Pin Assignments of the 64-Pin LFQFP/LQFP**




Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (36-Pin WFLGA)”.
• For the position of A1 pin in the package, see “Package Dimensions”.

**Figure 1.7 Pin Assignments of the 36-Pin WFLGA**

**Table 1.6 List of Pins and Pin Functions (64-Pin WFLGA) (1/2)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, POE, RTC) | Communication (SCIe, SCIf, RSPI, RIIC, USB) | Others |
|---|---|---|---|---|---|
| A1 | AVSS0 | | | | |
| A2 | AVCC0 | | | | |
| A3 | VREFH0 | PJ6*2 | | | |
| A4 | VREFL0 | PJ7*2 | | | |
| A5 | | P43*2 | | | AN003 |
| A6 | | P46*2 | | | AN006 |
| A7 | | PE2 | MTIOC4A | RXD12/RXDX12/SMISO12/SSCL12 | IRQ7/AN010 |
| A8 | | PE3 | MTIOC0A/MTIOC1B/ MTIOC4B/POE8# | CTS12#/RTS12#/SS12#/RSPCKA | IRQ3/AN011 |
| B1 | XCOUT | | | | |
| B2 | | P03 | | | DA0 |
| B3 | | P40*2 | | | AN000 |
| B4 | | P42*2 | | | AN002 |
| B5 | | P44*2 | | | AN004 |
| B6 | | PE6 | | | IRQ6/AN014 |
| B7 | | PE1 | MTIOC4C | TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12 | IRQ1/AN009 |
| B8 | | PE4 | MTIOC1A/MTIOC3A/ MTIOC4D | MOSIA | IRQ4/AN012 |
| C1 | XCIN | PH7 | | | |
| C2 | | P05 | | | DA1 |
| C3 | | P27 | MTIOC2B | SCK1/SCK12 | IRQ3/CMPA2/CACREF/ ADTRG0# |
| C4 | | P41*2 | | | AN001 |
| C5 | | PE7 | | | IRQ7/AN015 |
| C6 | | PE5 | MTIOC2B/MTIOC4C | | IRQ5/AN013 |
| C7 | | PA1 | MTIOC0B/MTCLKC/ RTCOUT | SCK5/SSLA2 | |
| C8 | | PA0 | MTIOC4A | SSLA1 | CACREF |
| D1 | RES# | | | | |
| D2 | | P30 | MTIOC4B/POE8# | RXD1/SMISO1/SSCL1 | IRQ0 |
| D3 | | P26 | MTIOC2A | TXD1/SMOSI1/SSDA1/ USB0_VBUSEN | |
| D4 | | PE0 | MTIOC2A/POE3# | SCK12 | IRQ0/AN008 |
| D5 | | PA6 | MTIC5V/MTIOC2A/MTCLKB/ POE2# | CTS5#/RTS5#/SS5#/SDA0/MOSIA | IRQ3 |
| D6 | | PA4 | MTIC5U/MTIOC2B/MTCLKA | TXD5/SMOSI5/SSDA5/SSLA0 | IRQ5 |
| D7 | | PA3 | MTIOC0D/MTCLKD/ MTIOC1B/POE0# | RXD5/SMISO5/SSCL5/MISOA | IRQ6 |
| D8 | VSS | | | | |
| E1 | XTAL | | | | |
| E2 | MD | | | | FINED |
| E3 | | P31 | MTIOC4D | CTS1#/RTS1#/SS1# | IRQ1 |
| E4 | | P55 | MTIOC4D | | |
| E5 | | PB3 | MTIOC0A/MTIOC3B/ MTIOC4A/POE3# | USB0_OVRCURA | |
| E6 | | PB1 | MTIOC0C/MTIOC4C | | IRQ4 |
| E7 | | PB0 | MTIC5W/MTIOC0C/ RTCOUT | SCL0/RSPCKA | IRQ2/ADTRG0# |
| E8 | VCC | | | | |
| F1 | EXTAL | | | | |

**Table 1.8 List of Pins and Pin Functions (40-Pin HWQFN) (1/2)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, POE, RTC) | Communication (SCIe, SCIf, RSPI, RIIC, USB) | Others |
|---|---|---|---|---|---|
| 1 | | P27 | MTIOC2B | SCK1/SCK12 | IRQ3/CMPA2/CACREF/ ADTRG0# |
| 2 | | P26 | MTIOC2A | TXD1/SMOSI1/SSDA1/ USB0_VBUSEN | |
| 3 | MD | | | | FINED |
| 4 | RES# | | | | |
| 5 | UPSEL | P35 | | | NMI |
| 6 | XTAL | | | | |
| 7 | EXTAL | | | | |
| 8 | VCL | | | | |
| 9 | VSS | | | | |
| 10 | VCC | | | | |
| 11 | | P32 | MTIOC0C | | IRQ2 |
| 12 | | P17 | MTIOC0C/MTIOC3A/ MTIOC3B/POE8# | SCK1/MISOA/SDA0/RXD12/ RXDX12/SMISO12/SSCL12 | IRQ7 |
| 13 | | P16 | MTIOC3C/MTIOC3D | TXD1/SMOSI1/SSDA1/SCL0/ MOSIA/USB0_VBUSEN/ USB0_OVRCURB/USB0_VBUS | IRQ6/ADTRG0# |
| 14 | | P15 | MTIOC0B/MTCLKB | RXD1/SMISO1/SSCL1/RSPCKA | IRQ5/CLKOUT |
| 15 | UB# | P14 | MTIOC0A/MTIOC3A/ MTCLKA | CTS1#/RTS1#/SS1#/SSLA0/TXD12/ TXDX12/SIOX12/SMOSI12/ SSDA12/USB0_OVRCURA | IRQ4 |
| 16 | VCC_USB | | | | |
| 17 | | | | USB0_DM | |
| 18 | | | | USB0_DP | |
| 19 | VSS_USB | | | | |
| 20 | | PC4 | MTIOC3D/MTCLKC/POE0# | SCK5/SSLA0/USB0_VBUS*1/ USB0_VBUSEN | IRQ2/CLKOUT |
| 21 | | PB3 | MTIOC0A/MTIOC3B/ MTIOC4A/POE3# | USB0_OVRCURA | |
| 22 | VCC | | | | |
| 23 | | PB0 | MTIOC0C/MTIC5W | SCL0/RSPCKA | IRQ2/ADTRG0# |
| 24 | VSS | | | | |
| 25 | | PA6 | MTIOC2A/MTIC5V/MTCLKB/ POE2# | CTS5#/RTS5#/SS5#/SDA0/MOSIA | IRQ3 |
| 26 | | PA4 | MTIOC2B/MTIC5U/MTCLKA | TXD5/SMOSI5/SSDA5/SSLA0 | IRQ5 |
| 27 | | PA3 | MTIOC0D/MTIOC1B/ MTCLKD/POE0# | RXD5/SMISO5/SSCL5/MISOA | IRQ6 |
| 28 | | PA1 | MTIOC0B/MTCLKC | SCK5/SSLA2 | |
| 29 | | PE4 | MTIOC1A/MTIOC3A/ MTIOC4D | MOSIA | IRQ4/AN012 |
| 30 | | PE3 | MTIOC0A/MTIOC1B/ MTIOC4B/POE8# | CTS12#/RTS12#/SS12#/RSPCKA | IRQ3/AN011 |
| 31 | | PE2 | MTIOC4A | RXD12/RXDX12/SMISO12/SSCL12 | IRQ7/AN010 |
| 32 | | PE1 | MTIOC4C | TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12 | IRQ1/AN009 |
| 33 | | PE0 | MTIOC2A/POE3# | SCK12 | IRQ0/AN008 |
| 34 | | P46*2 | | | AN006 |
| 35 | | P42*2 | | | AN002 |
| 36 | | P41*2 | | | AN001 |
| 37 | VREFL0 | PJ7*2 | | | |
| 38 | VREFH0 | PJ6*2 | | | |
| 39 | AVSS0 | | | | |

**Table 1.8 List of Pins and Pin Functions (40-Pin HWQFN) (2/2)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, POE, RTC) | Communication (SCIe, SCIf, RSPI, RIIC, USB) | Others |
|---|---|---|---|---|---|
| 40 | AVCC0 | | | | |

Note 1. Not 5 V tolerant.
Note 2. The power source of the I/O buffer for these pins is AVCC0.

**Table 4.1 List of I/O Registers (Address Order) (3/16)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|---|---|---|---|---|---|---|
| 0008 70ABh | ICU | Interrupt Request Register 171 | IR171 | 8 | 8 | 2 ICLK |
| 0008 70DAh | ICU | Interrupt Request Register 218 | IR218 | 8 | 8 | 2 ICLK |
| 0008 70DBh | ICU | Interrupt Request Register 219 | IR219 | 8 | 8 | 2 ICLK |
| 0008 70DCh | ICU | Interrupt Request Register 220 | IR220 | 8 | 8 | 2 ICLK |
| 0008 70DDh | ICU | Interrupt Request Register 221 | IR221 | 8 | 8 | 2 ICLK |
| 0008 70DEh | ICU | Interrupt Request Register 222 | IR222 | 8 | 8 | 2 ICLK |
| 0008 70DFh | ICU | Interrupt Request Register 223 | IR223 | 8 | 8 | 2 ICLK |
| 0008 70E0h | ICU | Interrupt Request Register 224 | IR224 | 8 | 8 | 2 ICLK |
| 0008 70E1h | ICU | Interrupt Request Register 225 | IR225 | 8 | 8 | 2 ICLK |
| 0008 70EEh | ICU | Interrupt Request Register 238 | IR238 | 8 | 8 | 2 ICLK |
| 0008 70EFh | ICU | Interrupt Request Register 239 | IR239 | 8 | 8 | 2 ICLK |
| 0008 70F0h | ICU | Interrupt Request Register 240 | IR240 | 8 | 8 | 2 ICLK |
| 0008 70F1h | ICU | Interrupt Request Register 241 | IR241 | 8 | 8 | 2 ICLK |
| 0008 70F2h | ICU | Interrupt Request Register 242 | IR242 | 8 | 8 | 2 ICLK |
| 0008 70F3h | ICU | Interrupt Request Register 243 | IR243 | 8 | 8 | 2 ICLK |
| 0008 70F4h | ICU | Interrupt Request Register 244 | IR244 | 8 | 8 | 2 ICLK |
| 0008 70F5h | ICU | Interrupt Request Register 245 | IR245 | 8 | 8 | 2 ICLK |
| 0008 70F6h | ICU | Interrupt Request Register 246 | IR246 | 8 | 8 | 2 ICLK |
| 0008 70F7h | ICU | Interrupt Request Register 247 | IR247 | 8 | 8 | 2 ICLK |
| 0008 70F8h | ICU | Interrupt Request Register 248 | IR248 | 8 | 8 | 2 ICLK |
| 0008 70F9h | ICU | Interrupt Request Register 249 | IR249 | 8 | 8 | 2 ICLK |
| 0008 711Bh | ICU | DTC Activation Enable Register 027 | DTCER027 | 8 | 8 | 2 ICLK |
| 0008 711Ch | ICU | DTC Activation Enable Register 028 | DTCER028 | 8 | 8 | 2 ICLK |
| 0008 711Dh | ICU | DTC Activation Enable Register 029 | DTCER029 | 8 | 8 | 2 ICLK |
| 0008 7124h | ICU | DTC Activation Enable Register 036 | DTCER036 | 8 | 8 | 2 ICLK |
| 0008 7125h | ICU | DTC Activation Enable Register 037 | DTCER037 | 8 | 8 | 2 ICLK |
| 0008 712Dh | ICU | DTC Activation Enable Register 045 | DTCER045 | 8 | 8 | 2 ICLK |
| 0008 712Eh | ICU | DTC Activation Enable Register 046 | DTCER046 | 8 | 8 | 2 ICLK |
| 0008 7140h | ICU | DTC Activation Enable Register 064 | DTCER064 | 8 | 8 | 2 ICLK |
| 0008 7141h | ICU | DTC Activation Enable Register 065 | DTCER065 | 8 | 8 | 2 ICLK |
| 0008 7142h | ICU | DTC Activation Enable Register 066 | DTCER066 | 8 | 8 | 2 ICLK |
| 0008 7143h | ICU | DTC Activation Enable Register 067 | DTCER067 | 8 | 8 | 2 ICLK |
| 0008 7144h | ICU | DTC Activation Enable Register 068 | DTCER068 | 8 | 8 | 2 ICLK |
| 0008 7145h | ICU | DTC Activation Enable Register 069 | DTCER069 | 8 | 8 | 2 ICLK |
| 0008 7146h | ICU | DTC Activation Enable Register 070 | DTCER070 | 8 | 8 | 2 ICLK |
| 0008 7147h | ICU | DTC Activation Enable Register 071 | DTCER071 | 8 | 8 | 2 ICLK |
| 0008 7166h | ICU | DTC Activation Enable Register 102 | DTCER102 | 8 | 8 | 2 ICLK |
| 0008 7167h | ICU | DTC Activation Enable Register 103 | DTCER103 | 8 | 8 | 2 ICLK |
| 0008 716Ah | ICU | DTC Activation Enable Register 106 | DTCER106 | 8 | 8 | 2 ICLK |
| 0008 7172h | ICU | DTC Activation Enable Register 114 | DTCER114 | 8 | 8 | 2 ICLK |
| 0008 7173h | ICU | DTC Activation Enable Register 115 | DTCER115 | 8 | 8 | 2 ICLK |
| 0008 7174h | ICU | DTC Activation Enable Register 116 | DTCER116 | 8 | 8 | 2 ICLK |
| 0008 7175h | ICU | DTC Activation Enable Register 117 | DTCER117 | 8 | 8 | 2 ICLK |
| 0008 7179h | ICU | DTC Activation Enable Register 121 | DTCER121 | 8 | 8 | 2 ICLK |
| 0008 717Ah | ICU | DTC Activation Enable Register 122 | DTCER122 | 8 | 8 | 2 ICLK |
| 0008 717Dh | ICU | DTC Activation Enable Register 125 | DTCER125 | 8 | 8 | 2 ICLK |
| 0008 717Eh | ICU | DTC Activation Enable Register 126 | DTCER126 | 8 | 8 | 2 ICLK |
| 0008 7181h | ICU | DTC Activation Enable Register 129 | DTCER129 | 8 | 8 | 2 ICLK |
| 0008 7182h | ICU | DTC Activation Enable Register 130 | DTCER130 | 8 | 8 | 2 ICLK |
| 0008 7183h | ICU | DTC Activation Enable Register 131 | DTCER131 | 8 | 8 | 2 ICLK |
| 0008 7184h | ICU | DTC Activation Enable Register 132 | DTCER132 | 8 | 8 | 2 ICLK |
| 0008 7186h | ICU | DTC Activation Enable Register 134 | DTCER134 | 8 | 8 | 2 ICLK |

# 5. Electrical Characteristics

## 5.1 Absolute Maximum Ratings

**Table 5.1 Absolute Maximum Ratings**

Conditions: VSS = AVSS0 = VREFL0 = VSS_USB = 0 V

| Item | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power supply voltage | | VCC, VCC_USB | –0.3 to +4.6 | V |
| Input voltage | Ports for 5 V tolerant*1 | $V_{in}$ | –0.3 to +6.5 | V |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | $V_{in}$ | –0.3 to AVCC0 +0.3 | V |
| | Ports other than above | $V_{in}$ | –0.3 to VCC +0.3 | V |
| Reference power supply voltage | | VREFH0 | –0.3 to AVCC0 +0.3 | V |
| Analog power supply voltage | | AVCC0 | –0.3 to +4.6 | V |
| Analog input voltage | | $V_{AN}$ | –0.3 to AVCC0 + 0.3<br>(when AN000 to AN004 and AN006 used)<br>–0.3 to VCC + 0.3<br>(when AN008 to AN015 used) | V |
| Operating temperature*2 | | $T_{opr}$ | –40 to +85<br>–40 to +105 | °C |
| Storage temperature | | $T_{stg}$ | –55 to +125 | °C |

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, and between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin, refer to section 5.12.1, Connecting VCL Capacitor and Bypass Capacitors.

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered. The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
If input voltage (within the specified range from -0.3 to + 6.5V) is applied to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports P16, P17, PA6, and PB0 are 5 V tolerant.
Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to 1.2 List of Products.

**Table 5.2 Operating Conditions**

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltages | VCC*1 | When USB not used | 1.8 | — | 3.6 | V |
| | | When USB used | 3.0 | — | 3.6 | V |
| | VSS | | — | 0 | — | V |
| USB power supply voltages | VCC_USB | | — | VCC | — | V |
| | VSS_USB | | — | 0 | — | V |
| Analog power supply voltages | AVCC0*1, *2 | | 1.8 | — | 3.6 | V |
| | AVSS0 | | — | 0 | — | V |
| | VREFH0 | | 1.8 | — | AVCC0 | V |
| | VREFL0 | | — | 0 | — | V |

Note 1. When powering on AVCC0 and VCC, power them on at the same time or VCC first.
Note 2. For details, refer to section 30.7.10, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.

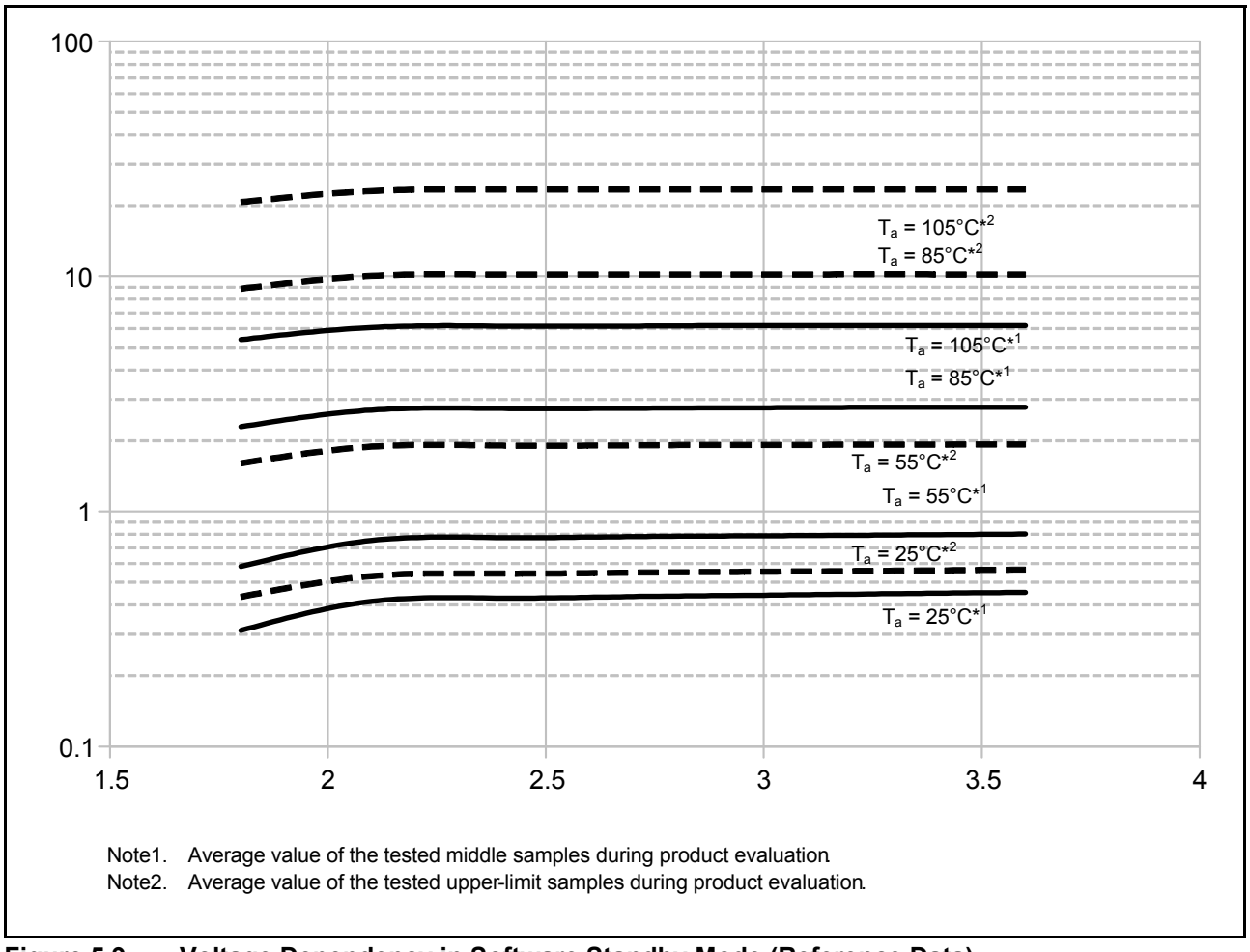
[256-Kbyte or more flash memory]

**Table 5.10 DC Characteristics (8)**

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, $T_a$ = –40 to +105°C

| Item | | | Symbol | Typ.*3 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Supply current*1 | Software standby mode*2 | $T_a$ = 25°C | $I_{CC}$ | 0.44 | 0.98 | µA | |
| | | $T_a$ = 55°C | | 0.80 | 3.47 | | |
| | | $T_a$ = 85°C | | 2.7 | 12.0 | | |
| | | $T_a$ = 105°C | | 6.17 | 42.7 | | |
| | Increment for RTC operation*4 | | | 0.31 | — | | RCR3.RTCDV[2:0] = 010b |
| | | | | 1.09 | — | | RCR3.RTCDV[2:0] = 100b |
| | Increment for IWDT operation | | | 0.37 | — | | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.




Note1. Average value of the tested middle samples during product evaluation.
Note2. Average value of the tested upper-limit samples during product evaluation.

**Figure 5.9 Voltage Dependency in Software Standby Mode (Reference Data)**

**Table 5.18 Permissible Output Currents (2)**

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
$T_a$ = –40 to +105°C (G version)

| Item | | Symbol | Max. | Unit |
|---|---|---|---|---|
| Permissible output low current (average value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | $I_{OL}$ | 0.4 | mA |
| | Ports other than above | | 8.0 | |
| Permissible output low current (maximum value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | | 0.4 | |
| | Ports other than above | | 8.0 | |
| Permissible output low current | Total of ports P40 to P44, P46, ports PJ6, PJ7 | $\Sigma I_{OL}$ | 1.6 | |
| | Total of ports P03, P05, ports P26, P27, ports P30, P31 | | 20 | |
| | Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7 | | 20 | |
| | Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7 | | 20 | |
| | Total of all output pins | | 40 | |
| Permissible output high current (average value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | $I_{OH}$ | –0.1 | |
| | Ports other than above | | –4.0 | |
| Permissible output high current (maximum value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | | –0.1 | |
| | Ports other than above | | –4.0 | |
| Permissible output high current | Total of ports P40 to P44, P46, ports PJ6, PJ7 | $\Sigma I_{OH}$ | –0.6 | |
| | Total of ports P03, P05, ports P26, P27, ports P30, P31 | | –10 | |
| | Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7 | | –15 | |
| | Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7 | | –15 | |
| | Total of all output pins | | –40 | |

Note: Do not exceed the permissible total supply current.

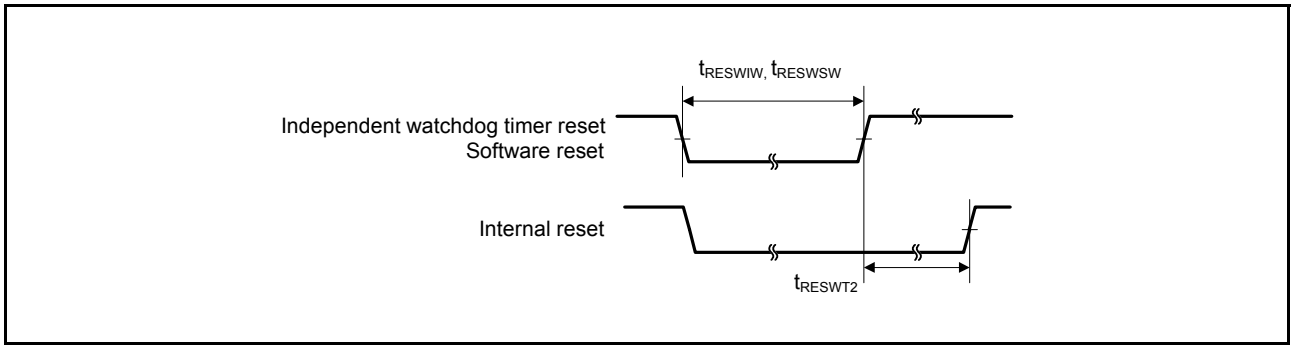



**Figure 5.33 Reset Input Timing (2)**

**Table 5.29 Timing of Recovery from Low Power Consumption Modes (4)**

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, $T_a$ = –40 to +105°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Recovery time from deep sleep mode*1 | High-speed mode*2 | $t_{DSLP}$ | — | 2 | 3.5 | µs | |
| | Middle-speed mode*3 | $t_{DSLP}$ | — | 3 | 4 | µs | |
| | Low-speed mode*4 | $t_{DSLP}$ | — | 400 | 500 | µs | |

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.
Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz.
Note 3. When the frequency of the system clock is 12 MHz.
Note 4. When the frequency of the system clock is 32.768 kHz.

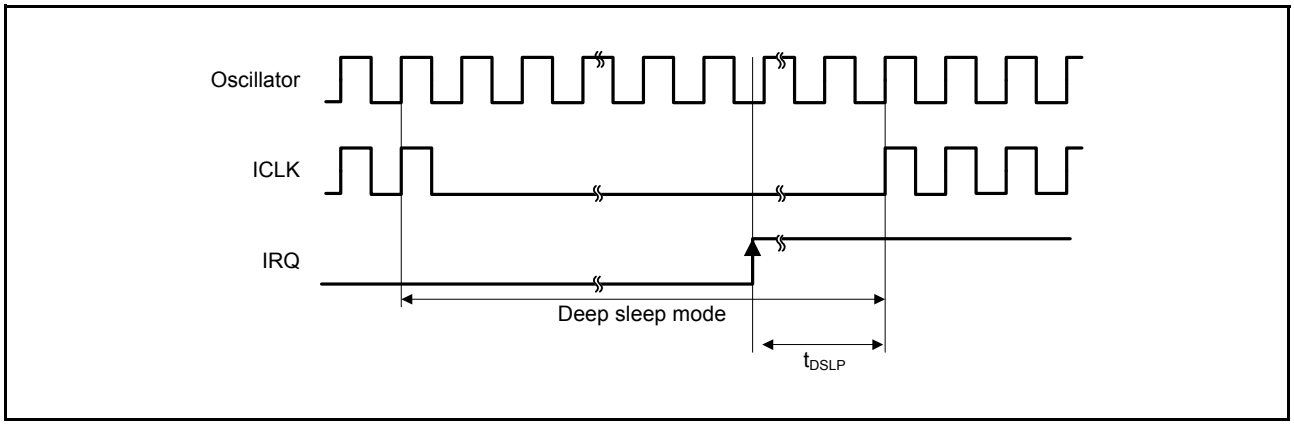



**Figure 5.35 Deep Sleep Mode Cancellation Timing**

**Table 5.30 Timing of Recovery from Low Power Consumption Modes (5) Operating Mode Transition Time**

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, $T_a$ = -40 to +105°C

| Mode before Transition | Mode after Transition | ICLK Frequency | Transition Time | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| High-speed operating mode | Middle-speed operating mode | 8 MHz | — | 10 | — | µs |
| Middle-speed operating mode | High-speed operating mode | 8 MHz | — | 37.5 | — | µs |
| Low-speed operating mode | Middle-speed operating mode, high-speed operating mode | 32.768 kHz | — | 213.62 | — | µs |
| Middle-speed operating mode, high-speed operating mode | Low-speed operating mode | 32.768 kHz | — | 183.11 | — | µs |

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

## 5.3.4 Control Signal Timing

**Table 5.31 Control Signal Timing**

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, $T_a$ = –40 to +105°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | — | — | ns | NMI digital filter disabled (NMIFLTE.NFLTEN = 0) | $t_{Pcyc}$ × 2 ≤ 200 ns |
| | | $t_{Pcyc}$ × 2*1 | — | — | | | $t_{Pcyc}$ × 2 > 200 ns |
| | | 200 | — | — | | NMI digital filter enabled (NMIFLTE.NFLTEN = 1) | $t_{NMICK}$ × 3 ≤ 200 ns |
| | | $t_{NMICK}$ × 3.5*2 | — | — | | | $t_{NMICK}$ × 3 > 200 ns |
| IRQ pulse width | $t_{IRQW}$ | 200 | — | — | ns | IRQ digital filter disabled (IRQFLTE0.FLTENi = 0) | $t_{Pcyc}$ × 2 ≤ 200 ns |
| | | $t_{Pcyc}$ × 2*1 | — | — | | | $t_{Pcyc}$ × 2 > 200 ns |
| | | 200 | — | — | | IRQ digital filter enabled (IRQFLTE0.FLTENi = 1) | $t_{IRQCK}$ × 3 ≤ 200 ns |
| | | $t_{IRQCK}$ × 3.5*3 | — | — | | | $t_{IRQCK}$ × 3 > 200 ns |

Note: • 200 ns minimum in software standby mode.
Note 1. $t_{Pcyc}$ indicates the cycle of PCLKB.
Note 2. $t_{NMICK}$ indicates the cycle of the NMI digital filter sampling clock.
Note 3. $t_{IRQCK}$ indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

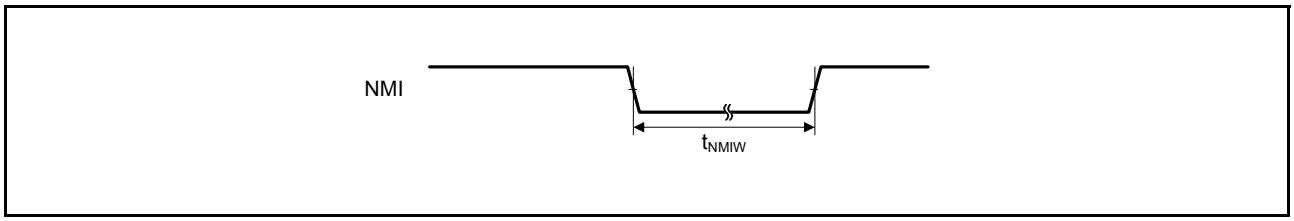



**Figure 5.36 NMI Interrupt Input Timing**

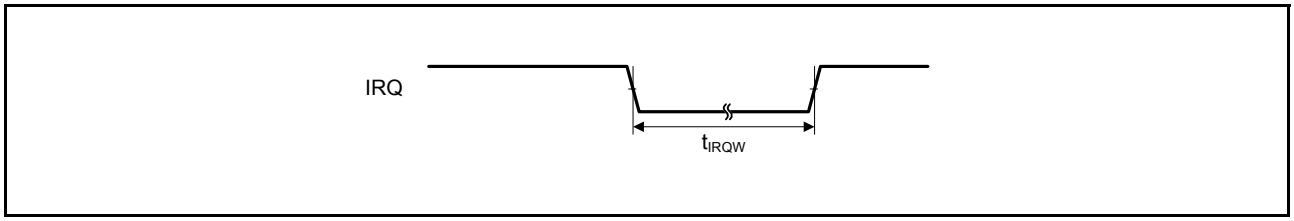



**Figure 5.37 IRQ Interrupt Input Timing**

## 5.3.5 Timing of On-Chip Peripheral Modules

**Table 5.32 Timing of On-Chip Peripheral Modules (1)**

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, $T_a$ = –40 to +105°C

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| I/O ports | Input data pulse width | | $t_{PRW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.38 |
| MTU2 | Input capture input pulse width | Single-edge setting | $t_{TICW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.39 |
| | | Both-edge setting | | 2.5 | — | | |
| | Timer clock pulse width | Single-edge setting | $t_{TCKWH}$, $t_{TCKWL}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.40 |
| | | Both-edge setting | | 2.5 | — | | |
| | | Phase counting mode | | 2.5 | — | | |
| POE | POE# input pulse width | | $t_{POEW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.41 |
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{Pcyc}$ | Figure 5.42 |
| | | Clock synchronous | | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 20 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 20 | ns | |
| | Output clock cycle | Asynchronous | $t_{Scyc}$ | 16 | — | $t_{Pcyc}$ | Figure 5.43 C = 30 pF |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 20 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 20 | ns | |
| | Transmit data delay time (master) | Clock synchronous | $t_{TXD}$ | — | 40 | ns | |
| | Transmit data delay time (slave) | Clock synchronous, 2.7 V or above | | — | 65 | ns | |
| | | Clock synchronous, 1.8 V or above | | — | 100 | ns | |
| | Receive data setup time (master) | Clock synchronous, 2.7 V or above | $t_{RXS}$ | 65 | — | ns | |
| | | Clock synchronous, 1.8 V or above | | 90 | — | ns | |
| | Receive data setup time (slave) | Clock synchronous | | 40 | — | ns | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 40 | — | ns | |
| A/D converter | Trigger input pulse width | | $t_{TRGW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.44 |
| CAC | CACREF input pulse width | $t_{Pcyc} \le t_{cac}$*2 | $t_{CACREF}$ | 4.5 $t_{cac}$ + 3 $t_{Pcyc}$ | — | ns | |
| | | $t_{Pcyc} > t_{cac}$*2 | | 5 $t_{cac}$ + 6.5 $t_{Pcyc}$ | | | |
| CLKOUT | CLKOUT pin output cycle*4 | VCC = 2.7 V or above | $t_{Ccyc}$ | 125 | — | ns | |
| | | VCC = 1.8 V or above | | 250 | | | |
| | CLKOUT pin high pulse width*3 | VCC = 2.7 V or above | $t_{CH}$ | 35 | — | ns | |
| | | VCC = 1.8 V or above | | 70 | | | |
| | CLKOUT pin low pulse width*3 | VCC = 2.7 V or above | $t_{CL}$ | 35 | — | ns | |
| | | VCC = 1.8 V or above | | 70 | | | |
| | CLKOUT pin output rise time | VCC = 2.7 V or above | $t_{Cr}$ | — | 15 | ns | |
| | | VCC = 1.8 V or above | | | 30 | | |
| | CLKOUT pin output fall time | VCC = 2.7 V or above | $t_{Cf}$ | — | 15 | ns | |
| | | VCC = 1.8 V or above | | | 30 | | |

Note 1. $t_{Pcyc}$: PCLK cycle
Note 2. $t_{cac}$: CAC count clock source cycle
Note 3. When the LOCO is selected as the clock output source (CKOCR.CKOSEL[2:0] bits = 000b), set the clock output division ratio selection to divided by 2 (CKOCR.CKODIV[2:0] bits = 001b).
Note 4. When the XTAL external clock input or an oscillator is used with divided by 1 (CKOCR.CKOSEL[2:0] bits = 010b and CKOCR.CKODIV[2:0] bits = 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

**Table 5.34 Timing of On-Chip Peripheral Modules (3)**

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
$T_a$ = –40 to +105°C, C = 30 pF

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| Simple SPI | SCK clock cycle output (master) | | $t_{SPcyc}$ | 4 | 65536 | $t_{Pcyc}$ | Figure 5.46 |
| | SCK clock cycle input (slave) | | | 6 | 65536 | | |
| | SCK clock high pulse width | | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise/fall time | | $t_{SPCKr}$, $t_{SPCKf}$ | — | 20 | ns | |
| | Data input setup time (master) | 2.7 V or above | $t_{SU}$ | 65 | — | ns | Figure 5.47, Figure 5.49 |
| | | 1.8 V or above | | 95 | — | | |
| | Data input setup time (slave) | | | 40 | — | | |
| | Data input hold time | | $t_H$ | 40 | — | ns | |
| | SS input setup time | | $t_{LEAD}$ | 3 | — | $t_{Pcyc}$ | |
| | SS input hold time | | $t_{LAG}$ | 3 | — | $t_{Pcyc}$ | |
| | Data output delay time (master) | | $t_{OD}$ | — | 40 | ns | |
| | Data output delay time (slave) | 2.7 V or above | | — | 65 | | |
| | | 1.8 V or above | | — | 85 | | |
| | Data output hold time (master) | 2.7 V or above | $t_{OH}$ | –10 | — | ns | |
| | | 1.8 V or above | | –20 | — | | |
| | Data output hold time (slave) | | | –10 | — | | |
| | Data rise/fall time | | $t_{Dr}$, $t_{Df}$ | — | 20 | ns | |
| | SS input rise/fall time | | $t_{SSLr}$, $t_{SSLf}$ | — | 20 | ns | |
| | Slave access time | | $t_{SA}$ | — | 6 | $t_{Pcyc}$ | Figure 5.51, Figure 5.52 |
| | Slave output release time | | $t_{REL}$ | — | 6 | $t_{Pcyc}$ | |

Note 1. $t_{Pcyc}$: PCLK cycle

## 5.11 E2 DataFlash Characteristics

**Table 5.51 E2 DataFlash Characteristics (1)**

| Item | | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| Reprogramming/erasure cycle*1 | | $N_{DPEC}$ | 100000 | 1000000 | — | Times | |
| Data hold time | After 10000 times of $N_{DPEC}$ | $t_{DDRP}$ | 20*2, *3 | — | — | Year | Ta = +85°C |
| | After 100000 times of $N_{DPEC}$ | | 5*2, *3 | — | — | Year | |
| | After 1000000 times of $N_{DPEC}$ | | — | 1*2, *3 | — | Year | Ta = +25°C |

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in 1-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristics when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. These results are obtained from reliability testing.

**Table 5.52 E2 DataFlash Characteristics (2) : high-speed operating mode**

Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: $T_a$ = –40 to +105°C

| Item | | Symbol | FCLK = 1 MHz | | | FCLK = 32 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time | 1-byte | $t_{DP1}$ | — | 86 | 761 | — | 40.5 | 374 | µs |
| Erasure time | 1-Kbyte | $t_{DE1K}$ | — | 17.4 | 456 | — | 6.15 | 228 | ms |
| | 8-Kbyte | $t_{DE8K}$ | — | 60.4 | 499 | — | 9.3 | 231 | ms |
| Blank check time | 1-byte | $t_{DBC1}$ | — | — | 48 | — | — | 15.9 | µs |
| | 1-Kbyte | $t_{DBC1K}$ | — | — | 1.58 | — | — | 0.127 | µs |
| Erase operation forcible stop time | | $t_{DSED}$ | — | — | 21.5 | — | — | 12.8 | µs |
| DataFlash STOP recovery time | | $t_{DSTOP}$ | 5 | — | — | 5 | — | — | µs |

Note: • Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: • The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: • The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.

**Table 5.53 E2 DataFlash Characteristics (3) : middle-speed operating mode**

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: $T_a$ = –40 to +85°C

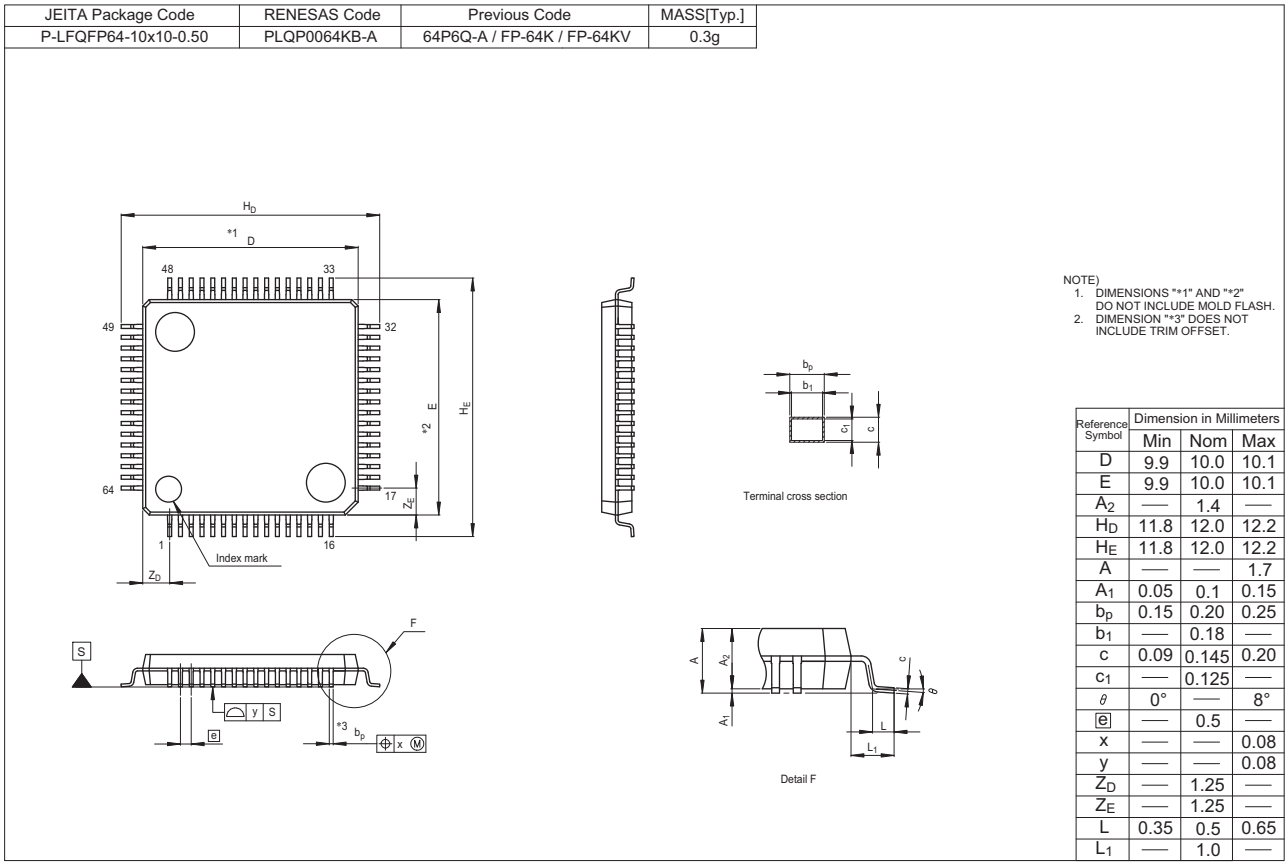
| Item | | Symbol | FCLK = 1 MHz | | | FCLK = 8 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time | 1-byte | $t_{DP1}$ | — | 126 | 1160 | — | 85.4 | 818 | µs |
| Erasure time | 1-Kbyte | $t_{DE1K}$ | — | 17.5 | 457 | — | 7.76 | 259 | ms |
| | 8-Kbyte | $t_{DE8K}$ | — | 60.5 | 500 | — | 16.7 | 267.6 | ms |
| Blank check time | 1-byte | $t_{DBC1}$ | — | — | 78 | — | — | 50 | µs |
| | 1-Kbyte | $t_{DBC1K}$ | — | — | 1.61 | — | — | 0.369 | ms |
| Erase operation forcible stop time | | $t_{DSED}$ | — | — | 33.5 | — | — | 25.5 | µs |
| DataFlash STOP recovery time | | $t_{DSTOP}$ | 720 | — | — | 720 | — | — | ns |

Note: • Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: • The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: • The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.

# Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

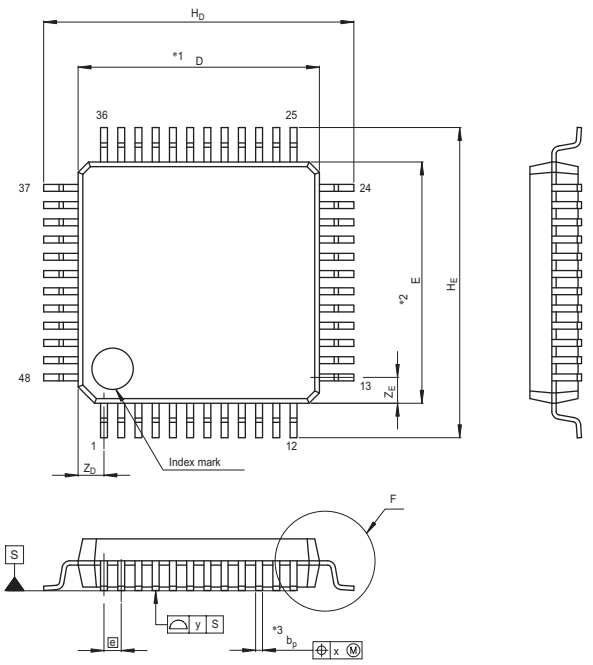
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP64-10x10-0.50 | PLQP0064KB-A | 64P6Q-A / FP-64K / FP-64KV | 0.3g |



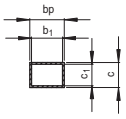

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| $\theta$ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure A 64-Pin LFQFP (PLQP0064KB-A)

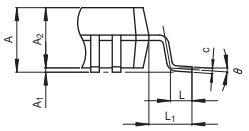
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP48-7x7-0.50 | PLQP0048KB-A | 48P6Q-A | 0.2g |






Terminal cross section




Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.9 | 7.0 | 7.1 |
| E | 6.9 | 7.0 | 7.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 8.8 | 9.0 | 9.2 |
| $H_E$ | 8.8 | 9.0 | 9.2 |
| A | — | — | 1.7 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.17 | 0.22 | 0.27 |
| $b_1$ | — | 0.20 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure D 48-Pin LFQFP (PLQP0048KB-A)

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

| Rev. | Date | Description | | Classification |
|---|---|---|---|---|
| | | Page | Summary | |
| 1.30 | May 31, 2016 | 1. Overview | | |
| | | 18 to 26 | Table 1.5 to 1.9 Note 2 regarding I/O power source is AVCC0 for the ports (P4, PJ6, and PJ7), added | |
| | | 5. Electrical Characteristics | | |
| | | 49 | Table 5.1 Absolute Maximum Ratings, Analog power supply voltage added | |
| | | 49 | Table 5.2 Recommended Operating Conditions, VREFH0 / VREFL0 added | |
| | | 58 | Figure 5.4 Voltage Dependency in High-Speed Operating Mode (Reference Data) added | |
| | | 59 | Figure 5.5 Voltage Dependency in Middle-Speed Operating Mode (Reference Data) added | |
| | | 59 | Figure 5.6 Voltage Dependency in Low-Speed Operating Mode (Reference Data) added | |
| | | 60 | Table 5.9 DC Characteristics (7), Increment for IWDT operation added | |
| | | 62 | Table 5.10 DC Characteristics (8), Increment for IWDT operation added | |
| | | 62 | Figure 5.9 Voltage Dependency in Software Standby Mode (Reference Data) added | |
| | | 63 | Figure 5.10 Temperature Dependency in Software Standby Mode (Reference Data) added | |
| | | 63 | Table 5.11 DC Characteristics (9) added | TN-RX*-A134A/E |
| | | 64 | Table 5.12 DC Characteristics (10), LDV1, 2 added | |
| | | 66, 67 | Table 5.18 Permissible Output Currents is divided into D version and G version | TN-RX*-A134A/E |
| | | 110 | Table 5.49 ROM (Flash Memory for Code Storage) Characteristics (2), Erasure time - 256-Kbyte added | TN-RX*-A132A/E |
| | | 111 | Table 5.50 ROM (Flash Memory for Code Storage) Characteristics (3), Temperature range for the programming/erasure operation changed and Erasure time - 256-Kbyte added | TN-RX*-A132A/E |
| | | 112 | Table 5.52 E2 DataFlash Characteristics (2), Low speed FCLK changed and Erasure time - 8-Kbyte added | TN-RX*-A132A/E |
| | | 112 | Table 5.53 E2 DataFlash Characteristics (3), Temperature range for the programming/erasure operation changed, Low speed FCLK changed and Erasure time - 8-Kbyte added | TN-RX*-A132A/E |
| | | 113, 114 | 5.12 Usage Notes added | |