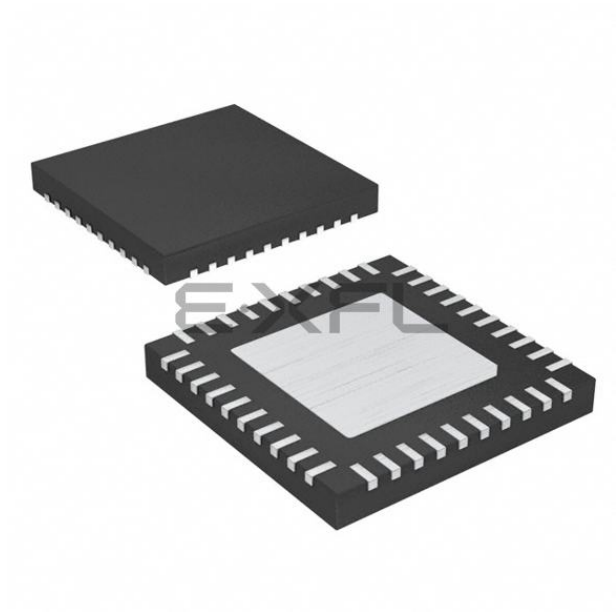
Renesas Electronics America Inc - R5F51113ADNF#UA Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51113adnf-ua

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

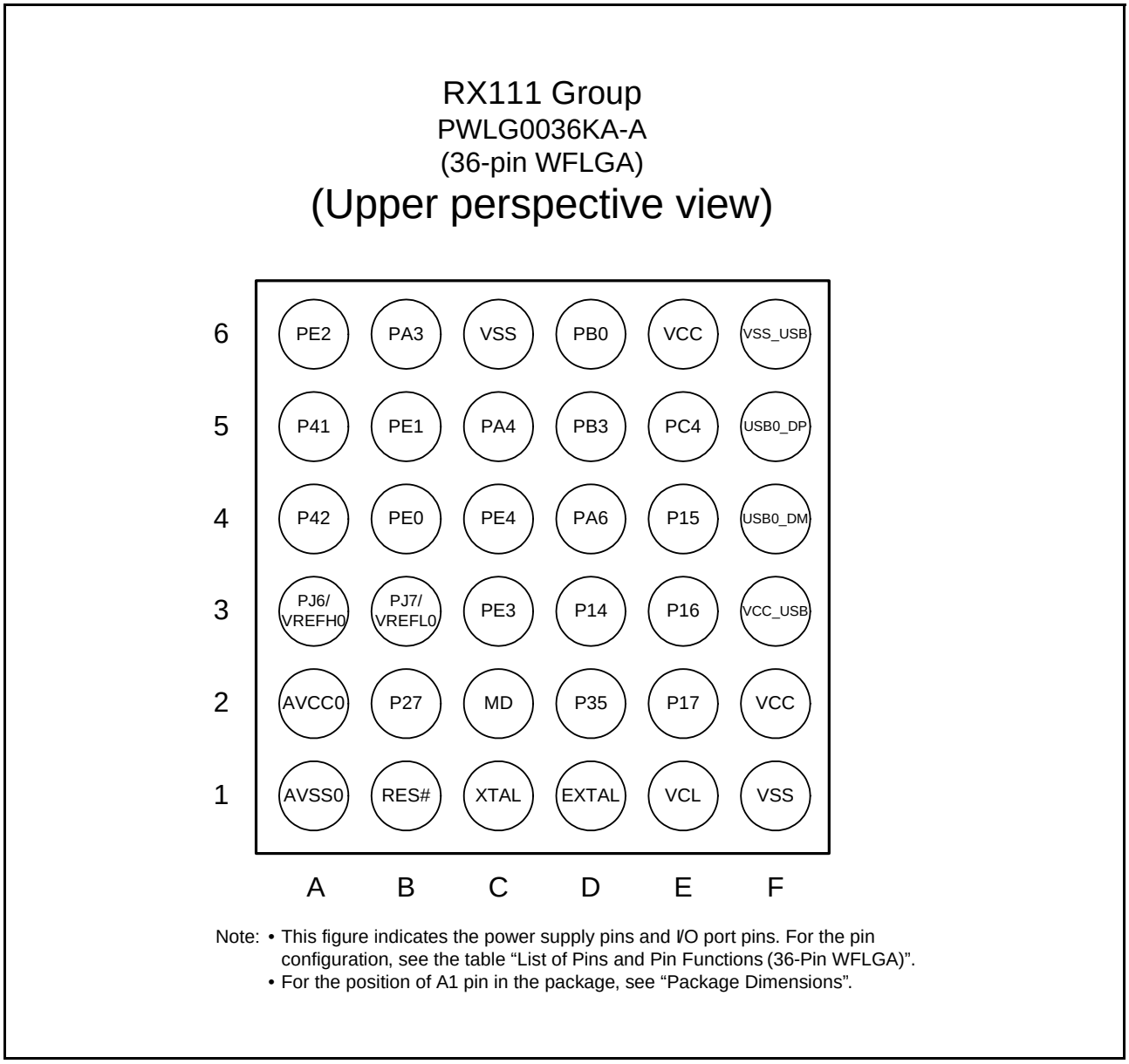
Table 1.3 List of Products (1/2)

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Maximum Operating Frequency	Operating Temperature
RX111	R5F51118AGFM	R5F51118AGFM#3A	PLQP0064KB-A	512 Kbytes	64 Kbytes	8 Kbytes	32 MHz	–40 to +105°C
	R5F51118AGFK	R5F51118AGFK#3A	PLQP0064GA-A					
	R5F51118AGFL	R5F51118AGFL#3A	PLQP0048KB-A					
	R5F51118AGNE	R5F51118AGNE#UA	PWQN0048KB-A					
	R5F51117AGFM	R5F51117AGFM#3A	PLQP0064KB-A	384 Kbytes				
	R5F51117AGFK	R5F51117AGFK#3A	PLQP0064GA-A					
	R5F51117AGFL	R5F51117AGFL#3A	PLQP0048KB-A					
	R5F51117AGNE	R5F51117AGNE#UA	PWQN0048KB-A					
	R5F51116AGFM	R5F51116AGFM#3A	PLQP0064KB-A	256 Kbytes	32 Kbytes			
	R5F51116AGFK	R5F51116AGFK#3A	PLQP0064GA-A					
	R5F51116AGFL	R5F51116AGFL#3A	PLQP0048KB-A					
	R5F51116AGNE	R5F51116AGNE#UA	PWQN0048KB-A					
	R5F51115AGFM	R5F51115AGFM#3A	PLQP0064KB-A	128 Kbytes	16 Kbytes			
	R5F51115AGFK	R5F51115AGFK#3A	PLQP0064GA-A					
	R5F51115AGFL	R5F51115AGFL#3A	PLQP0048KB-A					
	R5F51115AGNE	R5F51115AGNE#UA	PWQN0048KB-A					
	R5F51114AGFM	R5F51114AGFM#3A	PLQP0064KB-A	96 Kbytes				
	R5F51114AGFK	R5F51114AGFK#3A	PLQP0064GA-A					
	R5F51114AGFL	R5F51114AGFL#3A	PLQP0048KB-A					
	R5F51114AGNE	R5F51114AGNE#UA	PWQN0048KB-A					
	R5F51113AGFM	R5F51113AGFM#3A	PLQP0064KB-A	64 Kbytes	10 Kbytes			
	R5F51113AGFK	R5F51113AGFK#3A	PLQP0064GA-A					
	R5F51113AGFL	R5F51113AGFL#3A	PLQP0048KB-A					
	R5F51113AGNE	R5F51113AGNE#UA	PWQN0048KB-A					
	R5F51113AGNF	R5F51113AGNF#UA	PWQN0040KC-A					
	R5F51111AGFM	R5F51111AGFM#3A	PLQP0064KB-A	32 Kbytes				
	R5F51111AGFK	R5F51111AGFK#3A	PLQP0064GA-A					
	R5F51111AGFL	R5F51111AGFL#3A	PLQP0048KB-A					
	R5F51111AGNE	R5F51111AGNE#UA	PWQN0048KB-A					
	R5F51111AGNF	R5F51111AGNF#UA	PWQN0040KC-A					
	R5F5111JAGFM	R5F5111JAGFM#3A	PLQP0064KB-A	16 Kbytes	8 Kbytes			
	R5F5111JAGFK	R5F5111JAGFK#3A	PLQP0064GA-A					
	R5F5111JAGFL	R5F5111JAGFL#3A	PLQP0048KB-A					
	R5F5111JAGNE	R5F5111JAGNE#UA	PWQN0048KB-A					
	R5F5111JAGNF	R5F5111JAGNF#UA	PWQN0040KC-A					

Table 1.4 Pin Functions (3/3)

Classifications	Pin Name	I/O	Description
USB 2.0 host/ function module	USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver.
	USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver.
	USB0_VBUS	Input	USB cable connection monitor pin.
	USB0_EXICEN	Output	Low-power control signal for the OTG chip.
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for the OTG chip.
	USB0_OVRCURA, USB0_OVRCURB	Input	External overcurrent detection pins.
	USB0_ID	Input	Mini-AB connector ID input pin during operation in OTG mode.
12-bit A/D converter	AN000 to AN004, AN006, AN008 to AN015	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.
I/O ports	P03, P05	I/O	2-bit input/output pins.
	P14 to P17	I/O	4-bit input/output pins.
	P26, P27	I/O	2-bit input/output pins.
	P30 to P32, P35	I/O	4-bit input/output pins (P35 input pin).
	P40 to P44, P46	I/O	6-bit input/output pins.
	P54, P55	I/O	2-bit input/output pins.
	PA0, PA1, PA3, PA4, PA6	I/O	5-bit input/output pins.
	PB0, PB1, PB3, PB5 to PB7	I/O	6-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH7	Input	1-bit input pin.
	PJ6, PJ7	I/O	2-bit input/output pins.

Note 1. For external clock input.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (36-Pin WFLGA)”.
• For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.7 Pin Assignments of the 36-Pin WFLGA

Table 1.5 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC)	Communication (SCIe, SCIf, RSPI, RIIC, USB)	Others
42		PA4	MTIC5U/MTCLKA/MTIOC2B	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
43		PA3	MTIOC0D/MTCLKD/ MTIOC1B/POE0#	RXD5/SMISO5/SSCL5/MISOA	IRQ6
44		PA1	MTIOC0B/MTCLKC/ RTCOUT	SCK5/SSLA2	
45		PA0	MTIOC4A	SSLA1	CACREF
46		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
47		PE4	MTIOC4D/MTIOC1A/ MTIOC3A	MOSIA	IRQ4/AN012
48		PE3	MTIOC0A/MTIOC1B/ MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/RSPCKA	IRQ3/AN011
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12	IRQ7/AN010
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12	IRQ1/AN009
51		PE0	MTIOC2A/POE3#	SCK12	IRQ0/AN008
52		PE7			IRQ7/AN015
53		PE6			IRQ6/AN014
54		P46*2			AN006
55		P44*2			AN004
56		P43*2			AN003
57		P42*2			AN002
58		P41*2			AN001
59	VREFL0	PJ7*2			
60		P40*2			AN000
61	VREFH0	PJ6*2			
62	AVSS0				
63	AVCC0				
64		P05			DA1

Note 1. Not 5 V tolerant.
Note 2. The power source of the I/O buffer for these pins is AVCC0.

2.1 General-Purpose Registers (R0 to R15)

This CPU has 16 general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of 4, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

When executing an instruction after writing to multiple registers, only read the last I/O register written to and execute the instruction using that value; it is not necessary to execute the instruction using the values written to all the registers.

(3) Number of cycles necessary for accessing I/O registers

See Table 4.1 for details on the number of clock cycles necessary for accessing I/O registers.
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral buses 1 to 6

The number of bus cycles of internal peripheral buses 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral buses 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DTC).

(4) Notes on sleep mode and mode transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by ‘SYSTEM’ in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 003Eh	SYSTEM	CLKOUT Output Control Register	CKOCR	16	16	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00A5h	SYSTEM	High-Speed On-Chip Oscillator Wait Control Register	HOCOWTCR	8	8	3 ICLK
0008 00AAh	SYSTEM	Sub Operating Power Control Register	SOPCCR	8	8	3 ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK
0008 7020h	ICU	Interrupt Request Register 032	IR032	8	8	2 ICLK
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK
0008 7024h	ICU	Interrupt Request Register 036	IR036	8	8	2 ICLK
0008 7025h	ICU	Interrupt Request Register 037	IR037	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (3/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK
0008 70EEh	ICU	Interrupt Request Register 238	IR238	8	8	2 ICLK
0008 70EFh	ICU	Interrupt Request Register 239	IR239	8	8	2 ICLK
0008 70F0h	ICU	Interrupt Request Register 240	IR240	8	8	2 ICLK
0008 70F1h	ICU	Interrupt Request Register 241	IR241	8	8	2 ICLK
0008 70F2h	ICU	Interrupt Request Register 242	IR242	8	8	2 ICLK
0008 70F3h	ICU	Interrupt Request Register 243	IR243	8	8	2 ICLK
0008 70F4h	ICU	Interrupt Request Register 244	IR244	8	8	2 ICLK
0008 70F5h	ICU	Interrupt Request Register 245	IR245	8	8	2 ICLK
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt Request Register 249	IR249	8	8	2 ICLK
0008 711Bh	ICU	DTC Activation Enable Register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC Activation Enable Register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC Activation Enable Register 029	DTCER029	8	8	2 ICLK
0008 7124h	ICU	DTC Activation Enable Register 036	DTCER036	8	8	2 ICLK
0008 7125h	ICU	DTC Activation Enable Register 037	DTCER037	8	8	2 ICLK
0008 712Dh	ICU	DTC Activation Enable Register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC Activation Enable Register 046	DTCER046	8	8	2 ICLK
0008 7140h	ICU	DTC Activation Enable Register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC Activation Enable Register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC Activation Enable Register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC Activation Enable Register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC Activation Enable Register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC Activation Enable Register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC Activation Enable Register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC Activation Enable Register 071	DTCER071	8	8	2 ICLK
0008 7166h	ICU	DTC Activation Enable Register 102	DTCER102	8	8	2 ICLK
0008 7167h	ICU	DTC Activation Enable Register 103	DTCER103	8	8	2 ICLK
0008 716Ah	ICU	DTC Activation Enable Register 106	DTCER106	8	8	2 ICLK
0008 7172h	ICU	DTC Activation Enable Register 114	DTCER114	8	8	2 ICLK
0008 7173h	ICU	DTC Activation Enable Register 115	DTCER115	8	8	2 ICLK
0008 7174h	ICU	DTC Activation Enable Register 116	DTCER116	8	8	2 ICLK
0008 7175h	ICU	DTC Activation Enable Register 117	DTCER117	8	8	2 ICLK
0008 7179h	ICU	DTC Activation Enable Register 121	DTCER121	8	8	2 ICLK
0008 717Ah	ICU	DTC Activation Enable Register 122	DTCER122	8	8	2 ICLK
0008 717Dh	ICU	DTC Activation Enable Register 125	DTCER125	8	8	2 ICLK
0008 717Eh	ICU	DTC Activation Enable Register 126	DTCER126	8	8	2 ICLK
0008 7181h	ICU	DTC Activation Enable Register 129	DTCER129	8	8	2 ICLK
0008 7182h	ICU	DTC Activation Enable Register 130	DTCER130	8	8	2 ICLK
0008 7183h	ICU	DTC Activation Enable Register 131	DTCER131	8	8	2 ICLK
0008 7184h	ICU	DTC Activation Enable Register 132	DTCER132	8	8	2 ICLK
0008 7186h	ICU	DTC Activation Enable Register 134	DTCER134	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (10/16)

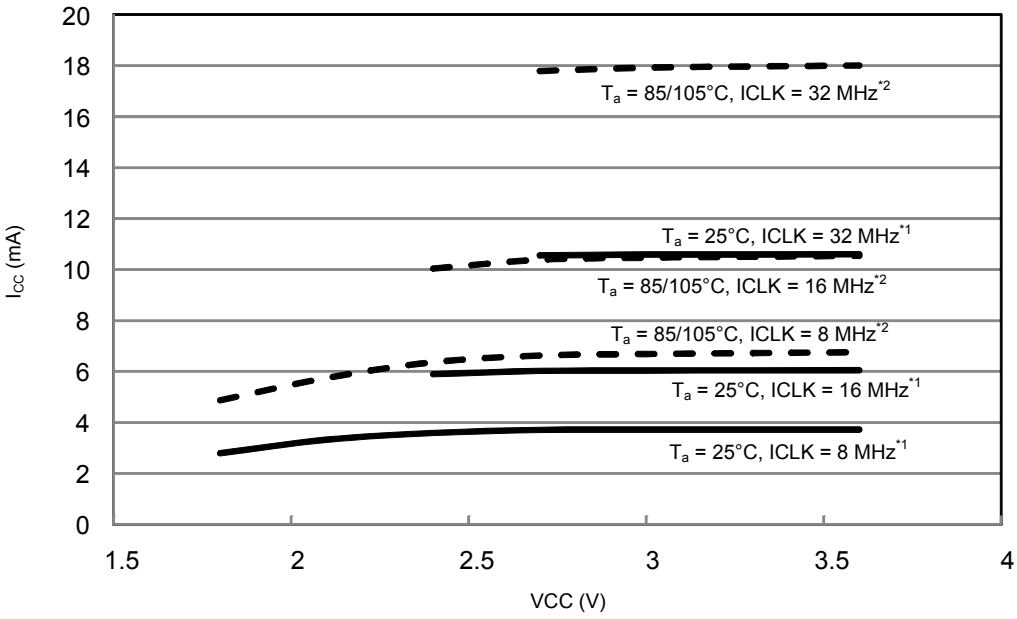
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A029h	SCI1	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A02Ah	SCI1	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A02Bh	SCI1	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A02Ch	SCI1	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A0A6h	SCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A0A9h	SCI5	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A0AAh	SCI5	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A0ABh	SCI5	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A0ACh	SCI5	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2 or 3 PCLKB
0008 B102h	ELC	Event Link Setting Register 1	ELSR1	8	8	2 or 3 PCLKB
0008 B103h	ELC	Event Link Setting Register 2	ELSR2	8	8	2 or 3 PCLKB
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2 or 3 PCLKB
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2 or 3 PCLKB
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2 or 3 PCLKB
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2 or 3 PCLKB
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2 or 3 PCLKB
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2 or 3 PCLKB
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2 or 3 PCLKB
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2 or 3 PCLKB
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2 or 3 PCLKB
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2 or 3 PCLKB
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2 or 3 PCLKB
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2 or 3 PCLKB
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2 or 3 PCLKB
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2 or 3 PCLKB
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2 or 3 PCLKB

[128-Kbyte or less flash memory]

Table 5.7 DC Characteristics (5) (1/2)

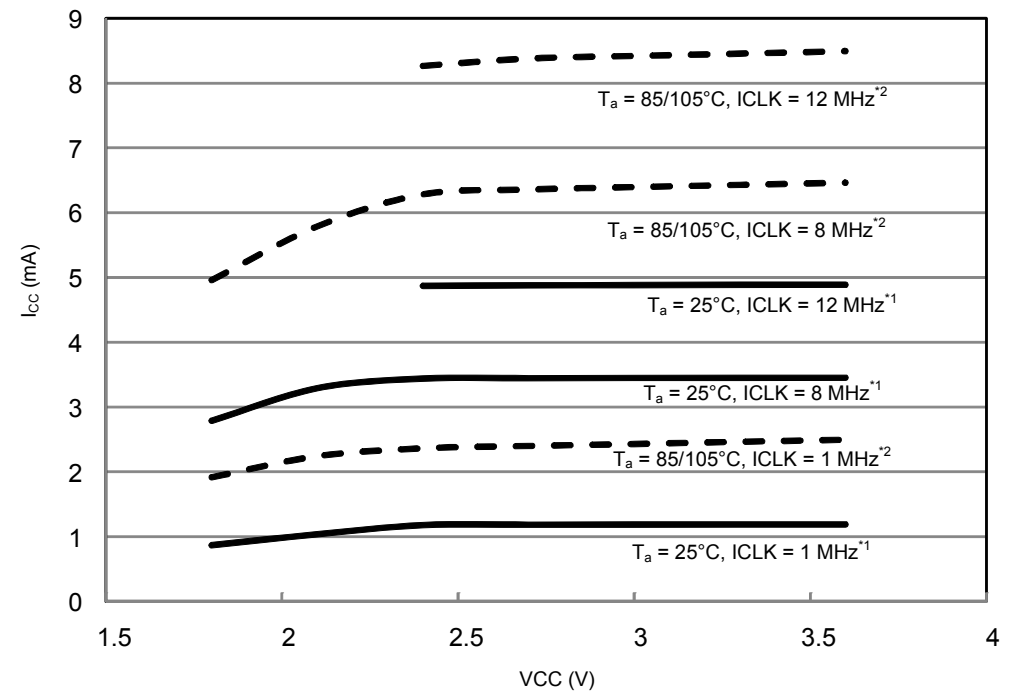
Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz	I_{CC}	3.2	—	mA	
				ICLK = 16 MHz		2.2	—		
				ICLK = 8 MHz		1.7	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		10.6	—		
				ICLK = 16 MHz		6.1	—		
				ICLK = 8 MHz		3.7	—		
			All peripheral operation: Max.*3	ICLK = 32 MHz		—	24		
		Sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.8	—		
				ICLK = 16 MHz		1.4	—		
				ICLK = 8 MHz		1.1	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		6.4	—		
				ICLK = 16 MHz		3.7	—		
				ICLK = 8 MHz		2.4	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.2	—		
				ICLK = 16 MHz		1.0	—		
				ICLK = 8 MHz		0.90	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		4.6	—		
				ICLK = 16 MHz		2.8	—		
				ICLK = 8 MHz		1.8	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I_{CC}	2.0	—	mA	
				ICLK = 8 MHz		1.3	—		
				ICLK = 1 MHz		0.75	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		4.9	—		
				ICLK = 8 MHz		3.5	—		
				ICLK = 1 MHz		1.2	—		
			All peripheral operation: Max.*7	ICLK = 12 MHz		—	11		
		Sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.4	—		
				ICLK = 8 MHz		0.85	—		
				ICLK = 1 MHz		0.65	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		3.2	—		
				ICLK = 8 MHz		2.2	—		
				ICLK = 1 MHz		1.0	—		
		Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.2	—		
				ICLK = 8 MHz		0.70	—		
				ICLK = 1 MHz		0.60	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		2.5	—		
				ICLK = 8 MHz		1.8	—		
				ICLK = 1 MHz		0.90	—		
		Increase during flash rewrite*5				2.5	—		



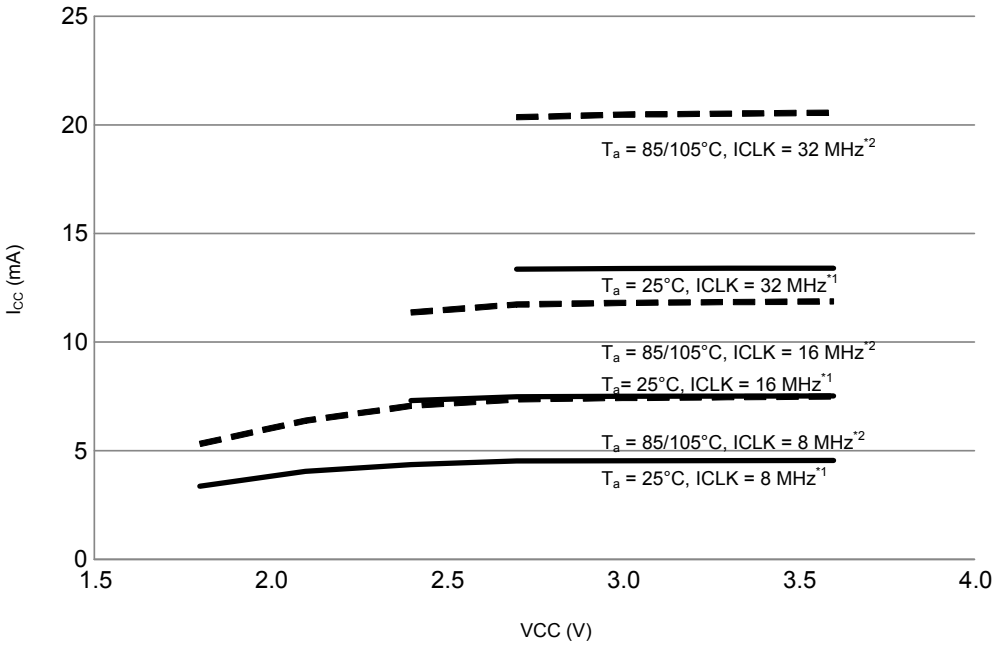
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.4 Voltage Dependency in High-Speed Operating Mode (Reference Data)

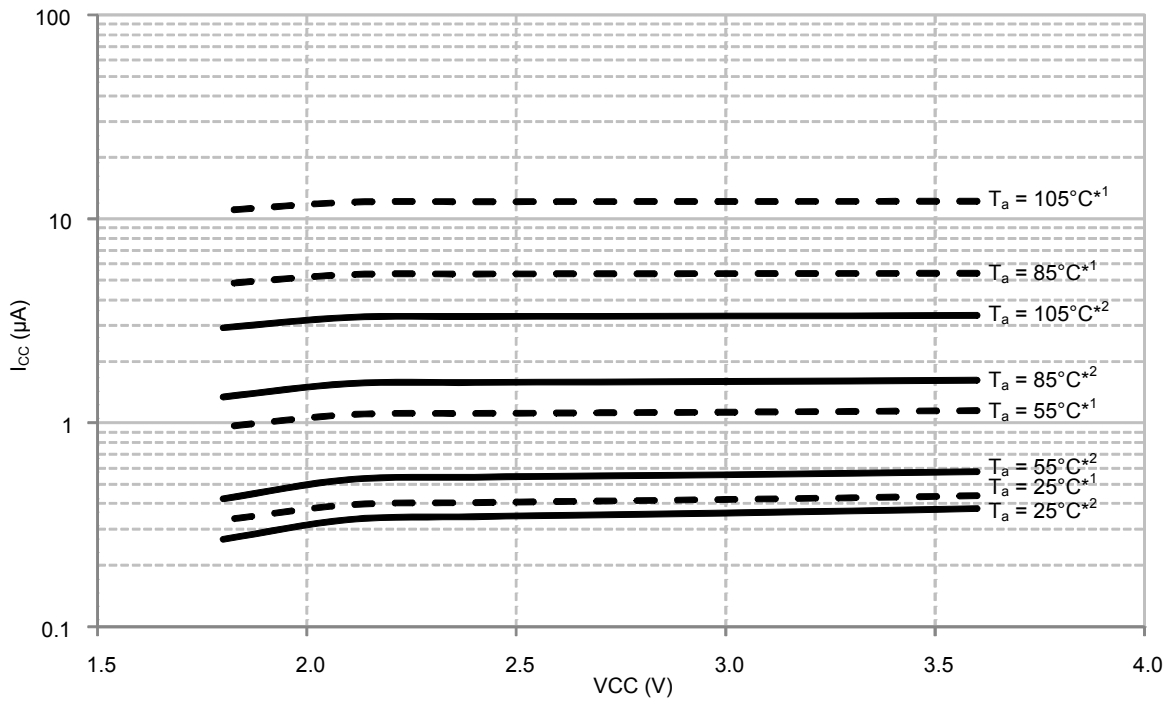
[128-Kbyte or less flash memory]

Table 5.9 DC Characteristics (7)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.35	0.53	µA	
		T_a = 55°C		0.58	1.45		
		T_a = 85°C		1.60	7.30		
		T_a = 105°C		3.30	16.50		
	Increment for RTC operation*4			0.31	—		RCR3.RTCDV[2:0] = 010b
				1.09	—		RCR3.RTCDV[2:0] = 100b
	Increment for IWDT operation			0.37	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.



Note1. Average value of the tested upper-limit samples during product evaluation.
Note2. Average value of the tested middle samples during product evaluation.

Figure 5.7 Voltage Dependency in Software Standby Mode (Reference Data)

5.3.4 Control Signal Timing

Table 5.31 Control Signal Timing

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	t_{NMICK} × 3 ≤ 200 ns
		t_{NMICK} × 3.5*2	—	—			t_{NMICK} × 3 > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	t_{IRQCK} × 3 ≤ 200 ns
		t_{IRQCK} × 3.5*3	—	—			t_{IRQCK} × 3 > 200 ns

Note: • 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

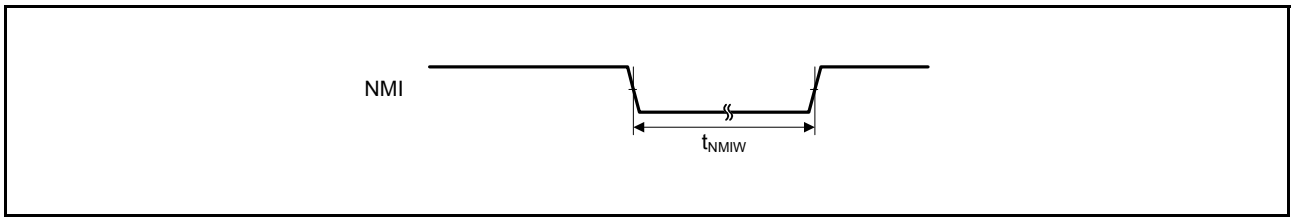


Figure 5.36 NMI Interrupt Input Timing

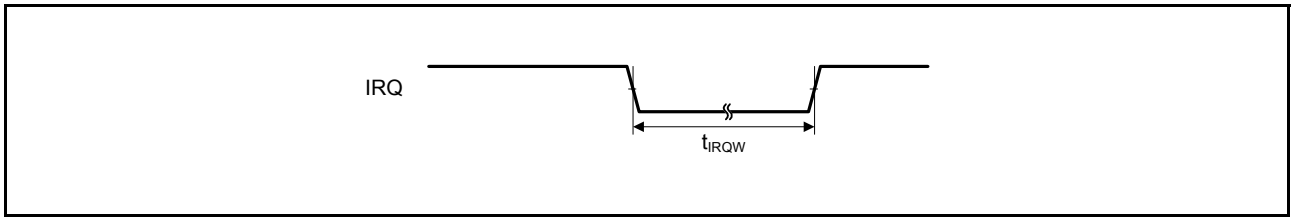


Figure 5.37 IRQ Interrupt Input Timing

Table 5.34 Timing of On-Chip Peripheral Modules (3)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
T_a = –40 to +105°C, C = 30 pF

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.46
	SCK clock cycle input (slave)			6	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	2.7 V or above	t_{SU}	65	—	ns	Figure 5.47, Figure 5.49
		1.8 V or above		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	3	—	t_{Pcyc}	
	SS input hold time		t_{LAG}	3	—	t_{Pcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	2.7 V or above		—	65		
		1.8 V or above		—	85		
	Data output hold time (master)	2.7 V or above	t_{OH}	–10	—	ns	
		1.8 V or above		–20	—		
	Data output hold time (slave)			–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.51, Figure 5.52
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

5.8 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.45 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 5.58, Figure 5.59
	Voltage detection circuit (LVD1)*1	V_{det1_4}	3.00	3.10	3.20	V	Figure 5.60 At falling edge VCC
		V_{det1_5}	2.91	3.00	3.09		
		V_{det1_6}	2.81	2.90	2.99		
		V_{det1_7}	2.70	2.79	2.88		
		V_{det1_8}	2.60	2.68	2.76		
		V_{det1_9}	2.50	2.58	2.66		
		V_{det1_A}	2.40	2.48	2.56		
		V_{det1_B}	1.99	2.06	2.13		
		V_{det1_C}	1.90	1.96	2.02		
		V_{det1_D}	1.80	1.86	1.92		

Note: • These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Table 5.46 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Voltage detection circuit (LVD2)*1	V_{det2_0}	2.71	2.90	3.09	V	Figure 5.61 At falling edge VCC
		V_{det2_1}	2.43	2.60	2.77		
		V_{det2_2}	1.87	2.00	2.13		
		V_{det2_3}*2	1.69	1.80	1.91		
Wait time after power-on reset cancellation	At normal startup*3	t_{POR}	—	9.1	—	ms	Figure 5.59
	During fast startup time*4	t_{POR}	—	1.6	—		
Wait time after voltage monitoring 1 reset cancellation	Power-on voltage monitoring 1 reset disabled*3	t_{LVD1}	—	568	—	µs	Figure 5.60
	Power-on voltage monitoring 1 reset enabled*4		—	100	—		
Wait time after voltage monitoring 2 reset cancellation		t_{LVD2}	—	100	—	µs	Figure 5.61
Response delay time		t_{det}	—	—	350	µs	Figure 5.58
Minimum VCC down time*5		t_{VOFF}	350	—	—	µs	Figure 5.58, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 5.59, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	300	µs	Figure 5.60, Figure 5.61
Hysteresis width (LVD1 and LVD2)		V_{LVH}	—	70	—	mV	Vdet1_4 selected
			—	60	—		Vdet1_5 to 9, LVD2 selected
			—	50	—		When selection is from among Vdet1_A to B.
			—	40	—		When selection is from among Vdet1_C to D.

Note: • These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.

Note 2. Vdet2_3 selection can be used only when the CMPA2 pin input voltage is selected and cannot be used when the power supply voltage (VCC) is selected.

Note 3. When OFS1.(STUPLVD1REN, FASTSTUP) = 11b.

Note 4. When OFS1.(STUPLVD1REN, FASTSTUP) ≠ 11b.

Note 5. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

5.9 Oscillation Stop Detection Timing

Table 5.47 Oscillation Stop Detection Circuit Characteristics

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.62

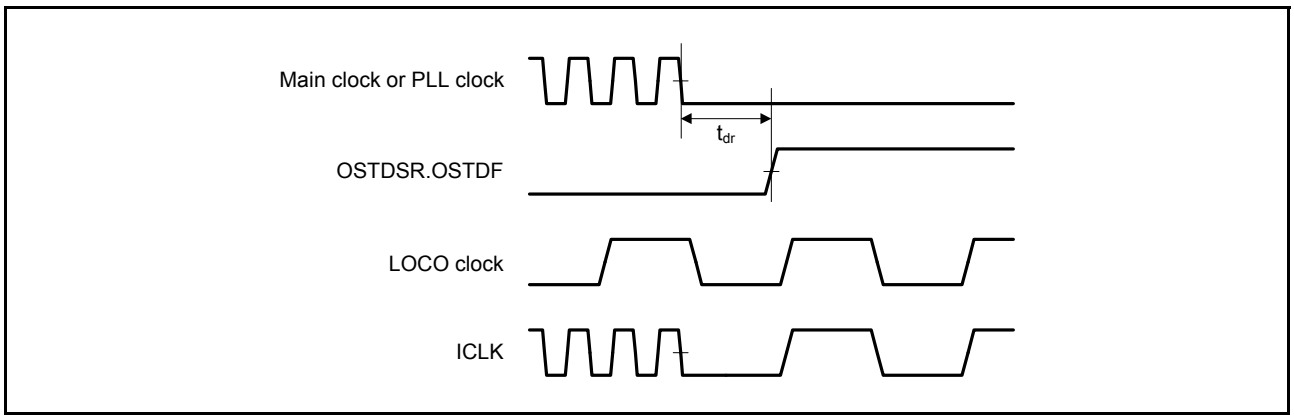
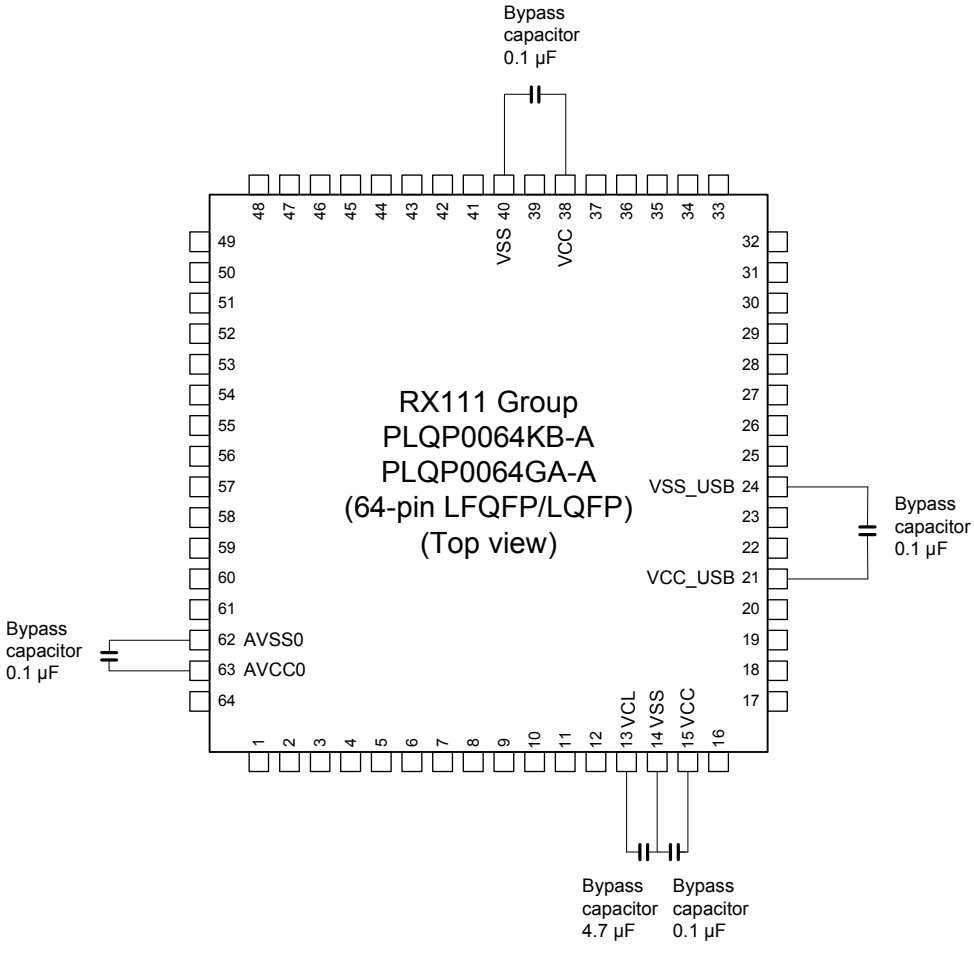


Figure 5.62 Oscillation Stop Detection Timing

5.12 Usage Notes

5.12.1 Connecting VCL Capacitor and Bypass Capacitors

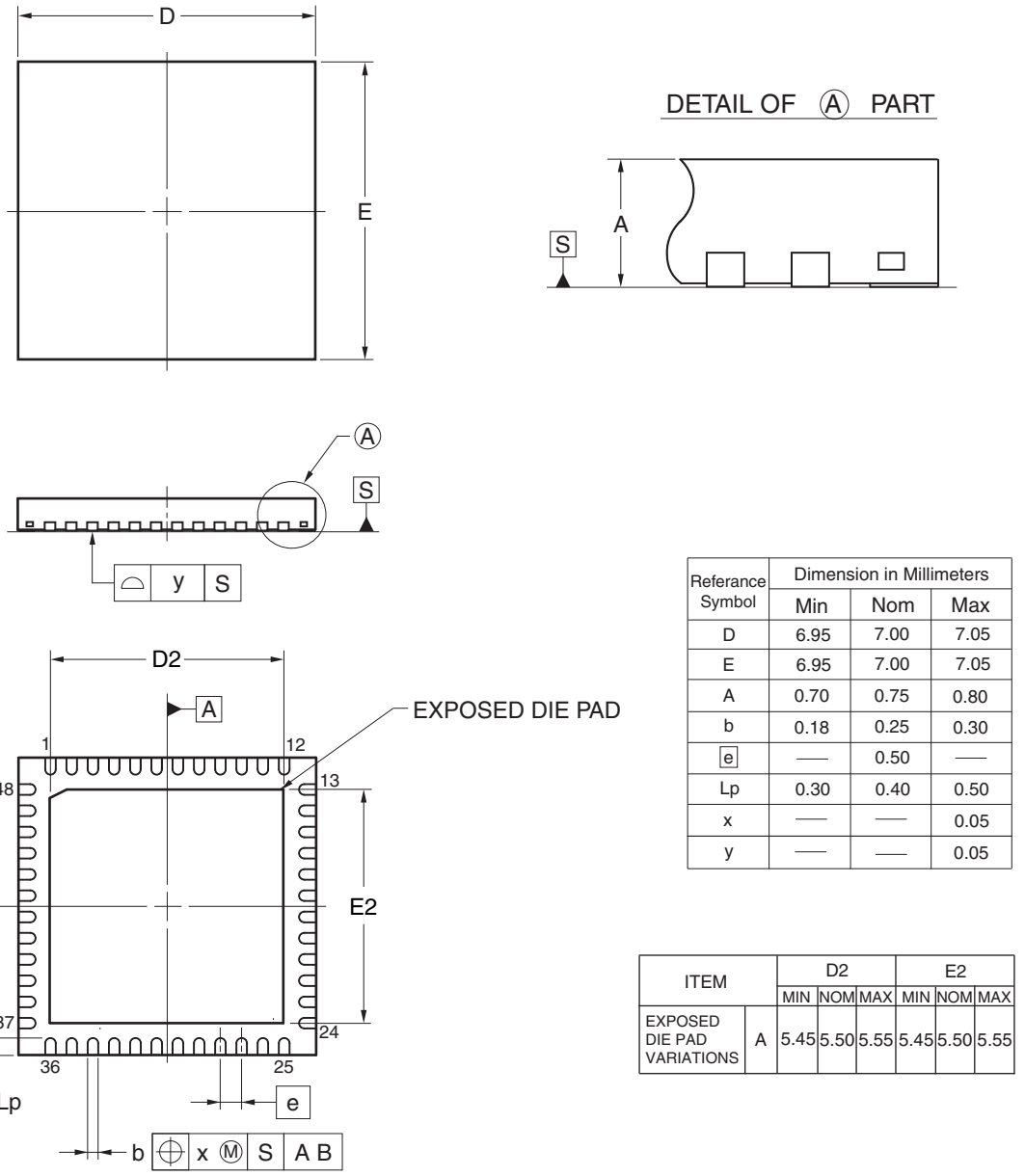
This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU to adjust automatically to the optimum level. A 4.7-µF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and VSS pin. Figure 5.63 to Figure 5.64 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin. Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor to the MCU power supply pins as close as possible. Use a recommended value of 0.1 µF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 30, 12-Bit A/D Converter (S12ADb) in the User's Manual: Hardware.
For notes on designing the printed circuit board, see the descriptions of the application note "Hardware Design Guide" (R01AN1411EJ). The latest version can be downloaded from Renesas Electronics Website.



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 5.63 Connecting Capacitors (64 Pins)

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-5	0.13



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	0.70	0.75	0.80
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	5.45	5.50	5.55	5.45	5.50	5.55

Figure E 48-Pin HWQFN (PWQN0048KB-A)

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.