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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SCI, SPI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51114adfm-3a

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products (1/2)

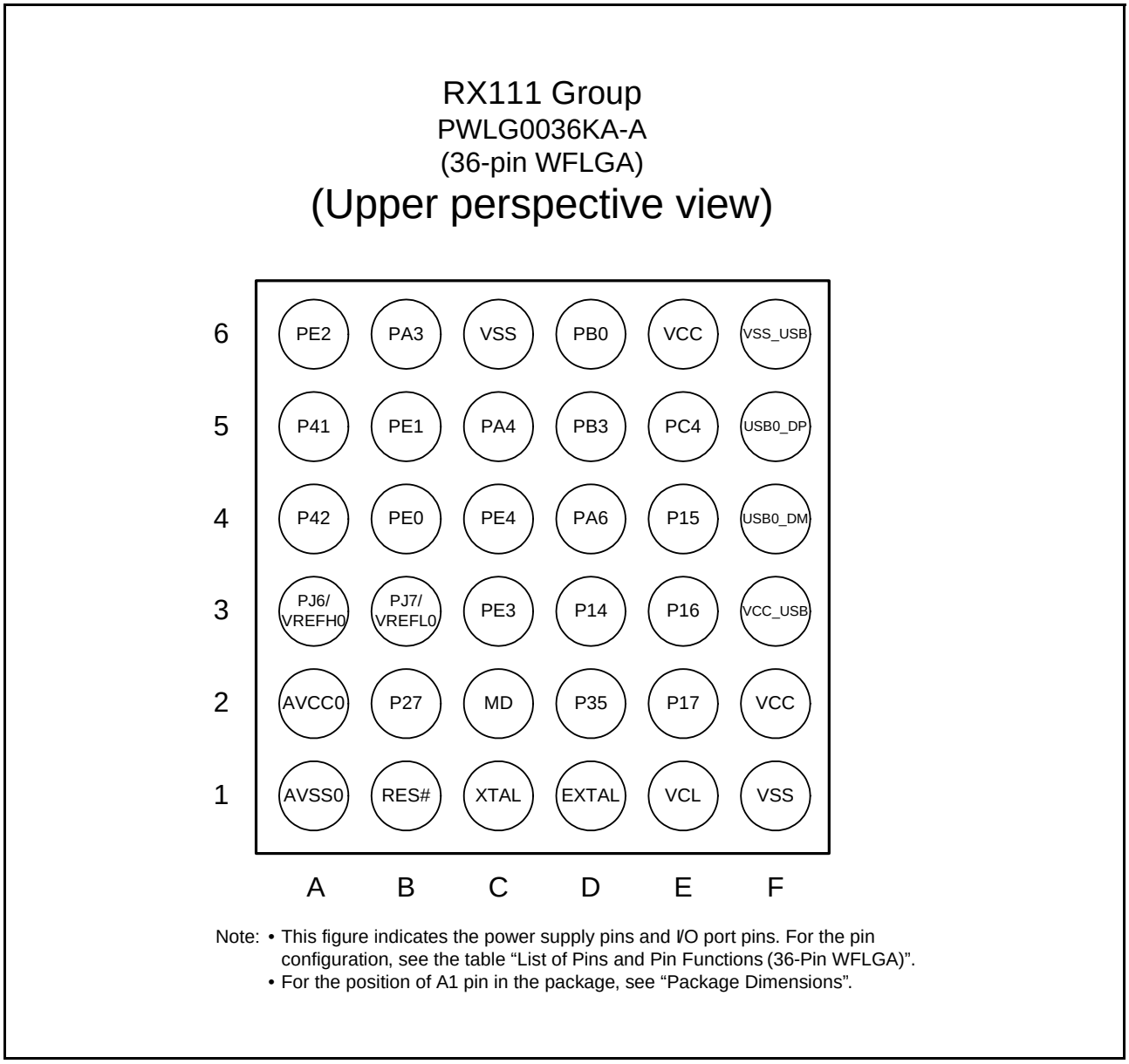
Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Maximum Operating Frequency	Operating Temperature
RX111	R5F51118AGFM	R5F51118AGFM#3A	PLQP0064KB-A	512 Kbytes	64 Kbytes	8 Kbytes	32 MHz	–40 to +105°C
	R5F51118AGFK	R5F51118AGFK#3A	PLQP0064GA-A					
	R5F51118AGFL	R5F51118AGFL#3A	PLQP0048KB-A					
	R5F51118AGNE	R5F51118AGNE#UA	PWQN0048KB-A					
	R5F51117AGFM	R5F51117AGFM#3A	PLQP0064KB-A	384 Kbytes				
	R5F51117AGFK	R5F51117AGFK#3A	PLQP0064GA-A					
	R5F51117AGFL	R5F51117AGFL#3A	PLQP0048KB-A					
	R5F51117AGNE	R5F51117AGNE#UA	PWQN0048KB-A					
	R5F51116AGFM	R5F51116AGFM#3A	PLQP0064KB-A	256 Kbytes	32 Kbytes			
	R5F51116AGFK	R5F51116AGFK#3A	PLQP0064GA-A					
	R5F51116AGFL	R5F51116AGFL#3A	PLQP0048KB-A					
	R5F51116AGNE	R5F51116AGNE#UA	PWQN0048KB-A					
	R5F51115AGFM	R5F51115AGFM#3A	PLQP0064KB-A	128 Kbytes	16 Kbytes			
	R5F51115AGFK	R5F51115AGFK#3A	PLQP0064GA-A					
	R5F51115AGFL	R5F51115AGFL#3A	PLQP0048KB-A					
	R5F51115AGNE	R5F51115AGNE#UA	PWQN0048KB-A					
	R5F51114AGFM	R5F51114AGFM#3A	PLQP0064KB-A	96 Kbytes				
	R5F51114AGFK	R5F51114AGFK#3A	PLQP0064GA-A					
	R5F51114AGFL	R5F51114AGFL#3A	PLQP0048KB-A					
	R5F51114AGNE	R5F51114AGNE#UA	PWQN0048KB-A					
	R5F51113AGFM	R5F51113AGFM#3A	PLQP0064KB-A	64 Kbytes	10 Kbytes			
	R5F51113AGFK	R5F51113AGFK#3A	PLQP0064GA-A					
	R5F51113AGFL	R5F51113AGFL#3A	PLQP0048KB-A					
	R5F51113AGNE	R5F51113AGNE#UA	PWQN0048KB-A					
	R5F51113AGNF	R5F51113AGNF#UA	PWQN0040KC-A					
	R5F51111AGFM	R5F51111AGFM#3A	PLQP0064KB-A	32 Kbytes				
	R5F51111AGFK	R5F51111AGFK#3A	PLQP0064GA-A					
	R5F51111AGFL	R5F51111AGFL#3A	PLQP0048KB-A					
	R5F51111AGNE	R5F51111AGNE#UA	PWQN0048KB-A					
	R5F51111AGNF	R5F51111AGNF#UA	PWQN0040KC-A					
	R5F5111JAGFM	R5F5111JAGFM#3A	PLQP0064KB-A	16 Kbytes	8 Kbytes			
	R5F5111JAGFK	R5F5111JAGFK#3A	PLQP0064GA-A					
	R5F5111JAGFL	R5F5111JAGFL#3A	PLQP0048KB-A					
	R5F5111JAGNE	R5F5111JAGNE#UA	PWQN0048KB-A					
	R5F5111JAGNF	R5F5111JAGNF#UA	PWQN0040KC-A					

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VCC_USB	Input	Power supply pin for USB. Connect this pin to VCC.
	VSS_USB	Input	Ground pin for USB. Connect this pin to VSS.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC when not using the 12-bit A/D converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS when not using the 12-bit A/D converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC when not using the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS when not using the 12-bit A/D converter.
Clock	XTAL	Output/ Input *1	Pins for connecting a crystal. An external clock can be input through the XTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
	UB#	Input	Pin used for boot mode (USB interface).
	UPSEL	Input	Pin used for boot mode (USB interface).
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
LVD	CMPA2	Input	Detection target voltage pin for voltage detection 2
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (36-Pin WFLGA)”.
• For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.7 Pin Assignments of the 36-Pin WFLGA

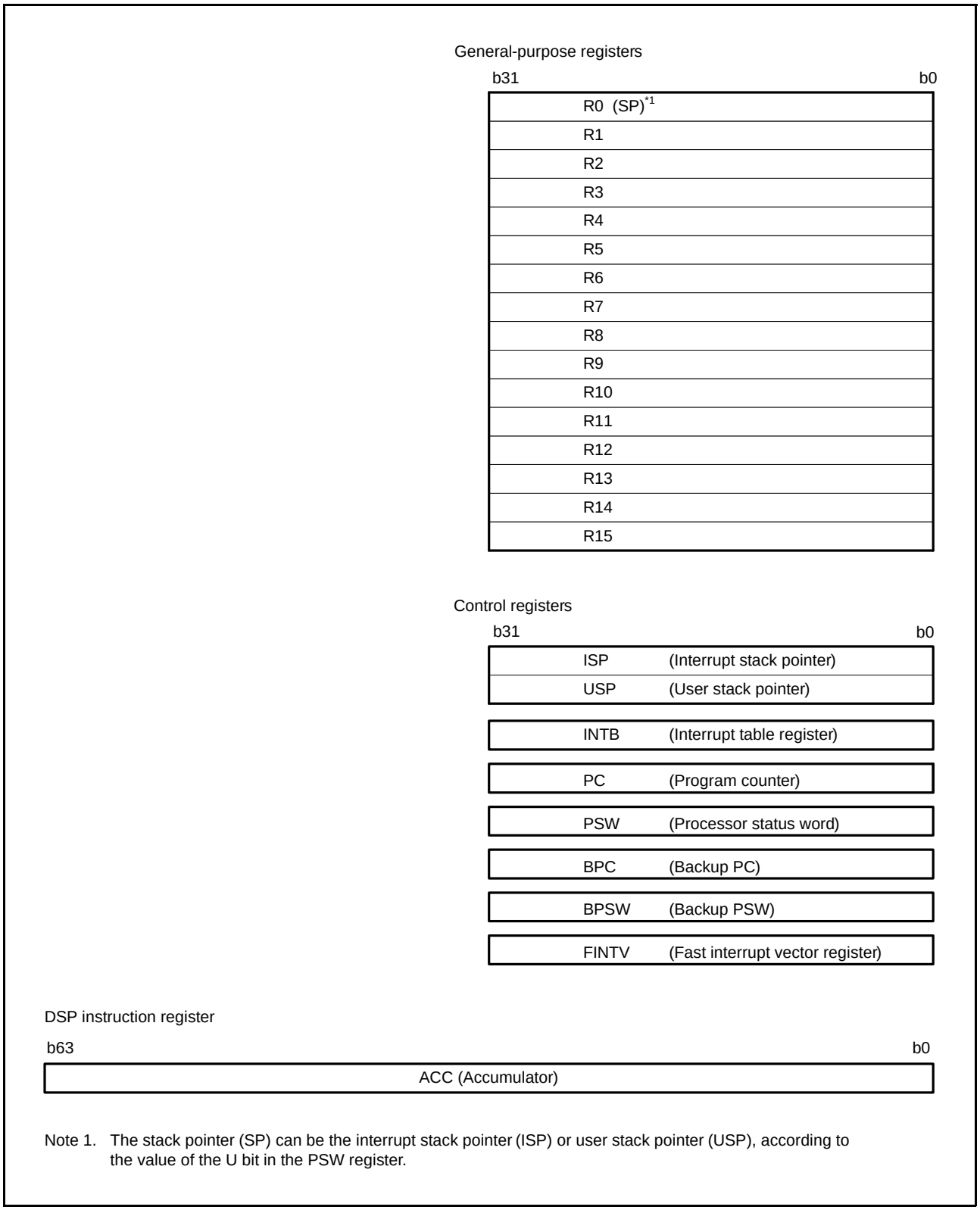
Table 1.7 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC)	Communication (SCIe, SCIf, RSPI, RIIC, USB)	Others
39		PE0	MTIOC2A/POE3#	SCK12	IRQ0/AN008
40		PE7			IRQ7/AN015
41		P46*2			AN006
42		P42*2			AN002
43		P41*2			AN001
44	VREFL0	PJ7*2			
45		P40*2			AN000
46	VREFH0	PJ6*2			
47	AVSS0				
48	AVCC0				

Note 1. Not 5 V tolerant.
Note 2. The power source of the I/O buffer for these pins is AVCC0.

2. CPU

Figure 2.1 shows the register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (14/16)

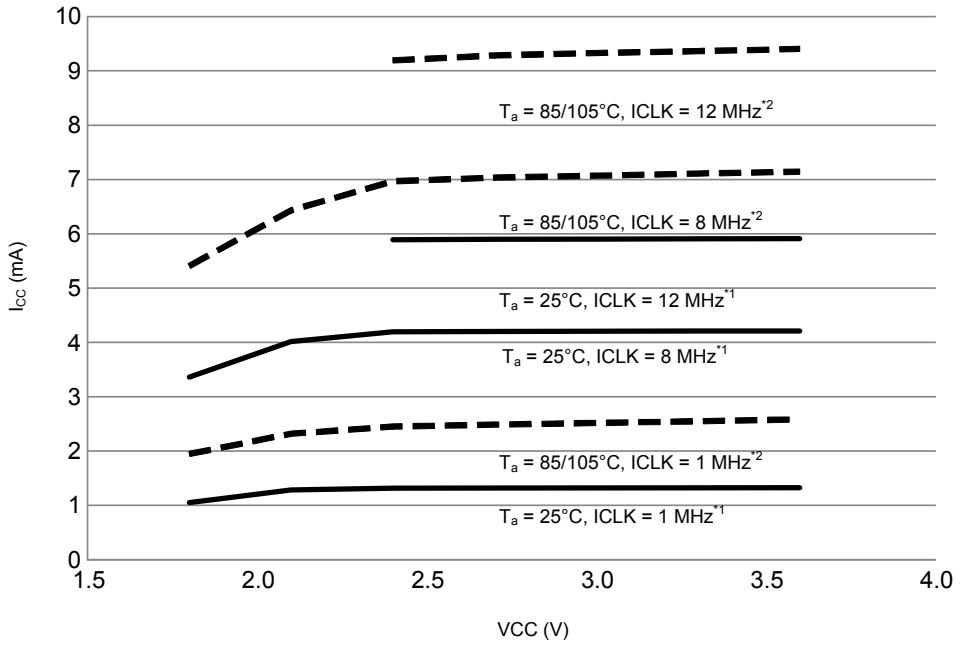
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2 or 3 PCLKB
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2 or 3 PCLKB
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2 or 3 PCLKB
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2 or 3 PCLKB
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2 or 3 PCLKB
0008 C1A7h	MPC	PC7 Pin Function Control Register	PC7PFS	8	8	2 or 3 PCLKB
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2 or 3 PCLKB
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2 or 3 PCLKB
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2 or 3 PCLKB
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2 or 3 PCLKB
0008 C1D6h	MPC	PJ6 Pin Function Control Register	PJ6PFS	8	8	2 or 3 PCLKB
0008 C1D7h	MPC	PJ7 Pin Function Control Register	PJ7PFS	8	8	2 or 3 PCLKB
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4 or 5 PCLKB
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB
0008 C408h	RTC	Day-Of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB

[256-Kbyte or more flash memory]

Table 5.8 DC Characteristics (6) (1/2)

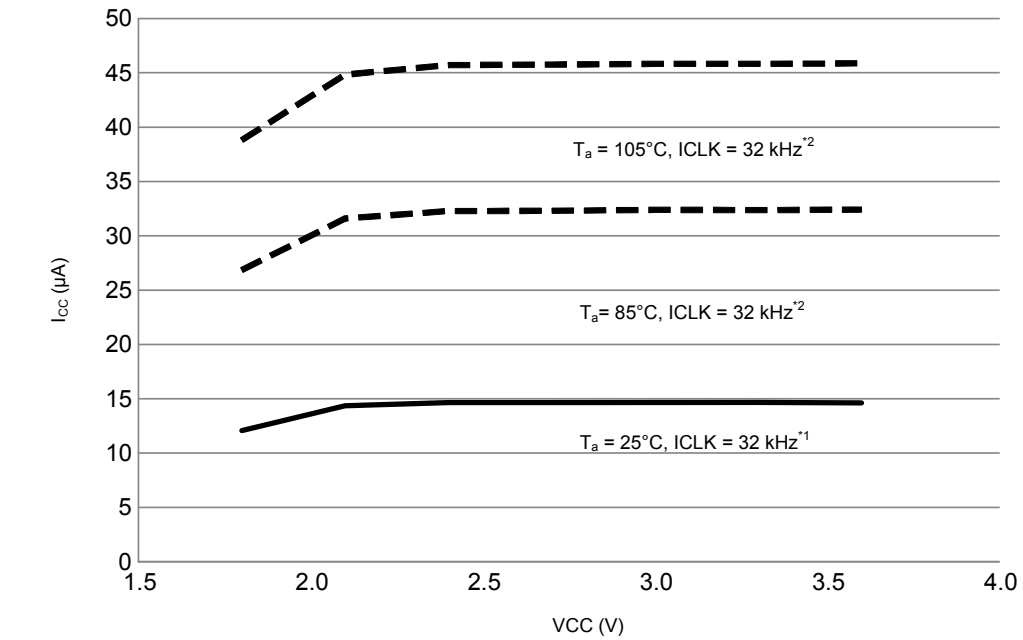
Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz	I_{CC}	3.6	—	mA	
				ICLK = 16 MHz		2.4	—		
				ICLK = 8 MHz		1.8	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		13.4	—		
				ICLK = 16 MHz		7.5	—		
				ICLK = 8 MHz		4.5	—		
			All peripheral operation: Max.*3	ICLK = 32 MHz		—	27		
		Sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.9	—		
				ICLK = 16 MHz		1.5	—		
				ICLK = 8 MHz		1.3	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		7.6	—		
				ICLK = 16 MHz		4.4	—		
				ICLK = 8 MHz		2.8	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.1	—		
				ICLK = 16 MHz		1.0	—		
				ICLK = 8 MHz		0.9	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		5.8	—		
				ICLK = 16 MHz		3.4	—		
				ICLK = 8 MHz		2.1	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I_{CC}	2.1	—	mA	
				ICLK = 8 MHz		1.4	—		
				ICLK = 1 MHz		0.8	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		5.9	—		
				ICLK = 8 MHz		4.2	—		
				ICLK = 1 MHz		1.3	—		
			All peripheral operation: Max.*7	ICLK = 12 MHz		—	12.2		
		Sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.4	—		
				ICLK = 8 MHz		0.9	—		
				ICLK = 1 MHz		0.7	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		3.6	—		
				ICLK = 8 MHz		2.5	—		
				ICLK = 1 MHz		1.1	—		
		Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.1	—		
				ICLK = 8 MHz		0.6	—		
				ICLK = 1 MHz		0.6	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		2.9	—		
				ICLK = 8 MHz		2.0	—		
				ICLK = 1 MHz		0.9	—		
		Increase during flash rewrite*5				2.5	—		



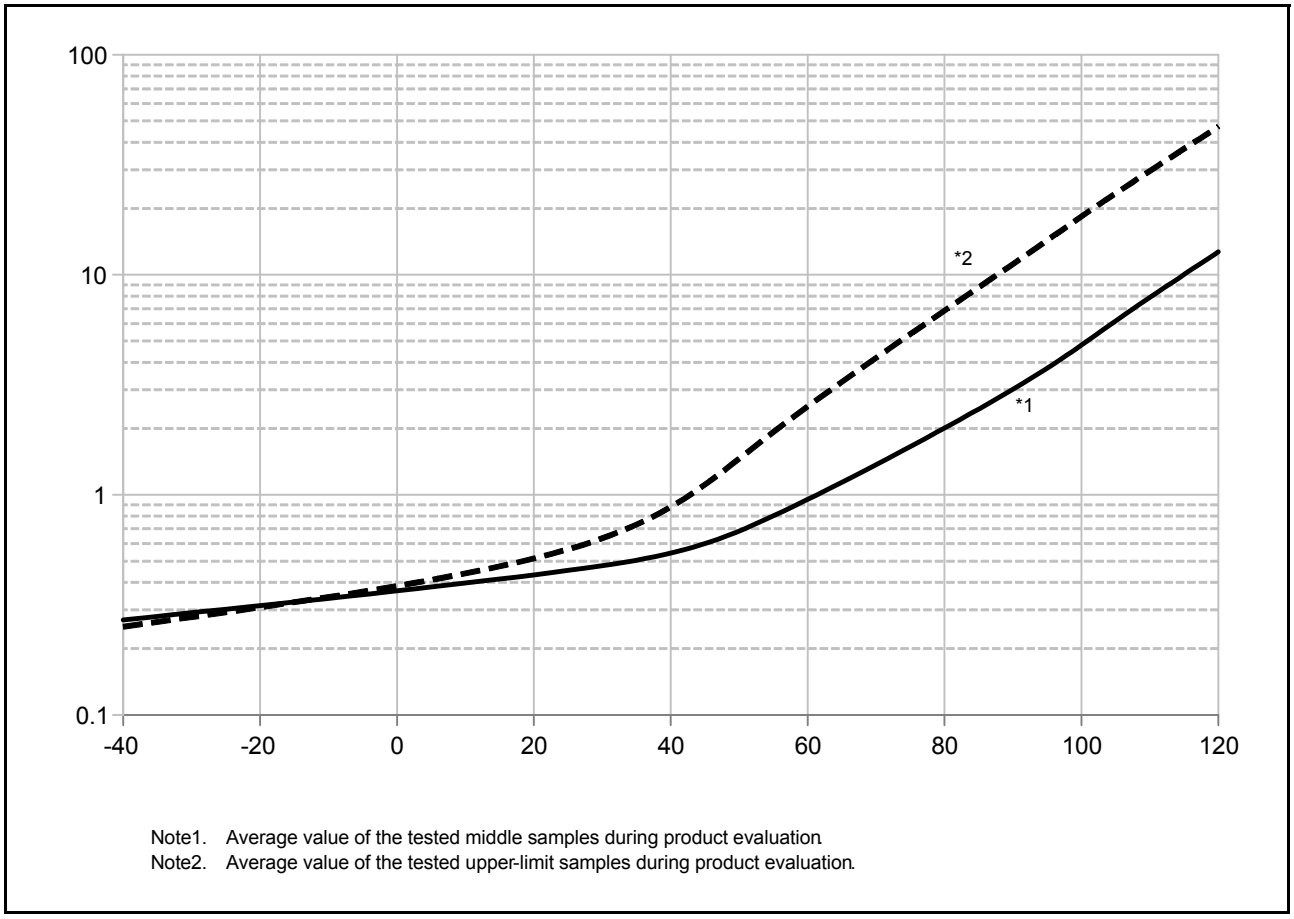
Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.5 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.6 Voltage Dependency in Low-Speed Operating Mode (Reference Data)



Note1. Average value of the tested middle samples during product evaluation.
Note2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.10 Temperature Dependency in Software Standby Mode (Reference Data)

Table 5.11 DC Characteristics (9)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	300	mW	D version (T_a = -40 to 85°C)
		—	105		G version (T_a = -40 to 105°C)*2

Note 1. Total power dissipated by the entire chip (including output currents).
Note 2. Please contact Renesas Electronics sales office for derating under T_a = +85°C to 105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 5.18 Permissible Output Currents (2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
T_a = –40 to +105°C (G version)

Item		Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7	I_{OL}	0.4	mA
	Ports other than above		8.0	
Permissible output low current (maximum value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7		0.4	
	Ports other than above		8.0	
Permissible output low current	Total of ports P40 to P44, P46, ports PJ6, PJ7	ΣI_{OL}	1.6	
	Total of ports P03, P05, ports P26, P27, ports P30, P31		20	
	Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7		20	
	Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7		20	
	Total of all output pins		40	
Permissible output high current (average value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7	I_{OH}	–0.1	
	Ports other than above		–4.0	
Permissible output high current (maximum value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7		–0.1	
	Ports other than above		–4.0	
Permissible output high current	Total of ports P40 to P44, P46, ports PJ6, PJ7	ΣI_{OH}	–0.6	
	Total of ports P03, P05, ports P26, P27, ports P30, P31		–10	
	Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7		–15	
	Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7		–15	
	Total of all output pins		–40	

Note: Do not exceed the permissible total supply current.

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.21 Operation Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC				Unit
			1.8 to 2.4 V	2.4 to 2.7 V	2.7 to 3.6 V	When USB in Use*4	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	16	32	24	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	24	
	Peripheral module clock (PCLKB)		8	16	32	24	
	Peripheral module clock (PCLKD)*3		8	16	32	24	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.
Note 4. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.

Table 5.22 Operation Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC				Unit
			1.8 to 2.4 V	2.4 to 2.7 V	2.7 to 3.6 V	When USB in Use*4	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	12	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	12	
	Peripheral module clock (PCLKB)		8	12	12	12	
	Peripheral module clock (PCLKD)*3		8	12	12	12	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.
Note 4. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.

Table 5.23 Operation Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 to 2.4 V	2.4 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKD)*2		32.768			

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

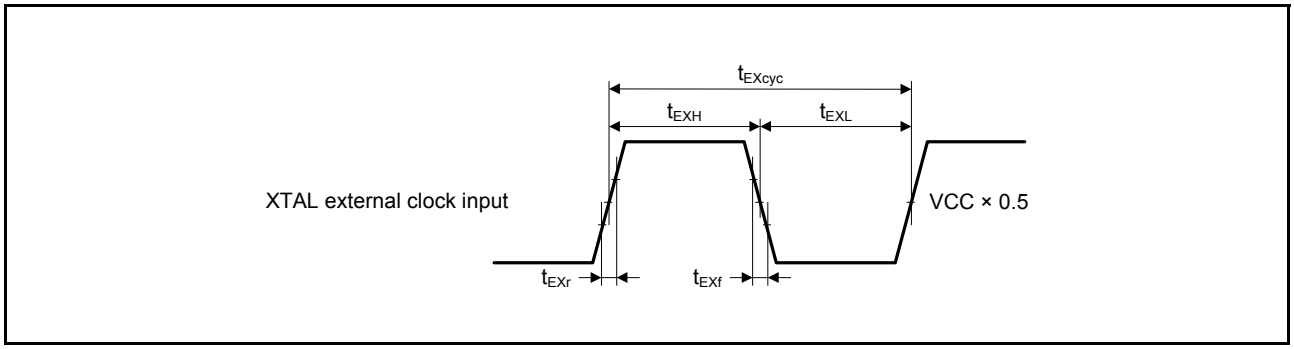


Figure 5.23 XTAL External Clock Input Timing

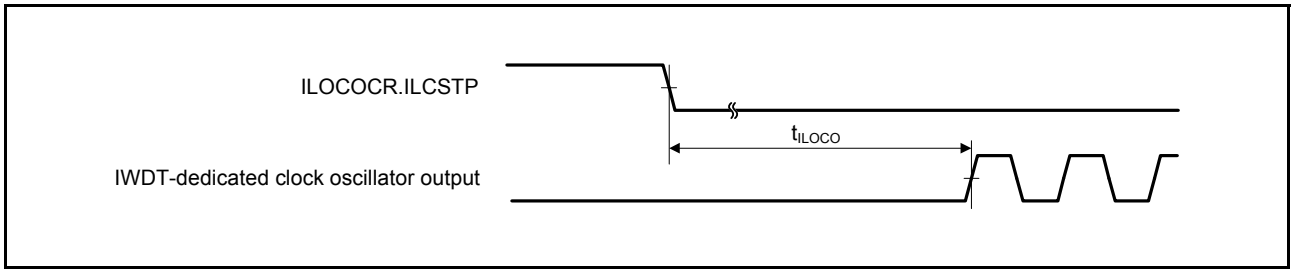


Figure 5.24 IWDT-Dedicated Clock Oscillation Start Timing

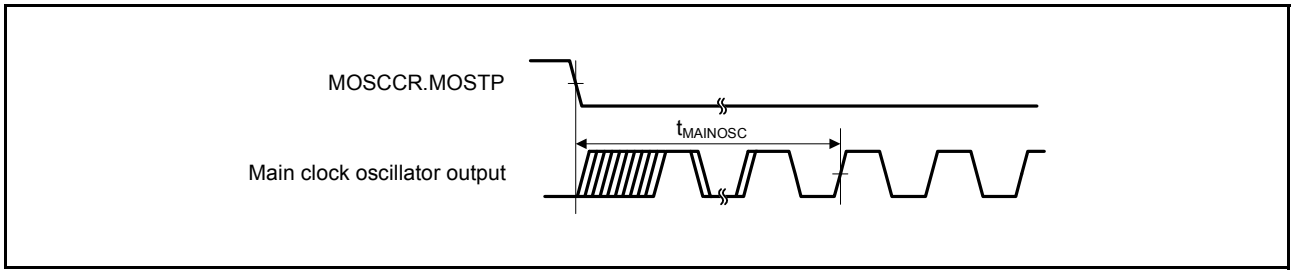


Figure 5.25 Main Clock Oscillation Start Timing

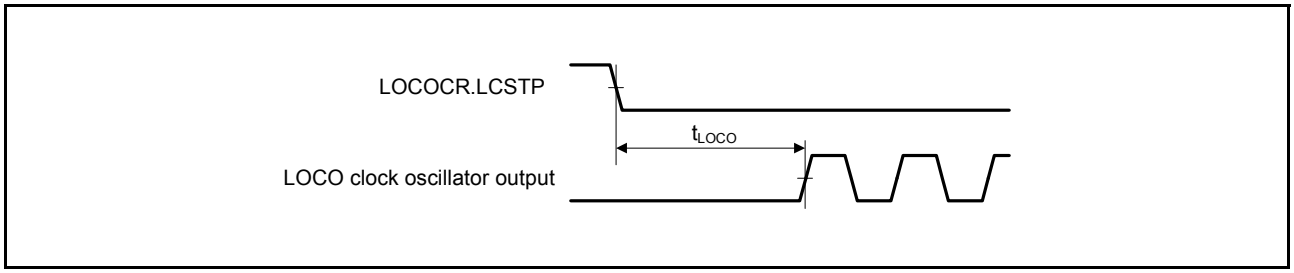


Figure 5.26 LOCO Clock Oscillation Start Timing

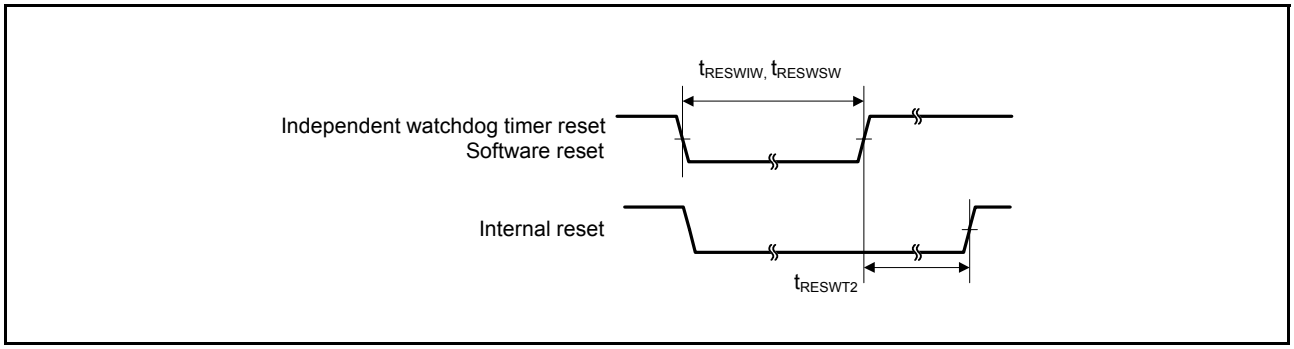


Figure 5.33 Reset Input Timing (2)

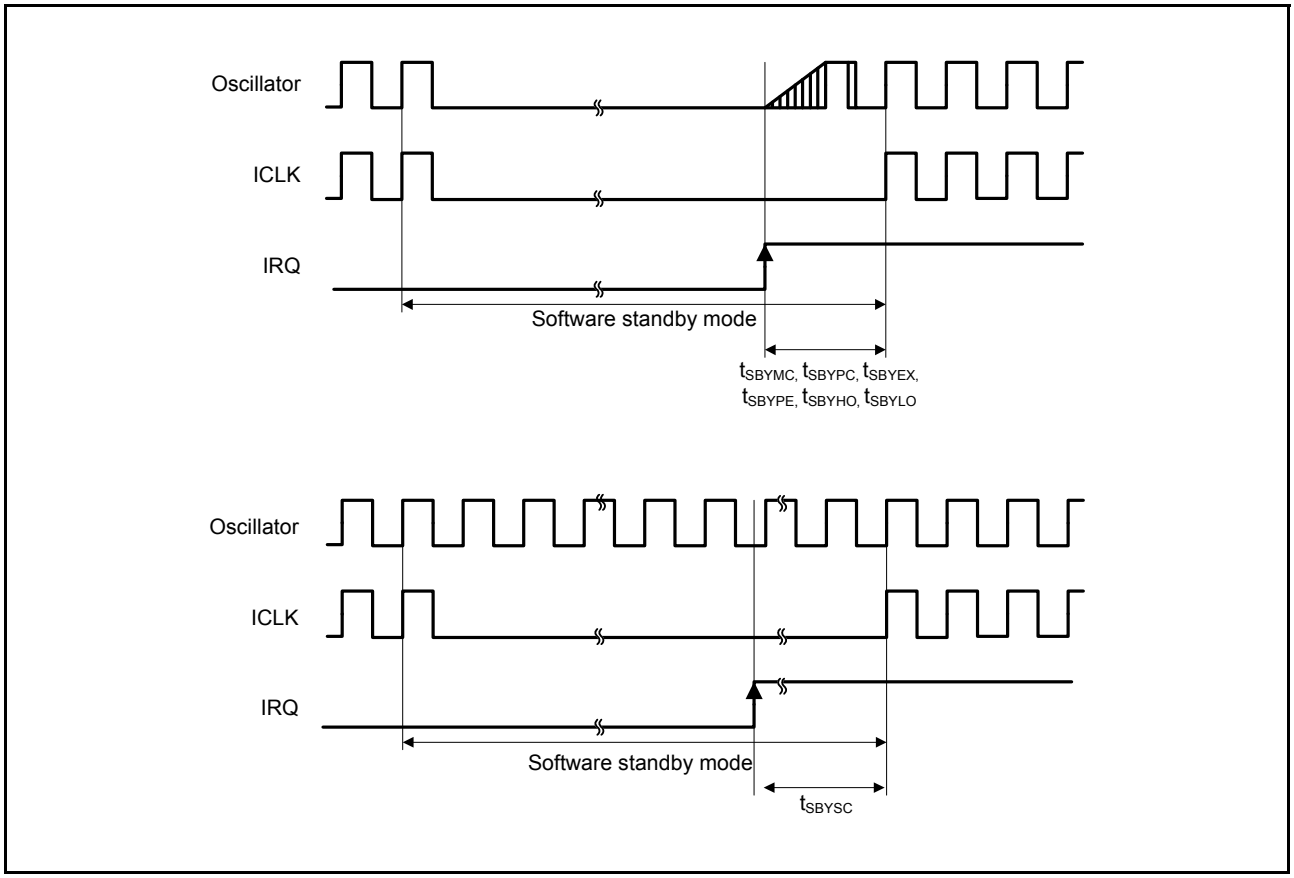


Figure 5.34 Software Standby Mode Cancellation Timing

Table 5.33 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
T_a = –40 to +105°C, C = 30 pF

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc} *1	Figure 5.46
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.47 to Figure 5.52
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$-30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$-30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			1.8 V or above		—	30		
		Slave	2.7 V or above		—	$3 \times t_{Pcyc} + 65$		
			1.8 V or above		—	$3 \times t_{Pcyc} + 105$		
	Data output hold time	Master	2.7 V or above	t_{OH}	0	—	ns	
			1.8 V or above		–20	—		
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V or above		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	20	ns	
		Input			—	1	µs	
	Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.51, Figure 5.52
			1.8 V or above		—	7		
	Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}	
			1.8 V or above		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

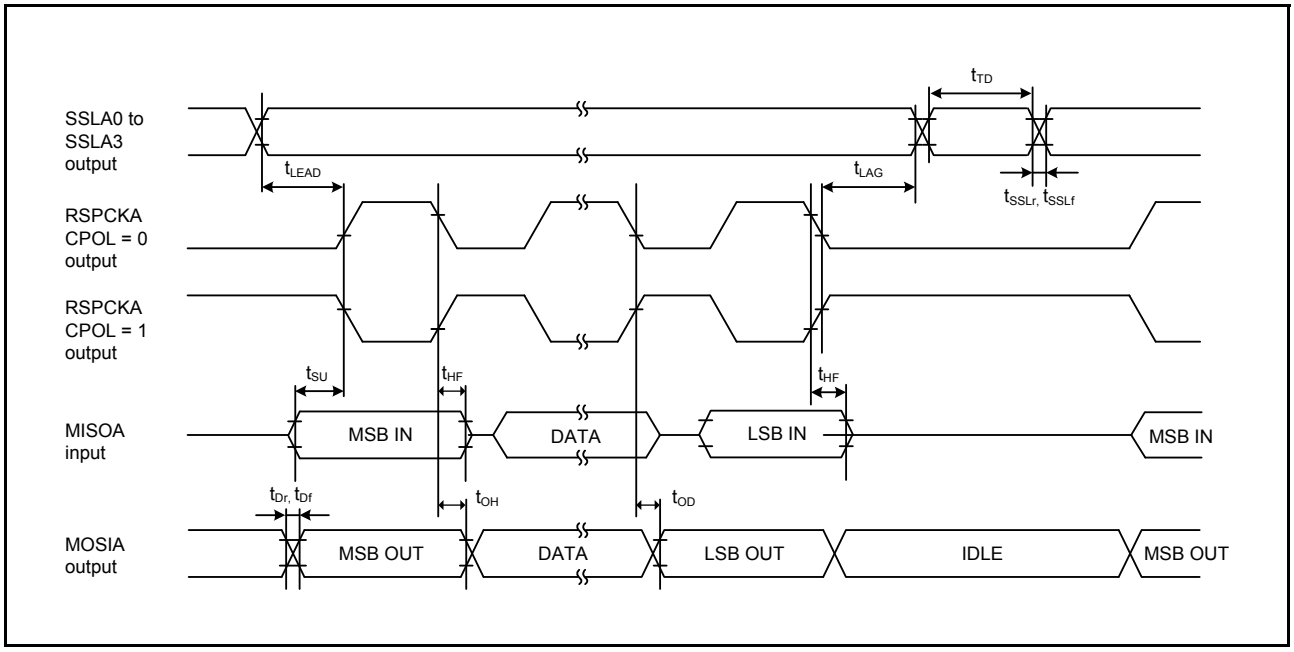


Figure 5.48 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2)

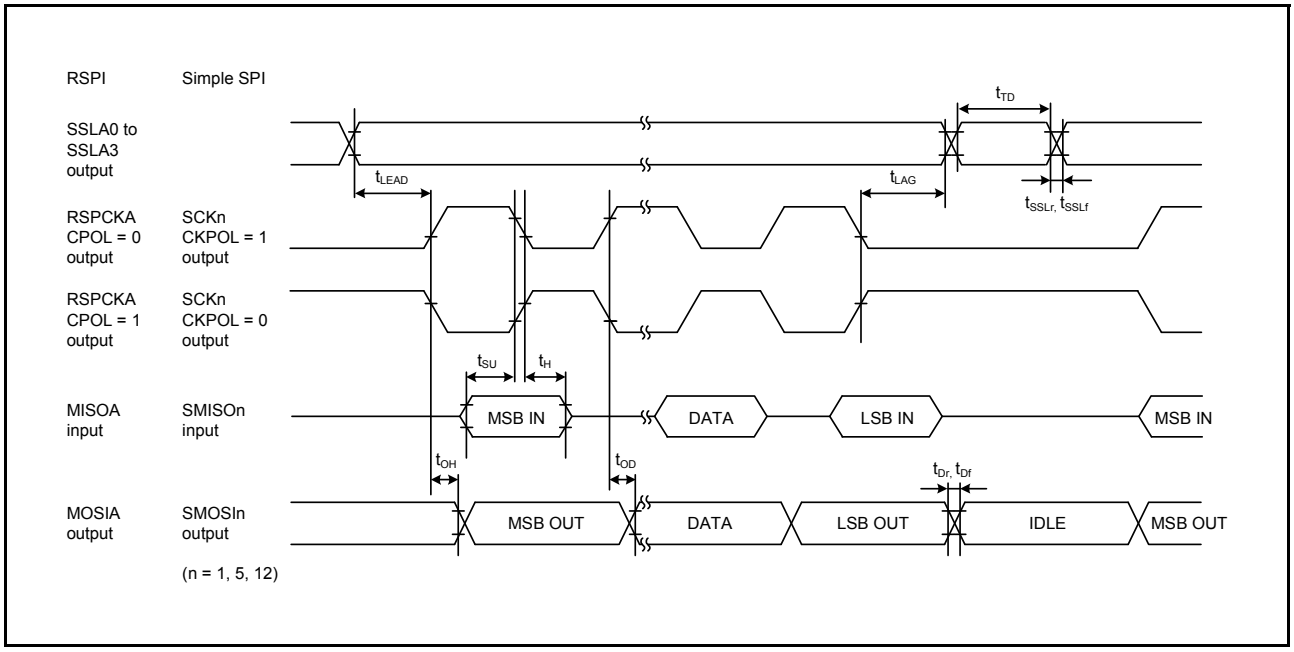


Figure 5.49 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 0)

Table 5.39 A/D Conversion Characteristics (2)

Conditions: 2.4 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.4 V ≤ AVCC0 ≤ 3.6 V, 2.4 V ≤ VREFH0 ≤ AVCC0, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		4	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 1.0 kΩ	2.062 (0.625)*2	—	—	µs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 09h
		2.750 (1.313)*2	—	—	µs	Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±6.0	LSB	
Full-scale error		—	±1.25	±6.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.40 A/D Conversion Characteristics (3)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, 1.8 V ≤ VREFH0 ≤ AVCC0, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5.0 kΩ	4.875 (1.250)*2	—	—	µs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 09h
		6.250 (2.625)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±24.0	LSB	
Full-scale error		—	±1.25	±24.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.75	±32.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.25	±12.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

5.11 E2 DataFlash Characteristics

Table 5.51 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2, *3	—	—	Year	Ta = +85°C
	After 100000 times of N_{DPEC}		5*2, *3	—	—	Year	
	After 1000000 times of N_{DPEC}		—	1*2, *3	—	Year	Ta = +25°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in 1-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristics when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 5.52 E2 DataFlash Characteristics (2) : high-speed operating mode

Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	86	761	—	40.5	374	µs
Erasure time	1-Kbyte	t_{DE1K}	—	17.4	456	—	6.15	228	ms
	8-Kbyte	t_{DE8K}	—	60.4	499	—	9.3	231	ms
Blank check time	1-byte	t_{DBC1}	—	—	48	—	—	15.9	µs
	1-Kbyte	t_{DBC1K}	—	—	1.58	—	—	0.127	µs
Erase operation forcible stop time		t_{DSED}	—	—	21.5	—	—	12.8	µs
DataFlash STOP recovery time		t_{DSTOP}	5	—	—	5	—	—	µs

Note: • Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: • The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: • The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.

Table 5.53 E2 DataFlash Characteristics (3) : middle-speed operating mode

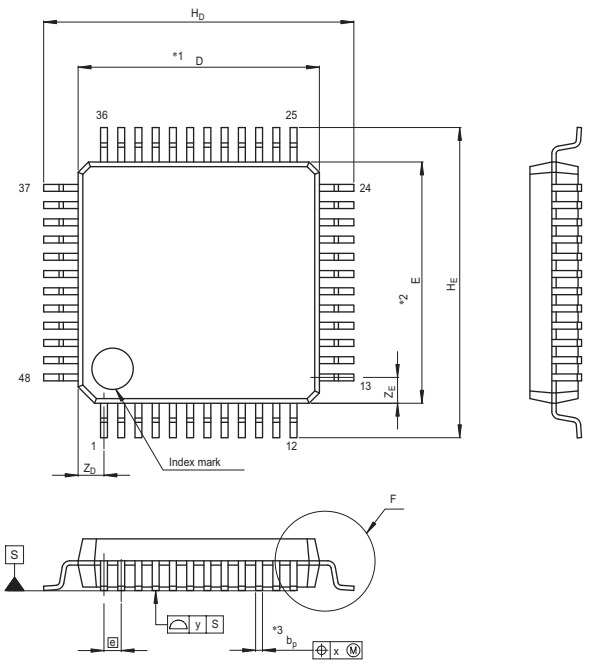
Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V

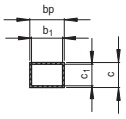
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	126	1160	—	85.4	818	µs
Erasure time	1-Kbyte	t_{DE1K}	—	17.5	457	—	7.76	259	ms
	8-Kbyte	t_{DE8K}	—	60.5	500	—	16.7	267.6	ms
Blank check time	1-byte	t_{DBC1}	—	—	78	—	—	50	µs
	1-Kbyte	t_{DBC1K}	—	—	1.61	—	—	0.369	ms
Erase operation forcible stop time		t_{DSED}	—	—	33.5	—	—	25.5	µs
DataFlash STOP recovery time		t_{DSTOP}	720	—	—	720	—	—	ns

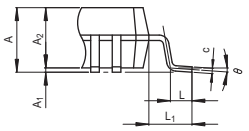
Note: • Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: • The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: • The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure D 48-Pin LFQFP (PLQP0048KB-A)

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.