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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51115adfl-v0

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

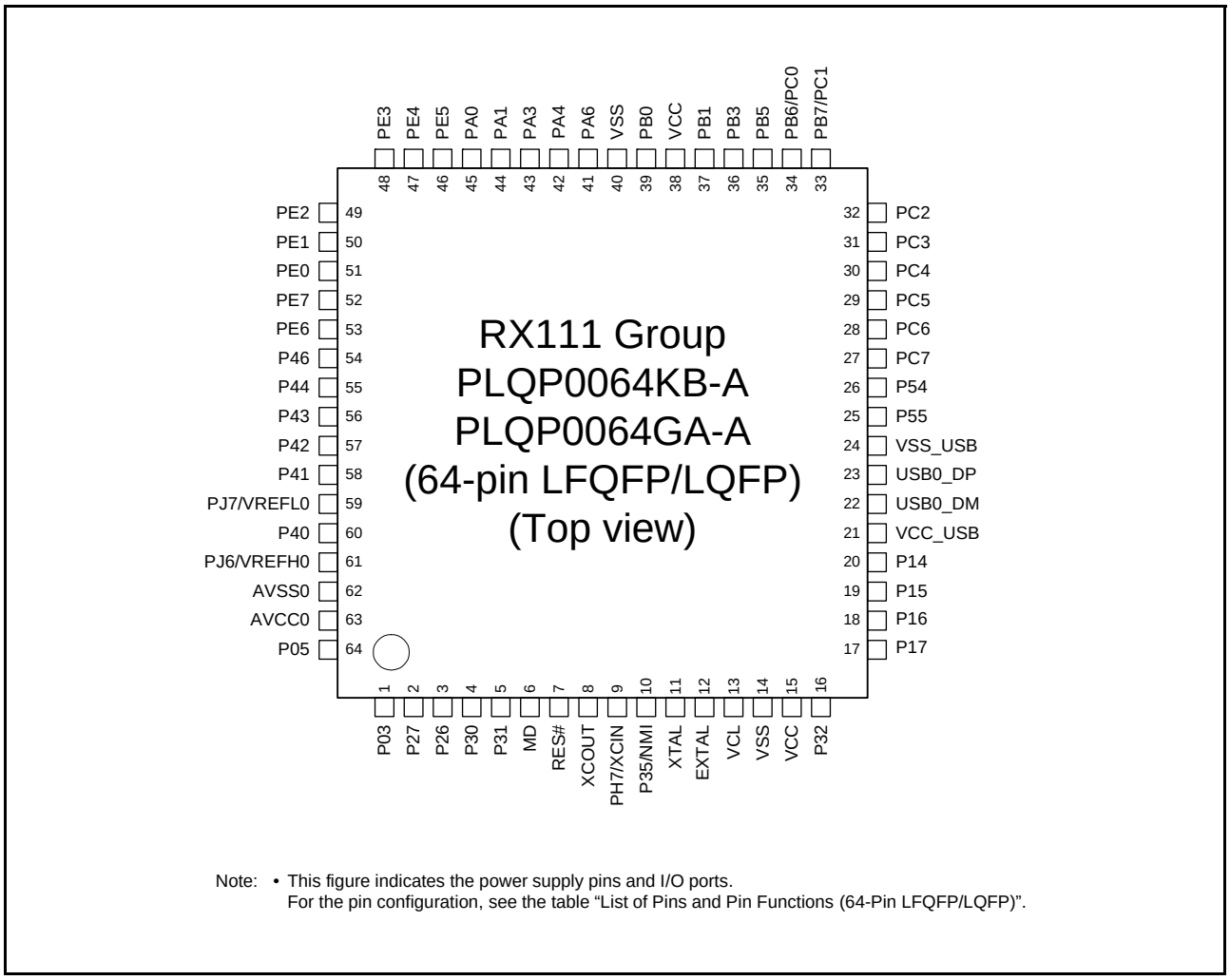
Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VCC_USB	Input	Power supply pin for USB. Connect this pin to VCC.
	VSS_USB	Input	Ground pin for USB. Connect this pin to VSS.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC when not using the 12-bit A/D converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS when not using the 12-bit A/D converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC when not using the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS when not using the 12-bit A/D converter.
Clock	XTAL	Output/ Input *1	Pins for connecting a crystal. An external clock can be input through the XTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
	UB#	Input	Pin used for boot mode (USB interface).
	UPSEL	Input	Pin used for boot mode (USB interface).
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
LVD	CMPA2	Input	Detection target voltage pin for voltage detection 2
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.

Table 1.4 Pin Functions (2/3)

Classifications	Pin Name	I/O	Description
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
Serial communications interface (SCIe)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5	I/O	Input/output pins for the clock.
	RXD1, RXD5	Input	Input pins for received data.
	TXD1, TXD5	Output	Output pins for transmitted data.
	CTS1#, CTS5#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#	Output	Output pins for controlling the start of transmission and reception.
Serial communications interface (SCIe)	• Simple I^2C mode		
	SSCL1, SSCL5	I/O	Input/output pins for the I^2C clock.
	SSDA1, SSDA5	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK1, SCK5	I/O	Input/output pins for the clock.
	SMISO1, SMISO5	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5	I/O	Input/output pins for master transmit data.
	SS1#, SS5#	Input	Chip-select input pins.
Serial communications interface (SCIf)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock.
	SSDA12	I/O	Input/output pin for the I^2C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Chip-select input pin.
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCIf.
	TXDX12	Output	Output pin for data transmission by SCIf.
	SIOX12	I/O	Input/output pin for data reception or transmission by SCIf.
I^2C bus interface	SCL0	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.

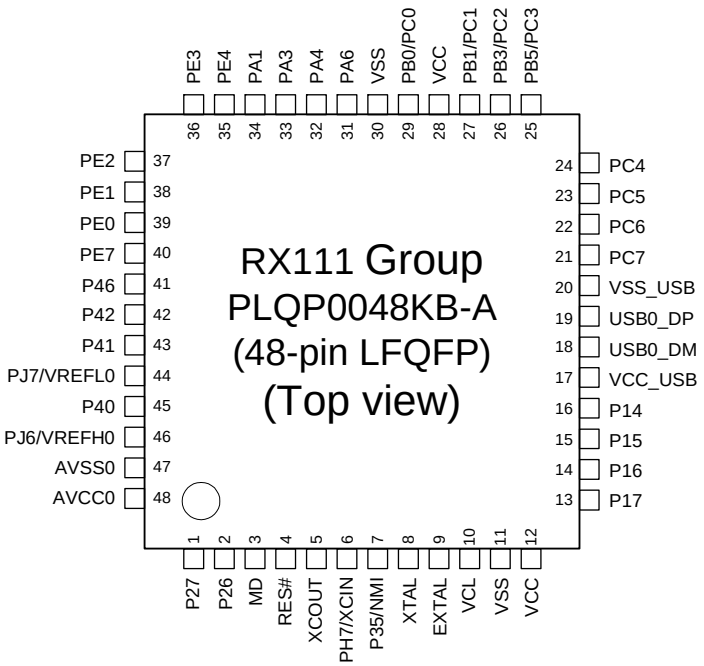
1.5 Pin Assignments

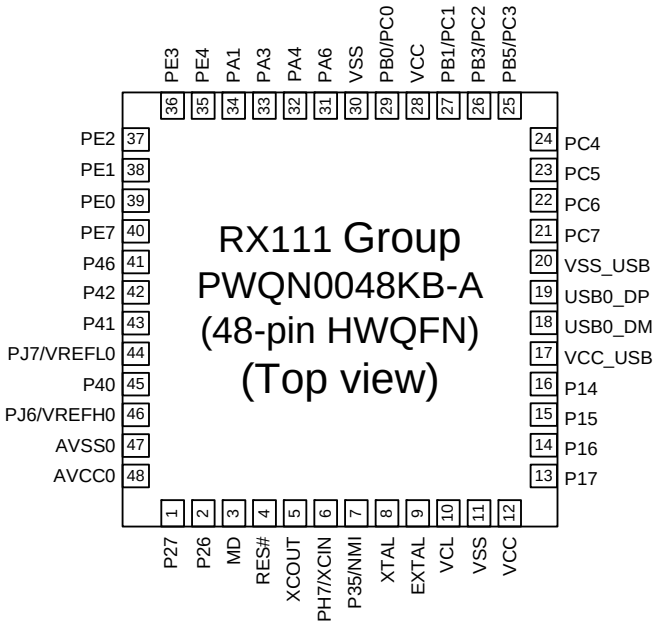
Figure 1.3 to Figure 1.7 show the pin assignments. Table 1.5 to Table 1.9 show the lists of pins and pin functions.



Note: • This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LFQFP/LQFP)”.

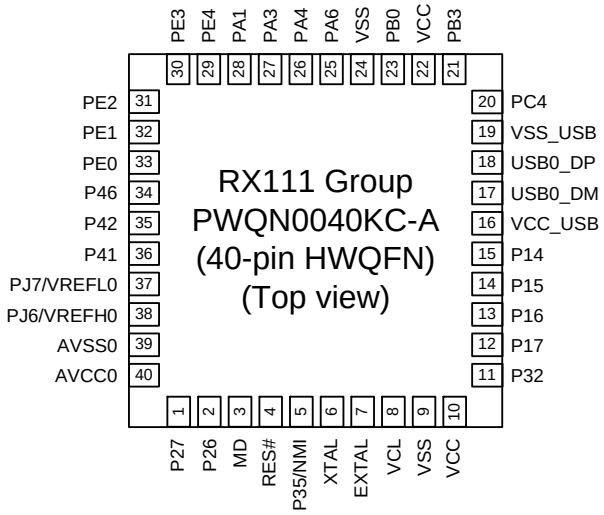
Figure 1.3 Pin Assignments of the 64-Pin LFQFP/LQFP





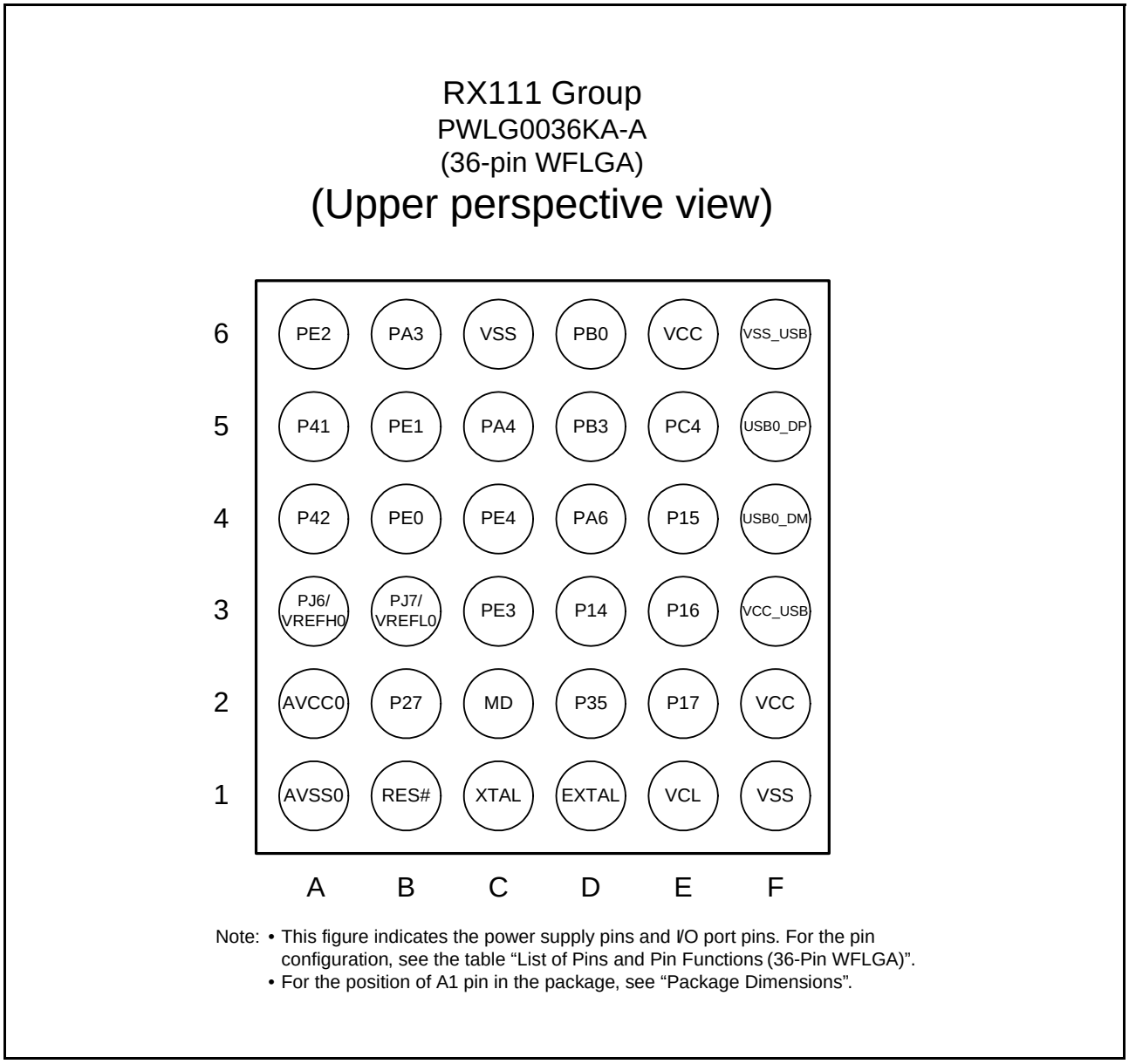
Note: • This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/HWQFN)”.
Note: • It is recommended that the exposed die pad of HWQFN should be connected to VSS.

Figure 1.5 Pin Assignments of the 48-Pin LFQFP/HWQFN



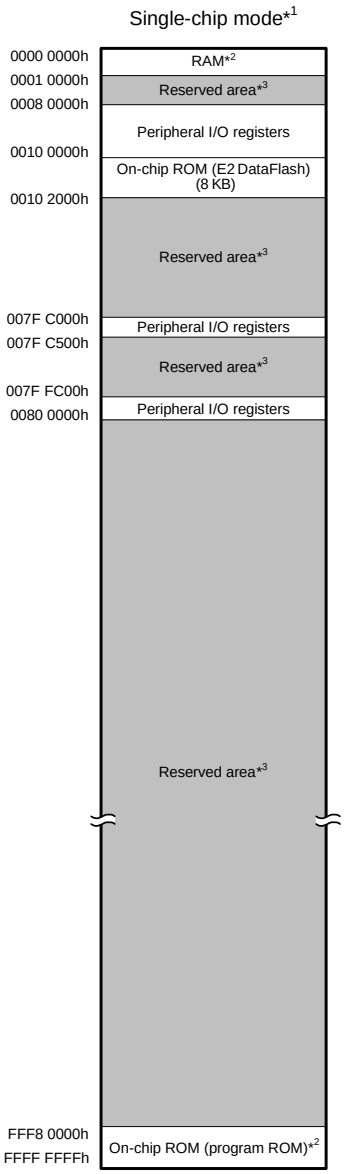
Note: • This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (40-Pin HWQFN)”.
Note: • It is recommended that the exposed die pad of HWQFN should be connected to VSS.

Figure 1.6 Pin Assignments of the 40-Pin HWQFN



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (36-Pin WFLGA)”.
• For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.7 Pin Assignments of the 36-Pin WFLGA



Note 1. The address space in boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
512 K	FFF8 0000h to FFFF FFFFh	64 K	0000 0000h to 0000 FFFFh
384 K	FFFA 0000h to FFFF FFFFh		
256 K	FFFC 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh
128 K	FFFE 0000h to FFFF FFFFh		
96 K	FFFE 8000h to FFFF FFFFh	16 K	0000 0000h to 0000 3FFFh
64 K	FFFF 0000h to FFFF FFFFh		
32 K	FFFF 8000h to FFFF FFFFh	10 K	0000 0000h to 0000 27FFh
16 K	FFFF C000h to FFFF FFFFh	8 K	0000 0000h to 0000 1FFFh

Note:See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map

Table 4.1 List of I/O Registers (Address Order) (11/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2 or 3 PCLKB
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2 or 3 PCLKB
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2 or 3 PCLKB
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2 or 3 PCLKB
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 B309h	SCI12	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 B30Ah	SCI12	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 B30Bh	SCI12	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 B30Ch	SCI12	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 B320h	SCI12	Extended Serial Mode Enable Register	ESMER	8	8	2 or 3 PCLKB
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 or 3 PCLKB
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 or 3 PCLKB
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 or 3 PCLKB
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 or 3 PCLKB
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 or 3 PCLKB
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 or 3 PCLKB
0008 B327h	SCI12	Status Register	STR	8	8	2 or 3 PCLKB
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 or 3 PCLKB
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 or 3 PCLKB
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 or 3 PCLKB
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 or 3 PCLKB
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 or 3 PCLKB
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 or 3 PCLKB
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 or 3 PCLKB
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 or 3 PCLKB
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 or 3 PCLKB
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 or 3 PCLKB
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2 or 3 PCLKB
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (12/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C032h	PORTJ	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C051h	PORTH	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C052h	PORTJ	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C064h	PORT4	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C071h	PORTH	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (16/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
000A 0098h	USB0	PIPE3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more
000A 009Ah	USB0	PIPE3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more
000A 009Ch	USB0	PIPE4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more
000A 009Eh	USB0	PIPE4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more
000A 00A0h	USB0	PIPE5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more
000A 00A2h	USB0	PIPE5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more
000A 00B0h	USB0	BC Control Register 0	USBBCCTRL0	16	16	9 PCLKB or more
000A 00CCh	USB0	USB Module Control Register	USBMC	16	16	9 PCLKB or more
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more
007F C090h	FLASH	E2 DataFlash Control Register	DFLCTL	8	8	2 or 3 FCLK
007F C0ACh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRL	8	8	1 or 2 PCLKB
007F C0ADh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRH	8	8	1 or 2 PCLKB
007F C0B0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 FCLK
007F C0B2h	FLASH	Flash Access Window Start Address Monitor	FAWSMR	16	16	2 or 3 FCLK
007F C0B4h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK
007F C0B6h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK
007F C0B7h	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK
007F C0B8h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK
007F C0BAh	FLASH	Flash Error Address Monitor Register H	FEAMH	8	8	2 or 3 FCLK
007F C0C0h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 FCLK
007F C0C1h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 FCLK
007F C0C2h	FLASH	Flash Read Buffer Register L	FRBL	16	16	2 or 3 FCLK
007F C0C4h	FLASH	Flash Read Buffer Register H	FRBH	16	16	2 or 3 FCLK
007F FF80h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK
007F FF81h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK
007F FF82h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK
007F FF84h	FLASH	Flash Processing Start Address Register H	FSARH	8	8	2 or 3 FCLK
007F FF85h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK
007F FF86h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK
007F FF88h	FLASH	Flash Processing End Address Register H	FEARH	8	8	2 or 3 FCLK
007F FF89h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK
007F FF8Ah	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 FCLK
007F FF8Bh	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK
007F FF8Ch	FLASH	Flash Write Buffer Register L	FWBL	16	16	2 or 3 FCLK
007F FF8Eh	FLASH	Flash Write Buffer Register H	FWBH	16	16	2 or 3 FCLK
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 or 3 FCLK

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCNTL register. Table 27.6 lists register allocation for 16-bit access in the User's Manual: Hardware.

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.7 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

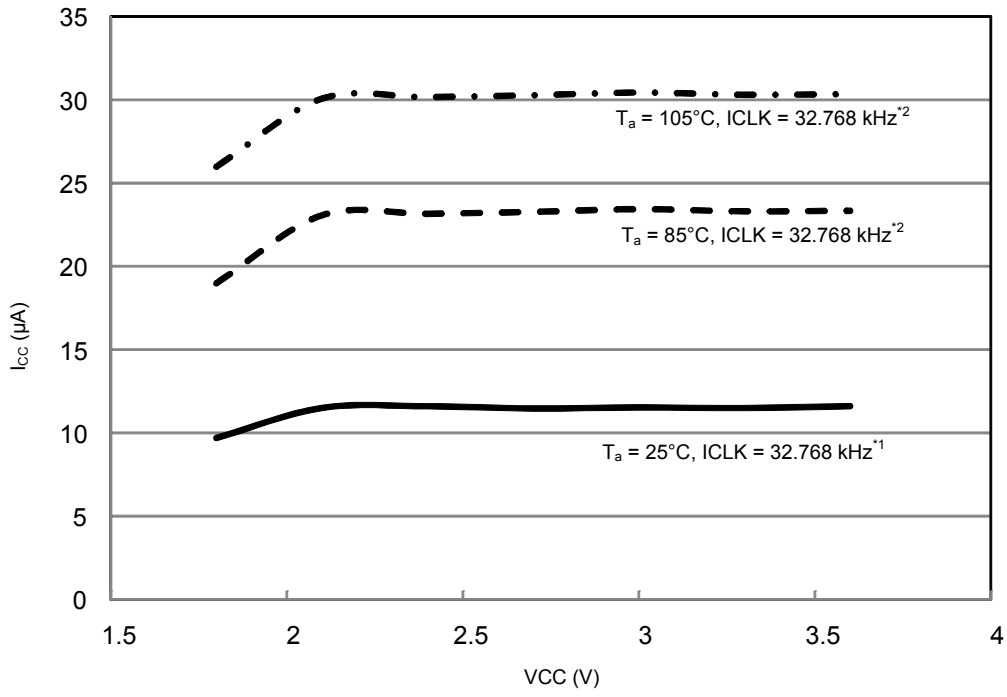
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports P16, P17, port PA6, port PB0 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports P03, P05, ports P14,P15, ports P26, P27, ports P30 to P32, P35, ports P54, P55, ports PA0, PA1, PA3, PA4, ports PB1, PB3, PB5 to PB7, ports PC2 to PC7, ports PE0 to PE7, port PH7, RES#		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Other than RIIC input pin		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Other than RIIC input pin		VCC × 0.1	—	—		
Input voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	XTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	Ports P40 to P44, P46, ports PJ6, PJ7		AVCC0 × 0.7	—	AVCC0 + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	XTAL (external clock input)		–0.3	—	VCC × 0.2		
	Ports P40 to P44, P46, ports PJ6, PJ7		–0.3	—	AVCC0 × 0.3		
	RIIC input pin (SMBus)		–0.3	—	0.8		

[128-Kbyte or less flash memory]

Table 5.7 DC Characteristics (5) (1/2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz	I_{CC}	3.2	—	mA	
				ICLK = 16 MHz		2.2	—		
				ICLK = 8 MHz		1.7	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		10.6	—		
				ICLK = 16 MHz		6.1	—		
				ICLK = 8 MHz		3.7	—		
			All peripheral operation: Max.*3	ICLK = 32 MHz		—	24		
		Sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.8	—		
				ICLK = 16 MHz		1.4	—		
				ICLK = 8 MHz		1.1	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		6.4	—		
				ICLK = 16 MHz		3.7	—		
				ICLK = 8 MHz		2.4	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.2	—		
				ICLK = 16 MHz		1.0	—		
				ICLK = 8 MHz		0.90	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		4.6	—		
				ICLK = 16 MHz		2.8	—		
				ICLK = 8 MHz		1.8	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I_{CC}	2.0	—	mA	
				ICLK = 8 MHz		1.3	—		
				ICLK = 1 MHz		0.75	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		4.9	—		
				ICLK = 8 MHz		3.5	—		
				ICLK = 1 MHz		1.2	—		
			All peripheral operation: Max.*7	ICLK = 12 MHz		—	11		
		Sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.4	—		
				ICLK = 8 MHz		0.85	—		
				ICLK = 1 MHz		0.65	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		3.2	—		
				ICLK = 8 MHz		2.2	—		
				ICLK = 1 MHz		1.0	—		
		Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.2	—		
				ICLK = 8 MHz		0.70	—		
				ICLK = 1 MHz		0.60	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		2.5	—		
				ICLK = 8 MHz		1.8	—		
				ICLK = 1 MHz		0.90	—		
		Increase during flash rewrite*5				2.5	—		



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

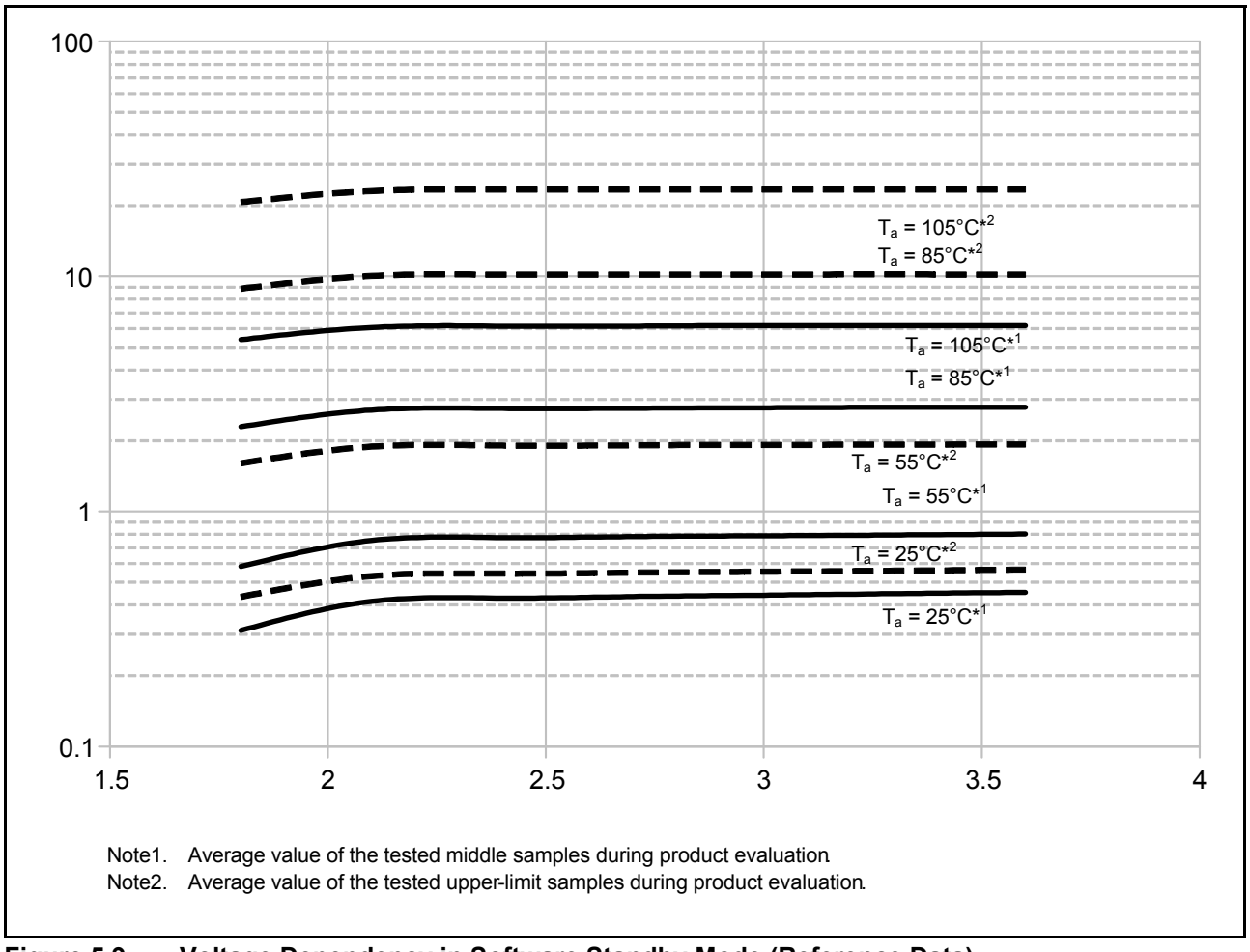
[256-Kbyte or more flash memory]

Table 5.10 DC Characteristics (8)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.44	0.98	µA	
		T_a = 55°C		0.80	3.47		
		T_a = 85°C		2.7	12.0		
		T_a = 105°C		6.17	42.7		
	Increment for RTC operation*4			0.31	—		RCR3.RTCDV[2:0] = 010b
				1.09	—		RCR3.RTCDV[2:0] = 100b
	Increment for IWDT operation			0.37	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.



Note1. Average value of the tested middle samples during product evaluation.
Note2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.9 Voltage Dependency in Software Standby Mode (Reference Data)

Table 5.17 Permissible Output Currents (1)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
T_a = –40 to +85°C (D version)

Item		Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7	I_{OL}	0.4	mA
	Ports other than above		8.0	
Permissible output low current (maximum value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7		0.4	
	Ports other than above		8.0	
Permissible output low current	Total of ports P40 to P44, P46, ports PJ6, PJ7	ΣI_{OL}	2.4	
	Total of ports P03, P05, ports P26, P27, ports P30, P31		30	
	Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7		30	
	Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7		30	
	Total of all output pins		60	
Permissible output high current (average value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7	I_{OH}	–0.1	
	Ports other than above		–4.0	
Permissible output high current (maximum value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7		–0.1	
	Ports other than above		–4.0	
Permissible output high current	Total of ports P40 to P44, P46, ports PJ6, PJ7	ΣI_{OH}	–0.6	
	Total of ports P03, P05, ports P26, P27, ports P30, P31		–10	
	Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7		–15	
	Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7		–15	
	Total of all output pins		–40	

Note: Do not exceed the permissible total supply current.

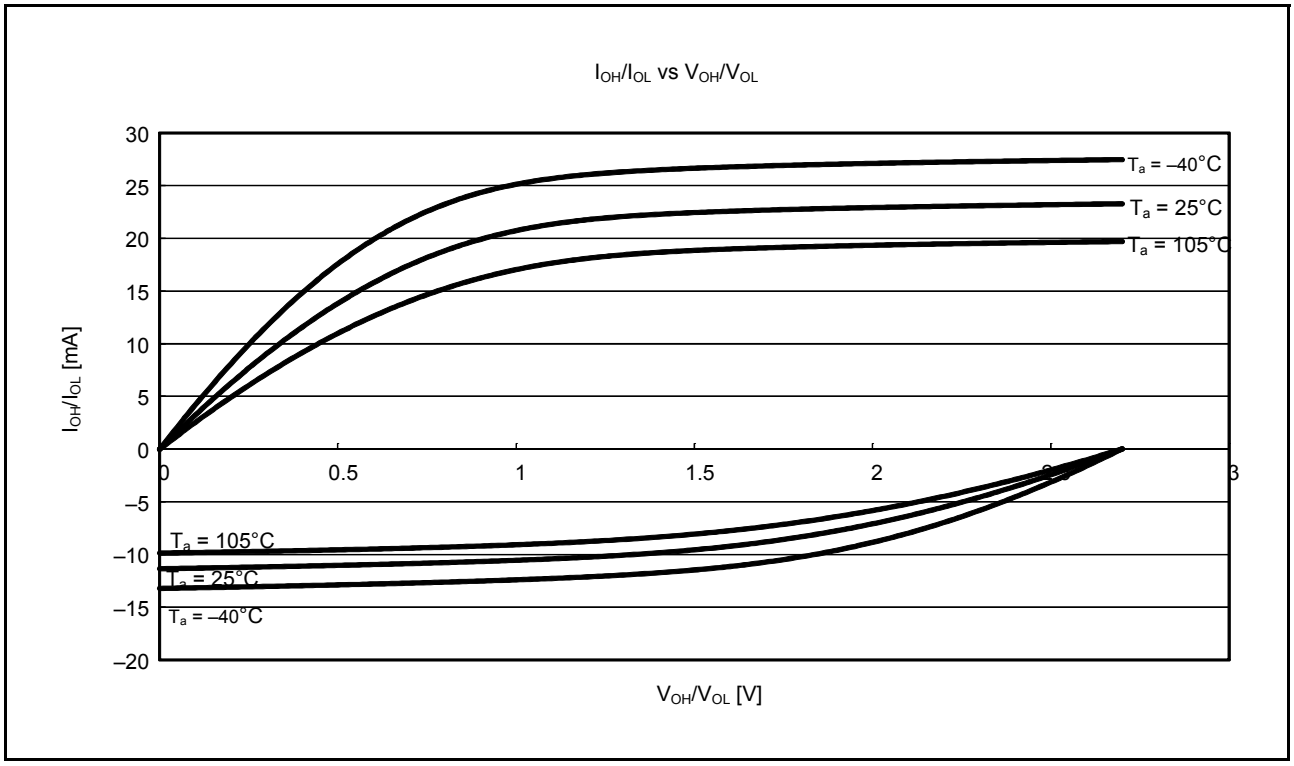


Figure 5.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of General Ports (Except for the RIIC Output Pin, Ports P40 to P44, P46, Ports PJ6, PJ7) at VCC = 2.7 V (Reference Data)

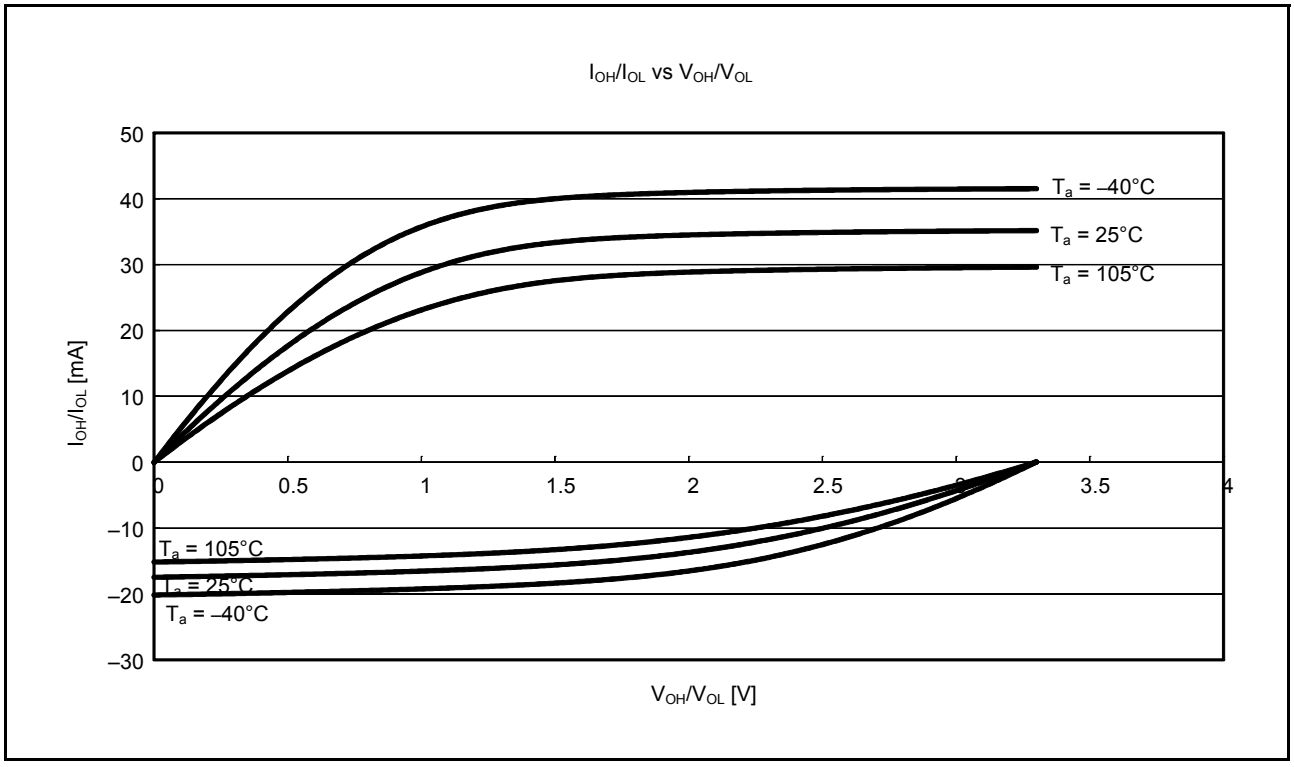


Figure 5.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of General Ports (Except for the RIIC Output Pin, Ports P40 to P44, P46, Ports PJ6, PJ7) at VCC = 3.3 V (Reference Data)

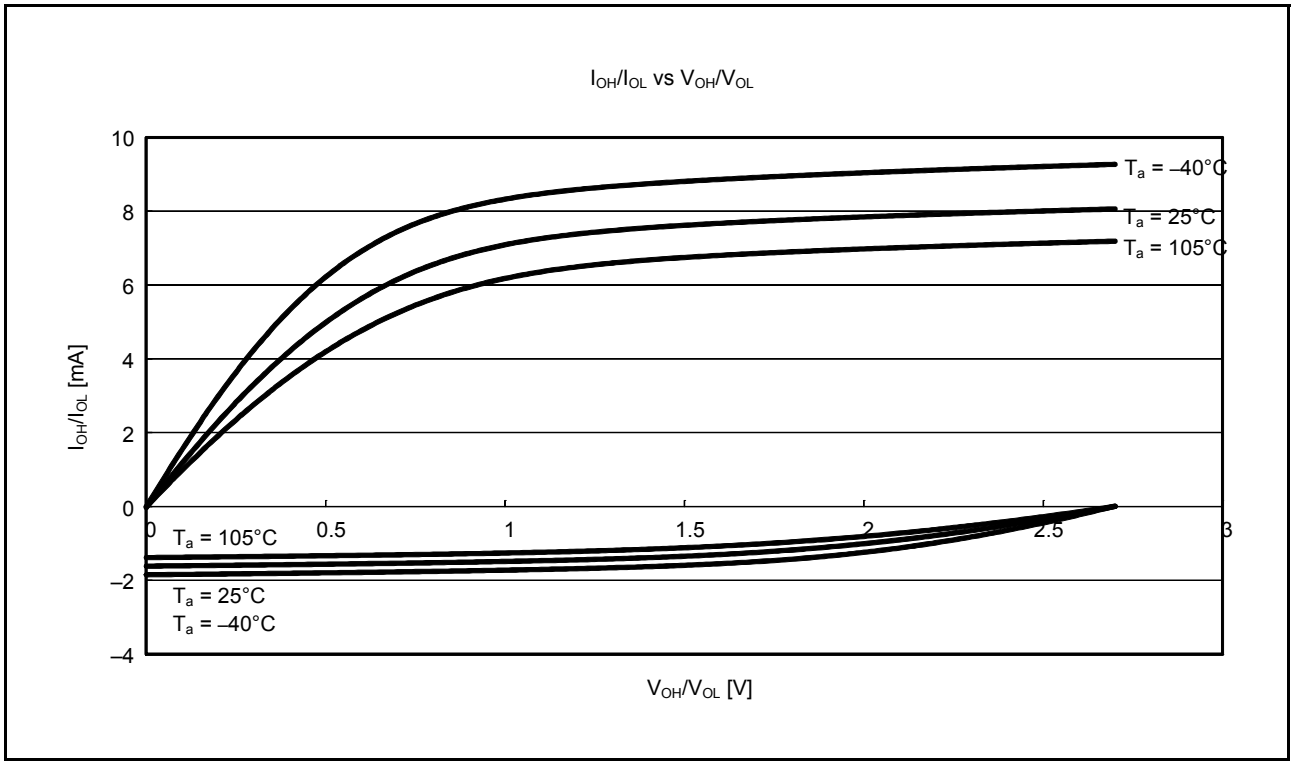


Figure 5.21 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Ports P40 to P44, P46, Ports PJ6, PJ7 at VCC = 2.7 V (Reference Data)

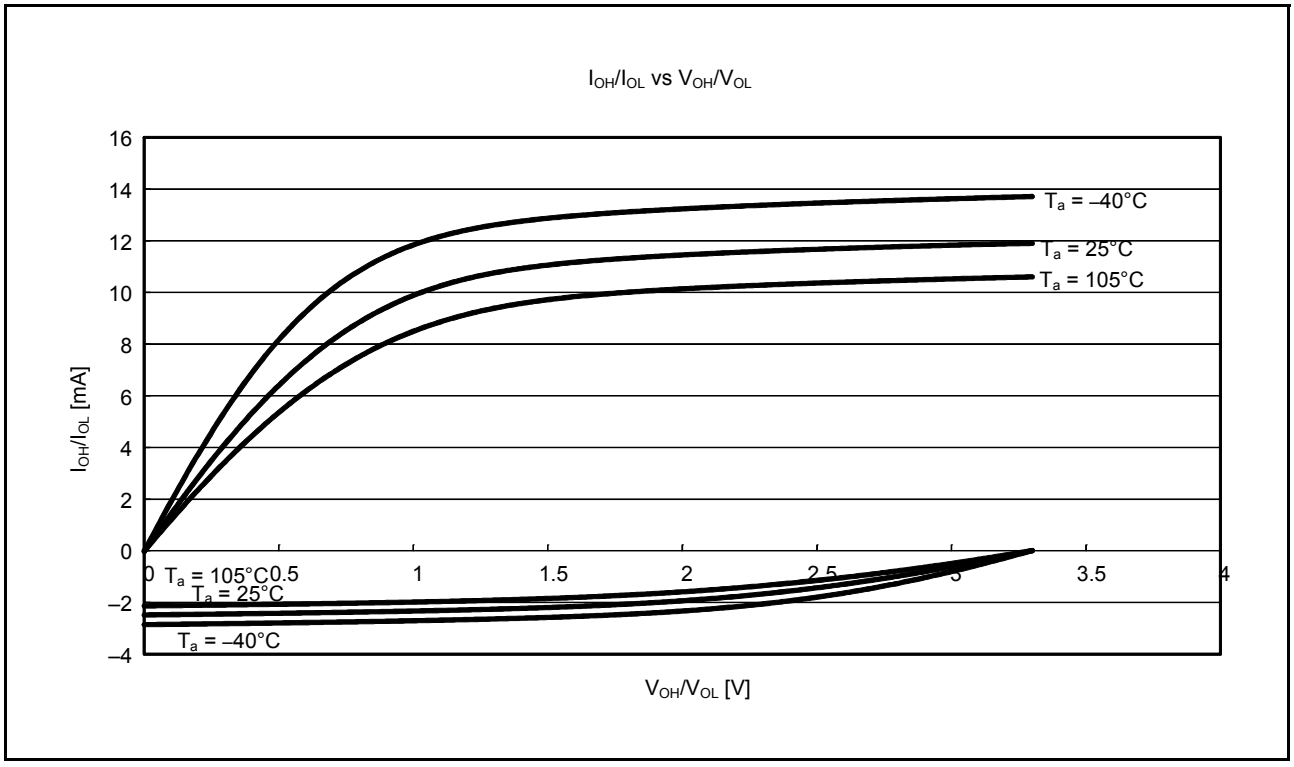


Figure 5.22 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Ports P40 to P44, P46, Ports PJ6, PJ7 at VCC = 3.3 V (Reference Data)

Table 5.35 Timing of On-Chip Peripheral Modules (4)

Conditions: 2.7 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.7 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, fPCLKB ≤ 32 MHz, T_a = –40 to +105°C

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL0 input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 5.53
	SCL0 input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL0 input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL0, SDA0 input rise time	t_{Sr}	—	1000	ns	
	SCL0, SDA0 input fall time	t_{Sf}	—	300	ns	
	SCL0, SDA0 input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA0 input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL0, SDA0 capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL0 input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 5.53
	SCL0 input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL0 input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL0, SDA0 input rise time	t_{Sr}	—*2	300	ns	
	SCL0, SDA0 input fall time	t_{Sf}	—*2	300	ns	
	SCL0, SDA0 input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA0 input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL0, SDA0 capacitive load	C_b	—	400	pF	

Note: • t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. The minimum tsr and tsf specifications for fast mode are not set.

5.8 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.45 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 5.58, Figure 5.59
	Voltage detection circuit (LVD1)*1	V_{det1_4}	3.00	3.10	3.20	V	Figure 5.60 At falling edge VCC
		V_{det1_5}	2.91	3.00	3.09		
		V_{det1_6}	2.81	2.90	2.99		
		V_{det1_7}	2.70	2.79	2.88		
		V_{det1_8}	2.60	2.68	2.76		
		V_{det1_9}	2.50	2.58	2.66		
		V_{det1_A}	2.40	2.48	2.56		
		V_{det1_B}	1.99	2.06	2.13		
		V_{det1_C}	1.90	1.96	2.02		
		V_{det1_D}	1.80	1.86	1.92		

Note: • These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Table 5.46 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Voltage detection circuit (LVD2)*1	V_{det2_0}	2.71	2.90	3.09	V	Figure 5.61 At falling edge VCC
		V_{det2_1}	2.43	2.60	2.77		
		V_{det2_2}	1.87	2.00	2.13		
		V_{det2_3}*2	1.69	1.80	1.91		
Wait time after power-on reset cancellation	At normal startup*3	t_{POR}	—	9.1	—	ms	Figure 5.59
	During fast startup time*4	t_{POR}	—	1.6	—		
Wait time after voltage monitoring 1 reset cancellation	Power-on voltage monitoring 1 reset disabled*3	t_{LVD1}	—	568	—	µs	Figure 5.60
	Power-on voltage monitoring 1 reset enabled*4		—	100	—		
Wait time after voltage monitoring 2 reset cancellation		t_{LVD2}	—	100	—	µs	Figure 5.61
Response delay time		t_{det}	—	—	350	µs	Figure 5.58
Minimum VCC down time*5		t_{VOFF}	350	—	—	µs	Figure 5.58, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 5.59, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	300	µs	Figure 5.60, Figure 5.61
Hysteresis width (LVD1 and LVD2)		V_{LVH}	—	70	—	mV	Vdet1_4 selected
			—	60	—		Vdet1_5 to 9, LVD2 selected
			—	50	—		When selection is from among Vdet1_A to B.
			—	40	—		When selection is from among Vdet1_C to D.

Note: • These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.

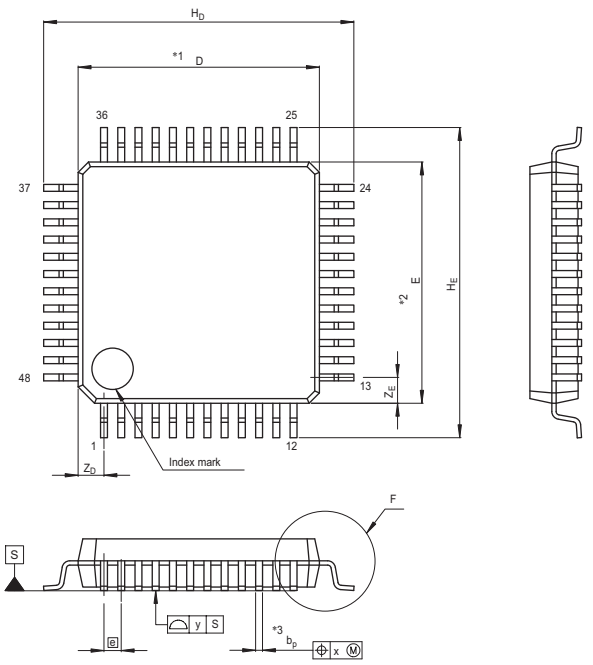
Note 2. Vdet2_3 selection can be used only when the CMPA2 pin input voltage is selected and cannot be used when the power supply voltage (VCC) is selected.

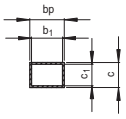
Note 3. When OFS1.(STUPLVD1REN, FASTSTUP) = 11b.

Note 4. When OFS1.(STUPLVD1REN, FASTSTUP) ≠ 11b.

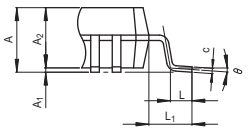
Note 5. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure D 48-Pin LFQFP (PLQP0048KB-A)