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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SCI, SPI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51115adfm-3a

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products (1/2)

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Maximum Operating Frequency	Operating Temperature
RX111	R5F51118AGFM	R5F51118AGFM#3A	PLQP0064KB-A	512 Kbytes	64 Kbytes	8 Kbytes	32 MHz	–40 to +105°C
	R5F51118AGFK	R5F51118AGFK#3A	PLQP0064GA-A					
	R5F51118AGFL	R5F51118AGFL#3A	PLQP0048KB-A					
	R5F51118AGNE	R5F51118AGNE#UA	PWQN0048KB-A					
	R5F51117AGFM	R5F51117AGFM#3A	PLQP0064KB-A	384 Kbytes				
	R5F51117AGFK	R5F51117AGFK#3A	PLQP0064GA-A					
	R5F51117AGFL	R5F51117AGFL#3A	PLQP0048KB-A					
	R5F51117AGNE	R5F51117AGNE#UA	PWQN0048KB-A					
	R5F51116AGFM	R5F51116AGFM#3A	PLQP0064KB-A	256 Kbytes	32 Kbytes			
	R5F51116AGFK	R5F51116AGFK#3A	PLQP0064GA-A					
	R5F51116AGFL	R5F51116AGFL#3A	PLQP0048KB-A					
	R5F51116AGNE	R5F51116AGNE#UA	PWQN0048KB-A					
	R5F51115AGFM	R5F51115AGFM#3A	PLQP0064KB-A	128 Kbytes	16 Kbytes			
	R5F51115AGFK	R5F51115AGFK#3A	PLQP0064GA-A					
	R5F51115AGFL	R5F51115AGFL#3A	PLQP0048KB-A					
	R5F51115AGNE	R5F51115AGNE#UA	PWQN0048KB-A					
	R5F51114AGFM	R5F51114AGFM#3A	PLQP0064KB-A	96 Kbytes				
	R5F51114AGFK	R5F51114AGFK#3A	PLQP0064GA-A					
	R5F51114AGFL	R5F51114AGFL#3A	PLQP0048KB-A					
	R5F51114AGNE	R5F51114AGNE#UA	PWQN0048KB-A					
	R5F51113AGFM	R5F51113AGFM#3A	PLQP0064KB-A	64 Kbytes	10 Kbytes			
	R5F51113AGFK	R5F51113AGFK#3A	PLQP0064GA-A					
	R5F51113AGFL	R5F51113AGFL#3A	PLQP0048KB-A					
	R5F51113AGNE	R5F51113AGNE#UA	PWQN0048KB-A					
	R5F51113AGNF	R5F51113AGNF#UA	PWQN0040KC-A					
	R5F51111AGFM	R5F51111AGFM#3A	PLQP0064KB-A	32 Kbytes				
	R5F51111AGFK	R5F51111AGFK#3A	PLQP0064GA-A					
	R5F51111AGFL	R5F51111AGFL#3A	PLQP0048KB-A					
	R5F51111AGNE	R5F51111AGNE#UA	PWQN0048KB-A					
	R5F51111AGNF	R5F51111AGNF#UA	PWQN0040KC-A					
	R5F5111JAGFM	R5F5111JAGFM#3A	PLQP0064KB-A	16 Kbytes	8 Kbytes			
	R5F5111JAGFK	R5F5111JAGFK#3A	PLQP0064GA-A					
	R5F5111JAGFL	R5F5111JAGFL#3A	PLQP0048KB-A					
	R5F5111JAGNE	R5F5111JAGNE#UA	PWQN0048KB-A					
	R5F5111JAGNF	R5F5111JAGNF#UA	PWQN0040KC-A					

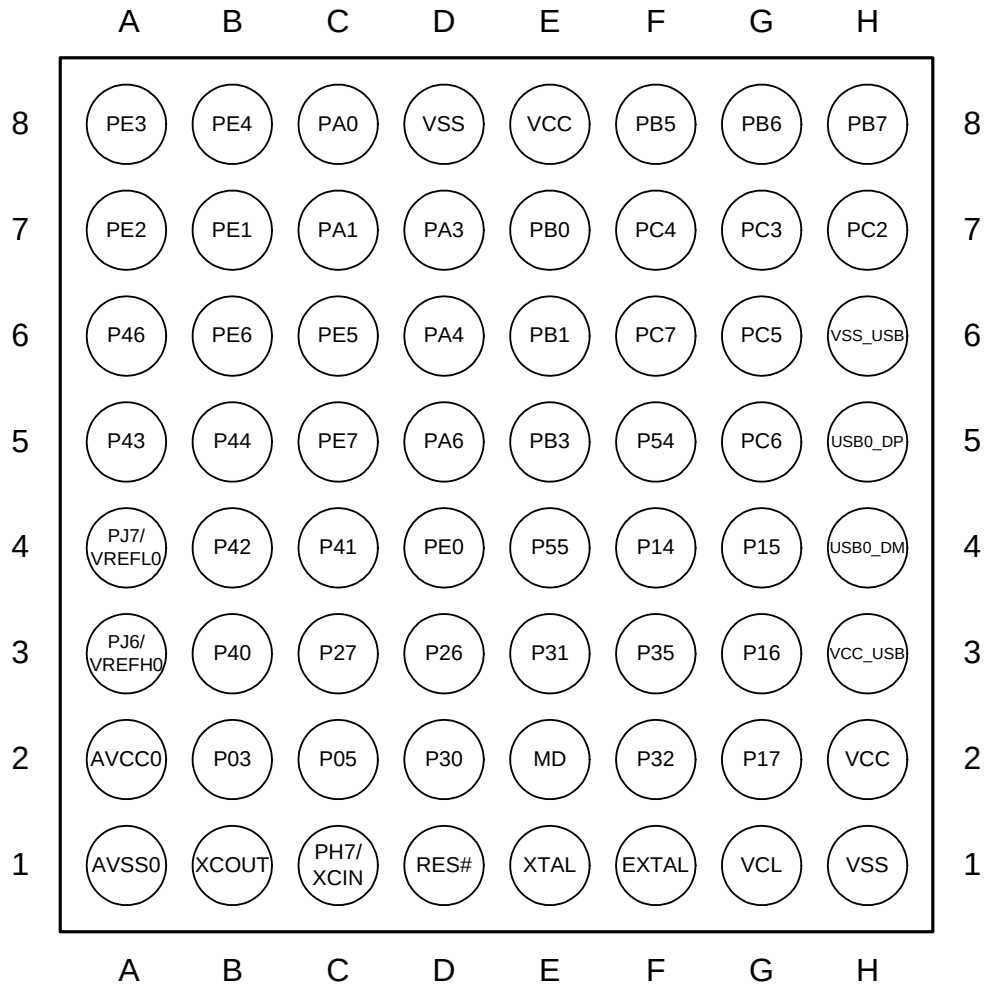
1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VCC_USB	Input	Power supply pin for USB. Connect this pin to VCC.
	VSS_USB	Input	Ground pin for USB. Connect this pin to VSS.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC when not using the 12-bit A/D converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS when not using the 12-bit A/D converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC when not using the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS when not using the 12-bit A/D converter.
Clock	XTAL	Output/ Input *1	Pins for connecting a crystal. An external clock can be input through the XTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
	UB#	Input	Pin used for boot mode (USB interface).
	UPSEL	Input	Pin used for boot mode (USB interface).
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
LVD	CMPA2	Input	Detection target voltage pin for voltage detection 2
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.

RX111 Group
PWLG0064KA-A
(64-pin WFLGA)
(Upper perspective view)



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin WFLGA)”.
• For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.4 Pin Assignments of the 64-Pin WFLGA

Table 4.1 List of I/O Registers (Address Order) (2/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 7026h	ICU	Interrupt Request Register 038	IR038	8	8	2 ICLK
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK
0008 703Fh	ICU	Interrupt Request Register 063	IR063	8	8	2 ICLK
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK
0008 7058h	ICU	Interrupt Request Register 088	IR088	8	8	2 ICLK
0008 7059h	ICU	Interrupt Request Register 089	IR089	8	8	2 ICLK
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8	2 ICLK
0008 705Ch	ICU	Interrupt Request Register 092	IR092	8	8	2 ICLK
0008 705Dh	ICU	Interrupt Request Register 093	IR093	8	8	2 ICLK
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (3/16)

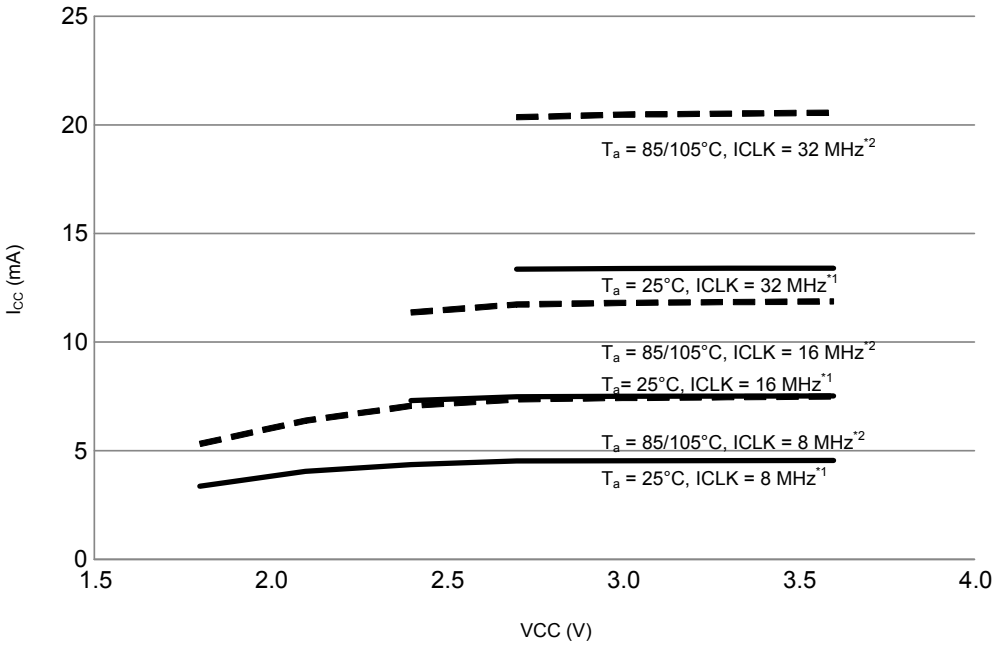
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK
0008 70EEh	ICU	Interrupt Request Register 238	IR238	8	8	2 ICLK
0008 70EFh	ICU	Interrupt Request Register 239	IR239	8	8	2 ICLK
0008 70F0h	ICU	Interrupt Request Register 240	IR240	8	8	2 ICLK
0008 70F1h	ICU	Interrupt Request Register 241	IR241	8	8	2 ICLK
0008 70F2h	ICU	Interrupt Request Register 242	IR242	8	8	2 ICLK
0008 70F3h	ICU	Interrupt Request Register 243	IR243	8	8	2 ICLK
0008 70F4h	ICU	Interrupt Request Register 244	IR244	8	8	2 ICLK
0008 70F5h	ICU	Interrupt Request Register 245	IR245	8	8	2 ICLK
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt Request Register 249	IR249	8	8	2 ICLK
0008 711Bh	ICU	DTC Activation Enable Register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC Activation Enable Register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC Activation Enable Register 029	DTCER029	8	8	2 ICLK
0008 7124h	ICU	DTC Activation Enable Register 036	DTCER036	8	8	2 ICLK
0008 7125h	ICU	DTC Activation Enable Register 037	DTCER037	8	8	2 ICLK
0008 712Dh	ICU	DTC Activation Enable Register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC Activation Enable Register 046	DTCER046	8	8	2 ICLK
0008 7140h	ICU	DTC Activation Enable Register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC Activation Enable Register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC Activation Enable Register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC Activation Enable Register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC Activation Enable Register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC Activation Enable Register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC Activation Enable Register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC Activation Enable Register 071	DTCER071	8	8	2 ICLK
0008 7166h	ICU	DTC Activation Enable Register 102	DTCER102	8	8	2 ICLK
0008 7167h	ICU	DTC Activation Enable Register 103	DTCER103	8	8	2 ICLK
0008 716Ah	ICU	DTC Activation Enable Register 106	DTCER106	8	8	2 ICLK
0008 7172h	ICU	DTC Activation Enable Register 114	DTCER114	8	8	2 ICLK
0008 7173h	ICU	DTC Activation Enable Register 115	DTCER115	8	8	2 ICLK
0008 7174h	ICU	DTC Activation Enable Register 116	DTCER116	8	8	2 ICLK
0008 7175h	ICU	DTC Activation Enable Register 117	DTCER117	8	8	2 ICLK
0008 7179h	ICU	DTC Activation Enable Register 121	DTCER121	8	8	2 ICLK
0008 717Ah	ICU	DTC Activation Enable Register 122	DTCER122	8	8	2 ICLK
0008 717Dh	ICU	DTC Activation Enable Register 125	DTCER125	8	8	2 ICLK
0008 717Eh	ICU	DTC Activation Enable Register 126	DTCER126	8	8	2 ICLK
0008 7181h	ICU	DTC Activation Enable Register 129	DTCER129	8	8	2 ICLK
0008 7182h	ICU	DTC Activation Enable Register 130	DTCER130	8	8	2 ICLK
0008 7183h	ICU	DTC Activation Enable Register 131	DTCER131	8	8	2 ICLK
0008 7184h	ICU	DTC Activation Enable Register 132	DTCER132	8	8	2 ICLK
0008 7186h	ICU	DTC Activation Enable Register 134	DTCER134	8	8	2 ICLK

[256-Kbyte or more flash memory]

Table 5.8 DC Characteristics (6) (1/2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz	I_{CC}	3.6	—	mA	
				ICLK = 16 MHz		2.4	—		
				ICLK = 8 MHz		1.8	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		13.4	—		
				ICLK = 16 MHz		7.5	—		
				ICLK = 8 MHz		4.5	—		
			All peripheral operation: Max.*3	ICLK = 32 MHz		—	27		
		Sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.9	—		
				ICLK = 16 MHz		1.5	—		
				ICLK = 8 MHz		1.3	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		7.6	—		
				ICLK = 16 MHz		4.4	—		
				ICLK = 8 MHz		2.8	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.1	—		
				ICLK = 16 MHz		1.0	—		
				ICLK = 8 MHz		0.9	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		5.8	—		
				ICLK = 16 MHz		3.4	—		
				ICLK = 8 MHz		2.1	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I_{CC}	2.1	—	mA	
				ICLK = 8 MHz		1.4	—		
				ICLK = 1 MHz		0.8	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		5.9	—		
				ICLK = 8 MHz		4.2	—		
				ICLK = 1 MHz		1.3	—		
			All peripheral operation: Max.*7	ICLK = 12 MHz		—	12.2		
		Sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.4	—		
				ICLK = 8 MHz		0.9	—		
				ICLK = 1 MHz		0.7	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		3.6	—		
				ICLK = 8 MHz		2.5	—		
				ICLK = 1 MHz		1.1	—		
		Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.1	—		
				ICLK = 8 MHz		0.6	—		
				ICLK = 1 MHz		0.6	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		2.9	—		
				ICLK = 8 MHz		2.0	—		
				ICLK = 1 MHz		0.9	—		
		Increase during flash rewrite*5				2.5	—		



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.4 Voltage Dependency in High-Speed Operating Mode (Reference Data)

5.2.3 Standard I/O Pin Output Characteristics (3)

Figure 5.19 to Figure 5.22 show the characteristics of ports P40 to P44, P46, ports PJ6, PJ7.

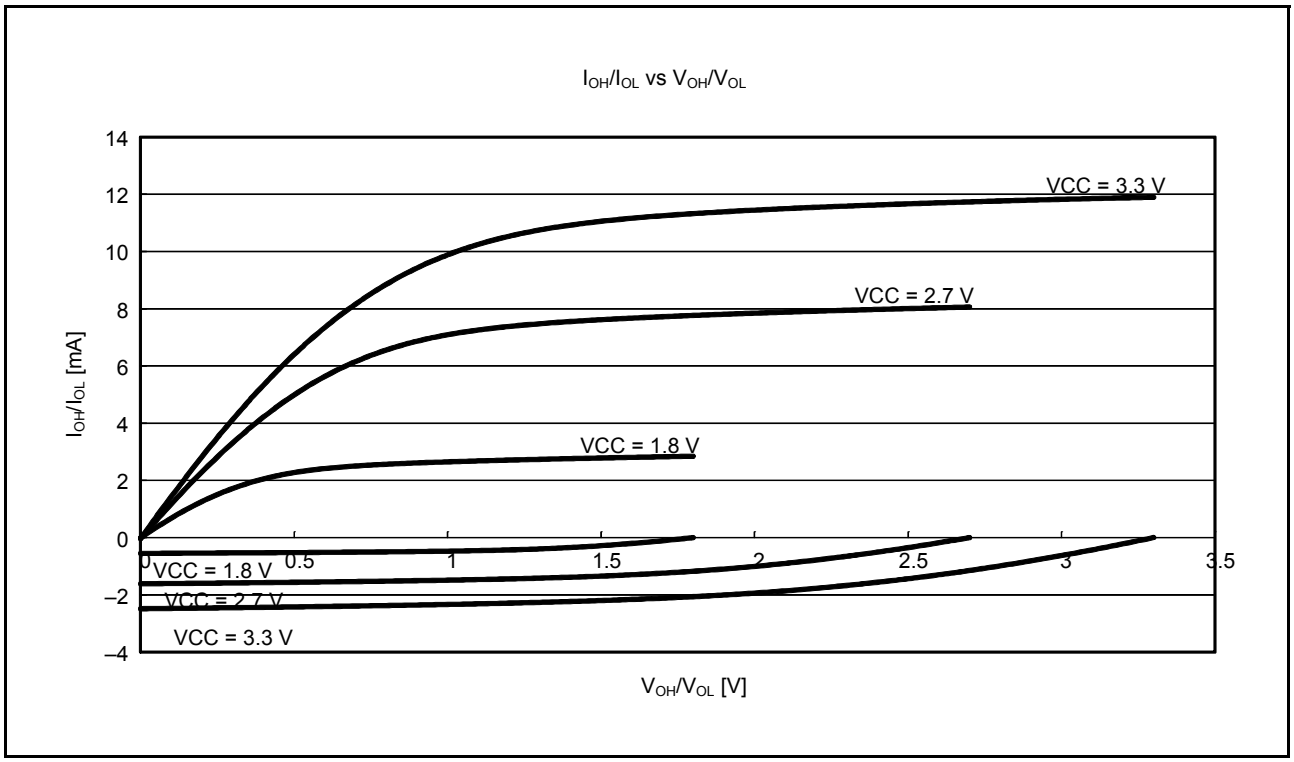


Figure 5.19 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics of Ports P40 to P44, P46, Ports PJ6, PJ7 at T_a = 25°C (Reference Data)

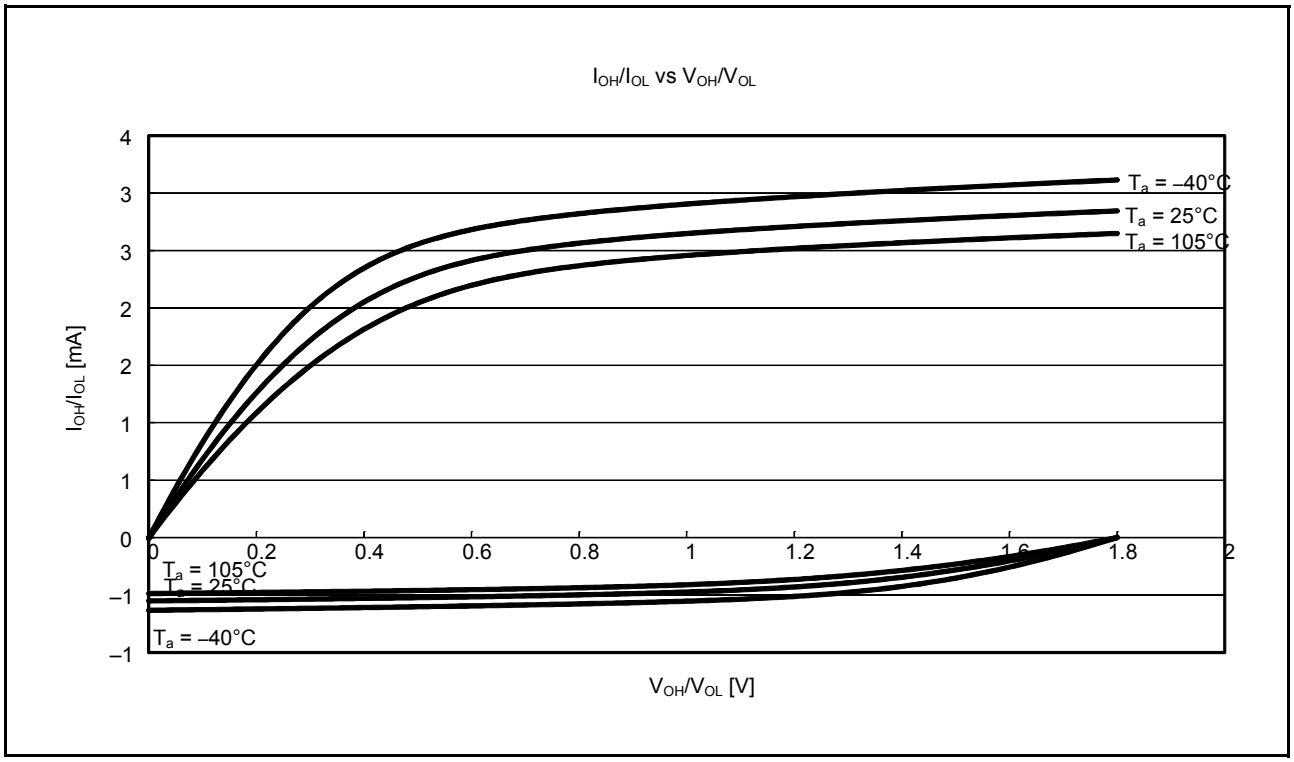


Figure 5.20 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Ports P40 to P44, P46, Ports PJ6, PJ7 at VCC = 1.8 V (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.21 Operation Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC				Unit
			1.8 to 2.4 V	2.4 to 2.7 V	2.7 to 3.6 V	When USB in Use*4	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	16	32	24	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	24	
	Peripheral module clock (PCLKB)		8	16	32	24	
	Peripheral module clock (PCLKD)*3		8	16	32	24	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.
Note 4. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.

Table 5.22 Operation Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC				Unit
			1.8 to 2.4 V	2.4 to 2.7 V	2.7 to 3.6 V	When USB in Use*4	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	12	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	12	
	Peripheral module clock (PCLKB)		8	12	12	12	
	Peripheral module clock (PCLKD)*3		8	12	12	12	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.
Note 4. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.

Table 5.23 Operation Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 to 2.4 V	2.4 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKD)*2		32.768			

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

5.3.4 Control Signal Timing

Table 5.31 Control Signal Timing

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	t_{NMICK} × 3 ≤ 200 ns
		t_{NMICK} × 3.5*2	—	—			t_{NMICK} × 3 > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	t_{IRQCK} × 3 ≤ 200 ns
		t_{IRQCK} × 3.5*3	—	—			t_{IRQCK} × 3 > 200 ns

Note: • 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

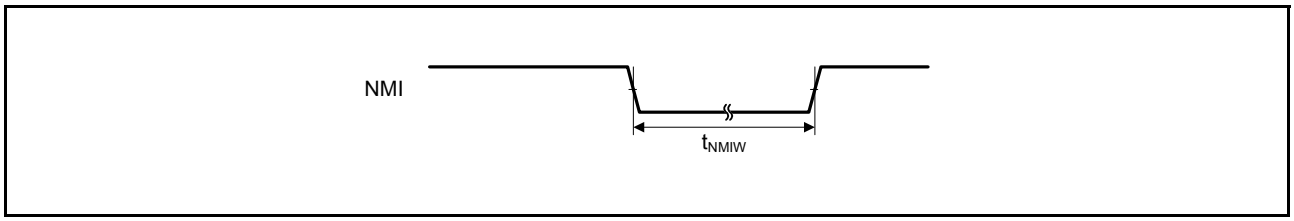


Figure 5.36 NMI Interrupt Input Timing

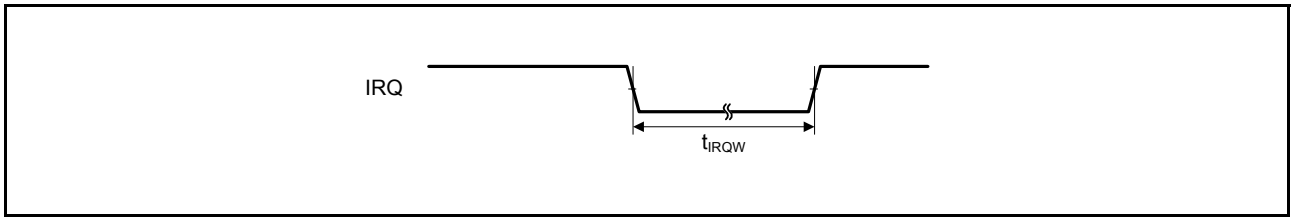


Figure 5.37 IRQ Interrupt Input Timing

Table 5.33 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
T_a = –40 to +105°C, C = 30 pF

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc} *1	Figure 5.46
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.47 to Figure 5.52
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$-30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$-30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			1.8 V or above		—	30		
		Slave	2.7 V or above		—	$3 \times t_{Pcyc} + 65$		
			1.8 V or above		—	$3 \times t_{Pcyc} + 105$		
	Data output hold time	Master	2.7 V or above	t_{OH}	0	—	ns	
			1.8 V or above		–20	—		
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V or above		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	20	ns	
		Input			—	1	µs	
	Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.51, Figure 5.52
			1.8 V or above		—	7		
	Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}	
			1.8 V or above		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

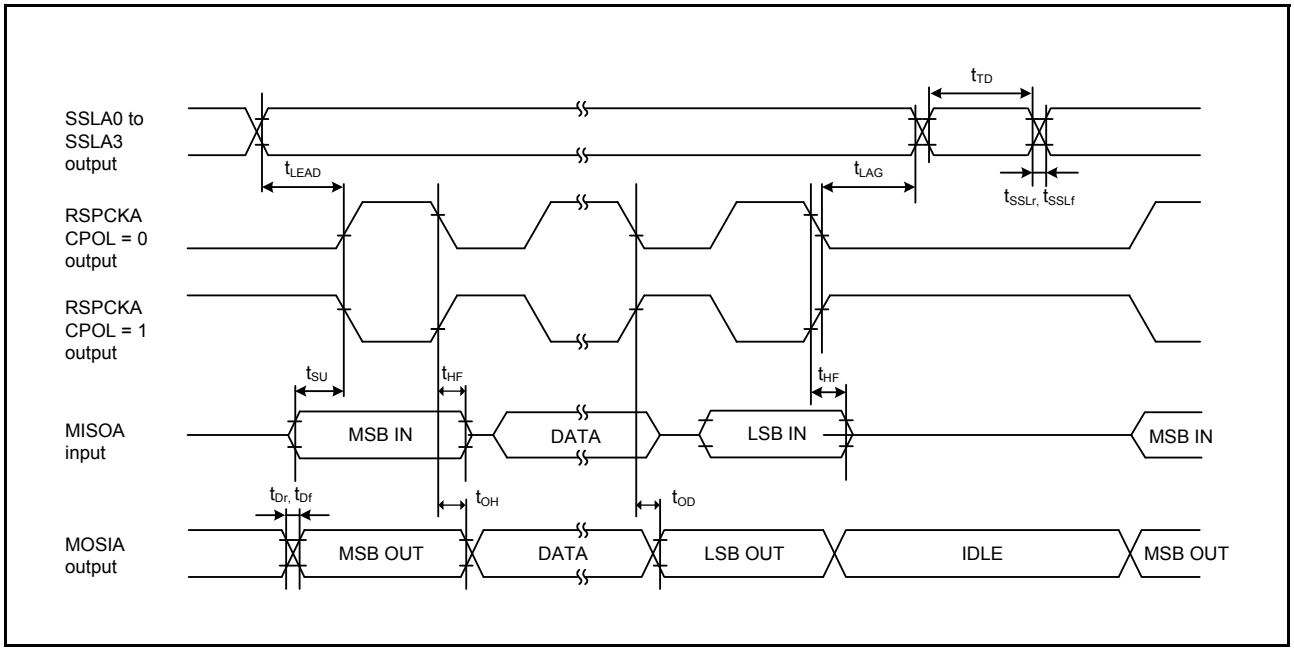


Figure 5.48 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2)

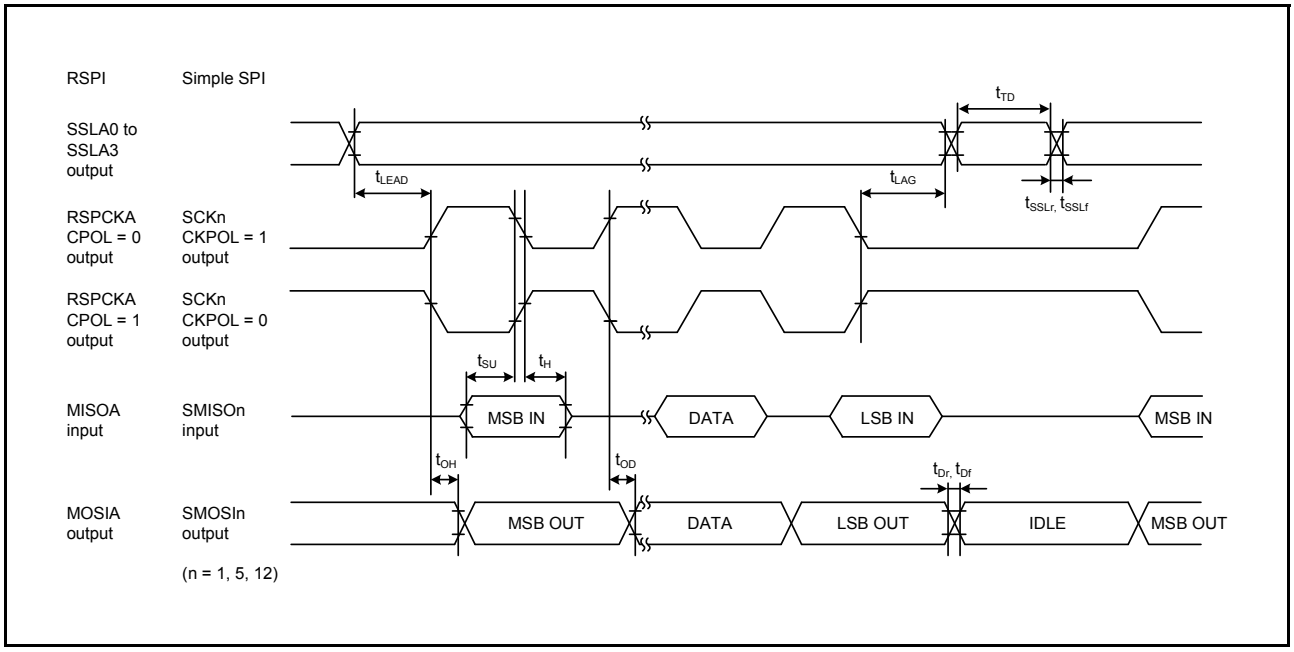


Figure 5.49 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 0)

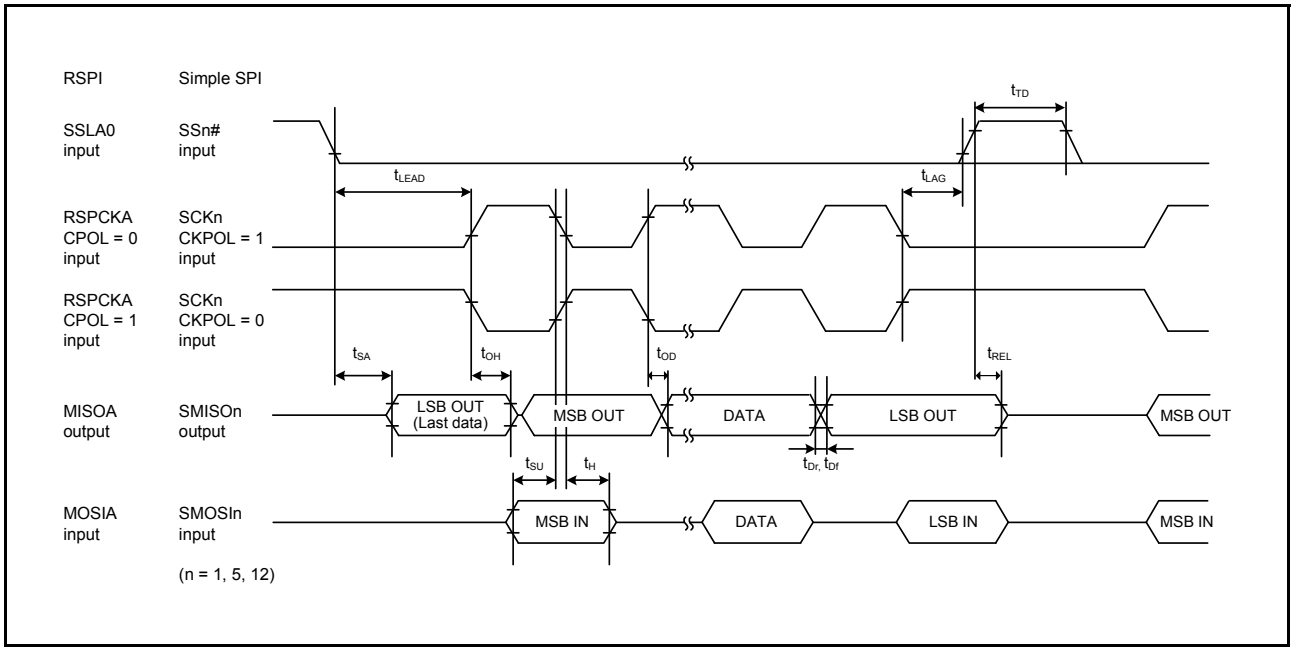
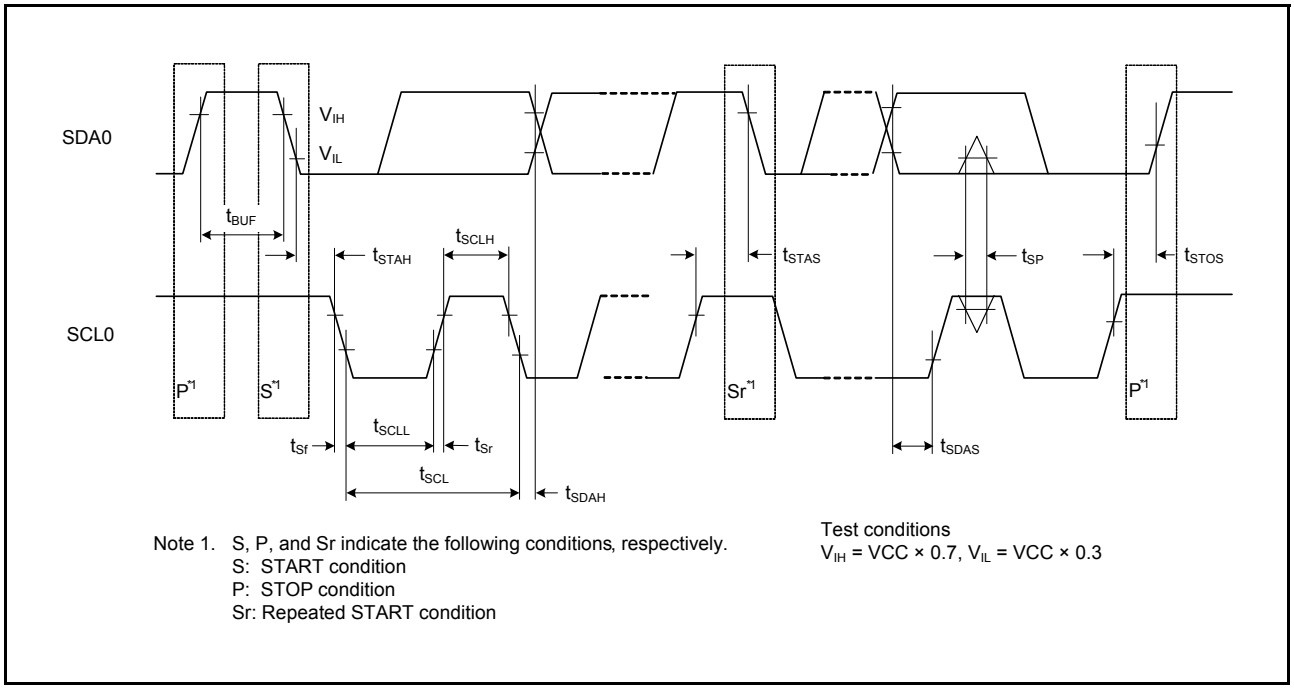


Figure 5.52 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3

Figure 5.53 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

5.5 A/D Conversion Characteristics

Table 5.38 A/D Conversion Characteristics (1)

Conditions: 2.7 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		4	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance (Max.) = 0.3 kΩ	1.031 (0.313)*2	—	—	µs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 09h
		1.375 (0.641)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	High-precision channel PJ6PFS.ASEL bit = 1 PJ7PFS.ASEL bit = 1
				±6.0	LSB	Other than above
Full-scale error		—	±0.75	±4.5	LSB	High-precision channel PJ6PFS.ASEL bit = 1 PJ7PFS.ASEL bit = 1
				±6.0	LSB	Other than above
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel PJ6PFS.ASEL bit = 1 PJ7PFS.ASEL bit = 1
				±8.0	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.39 A/D Conversion Characteristics (2)

Conditions: 2.4 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.4 V ≤ AVCC0 ≤ 3.6 V, 2.4 V ≤ VREFH0 ≤ AVCC0, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		4	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 1.0 kΩ	2.062 (0.625)*2	—	—	µs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 09h
		2.750 (1.313)*2	—	—	µs	Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±6.0	LSB	
Full-scale error		—	±1.25	±6.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.40 A/D Conversion Characteristics (3)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, 1.8 V ≤ VREFH0 ≤ AVCC0, VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5.0 kΩ	4.875 (1.250)*2	—	—	µs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 09h
		6.250 (2.625)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±24.0	LSB	
Full-scale error		—	±1.25	±24.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.75	±32.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.25	±12.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

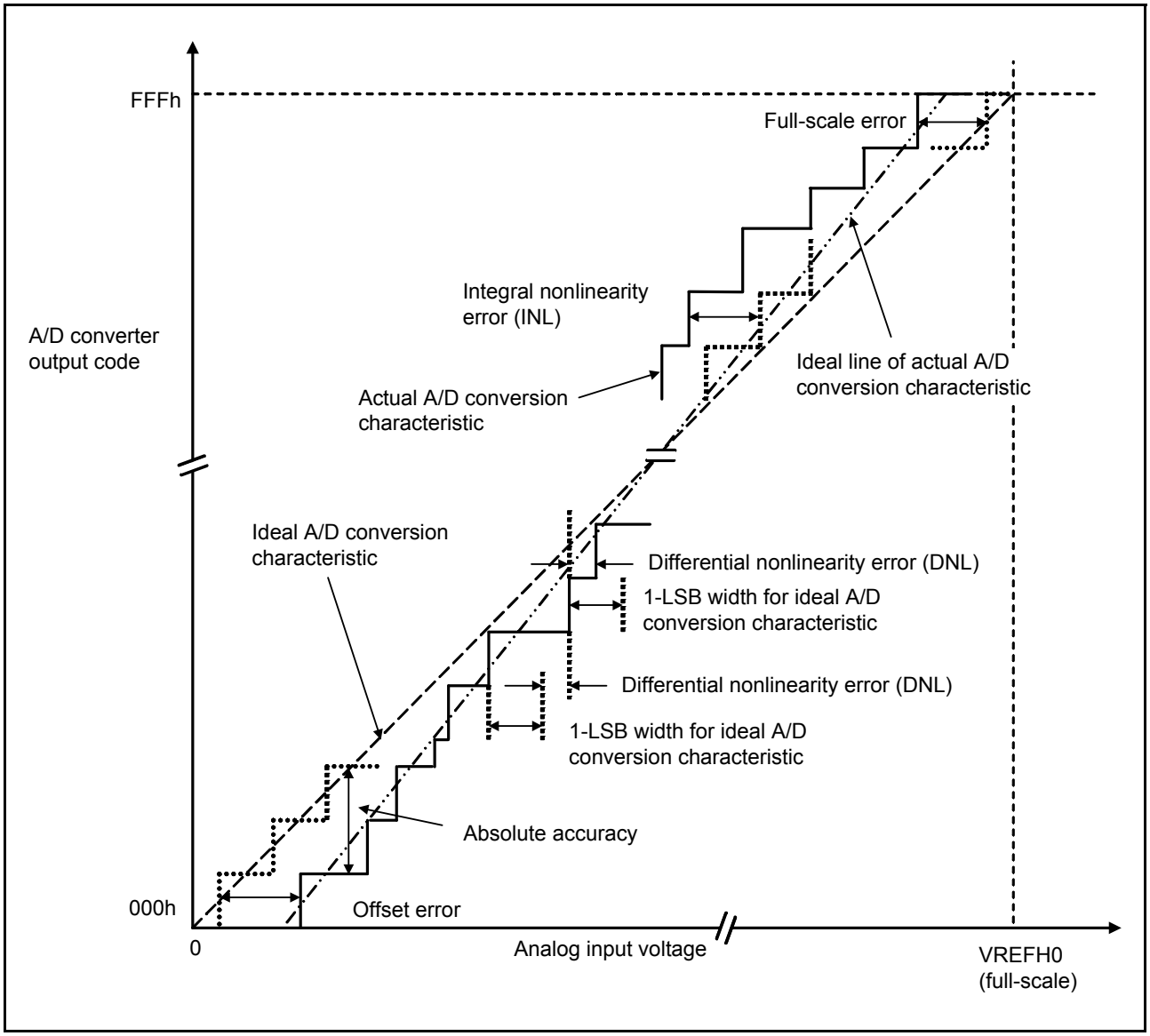


Figure 5.57 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

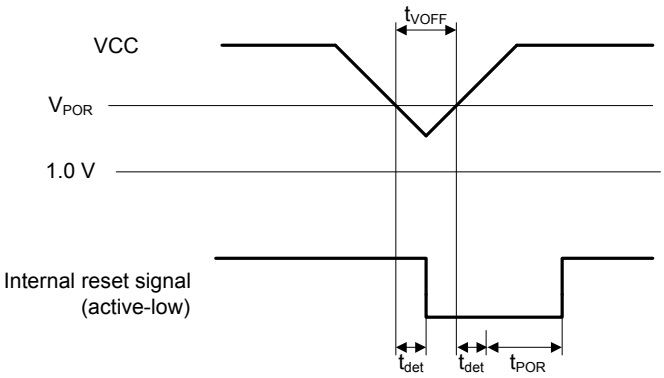
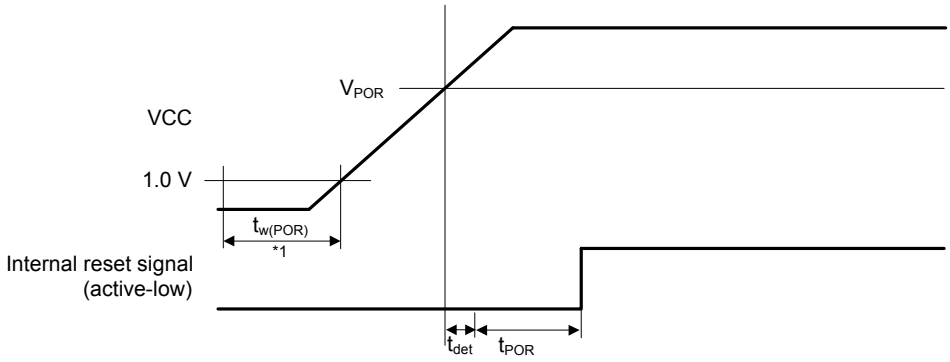


Figure 5.58 Voltage Detection Reset Timing



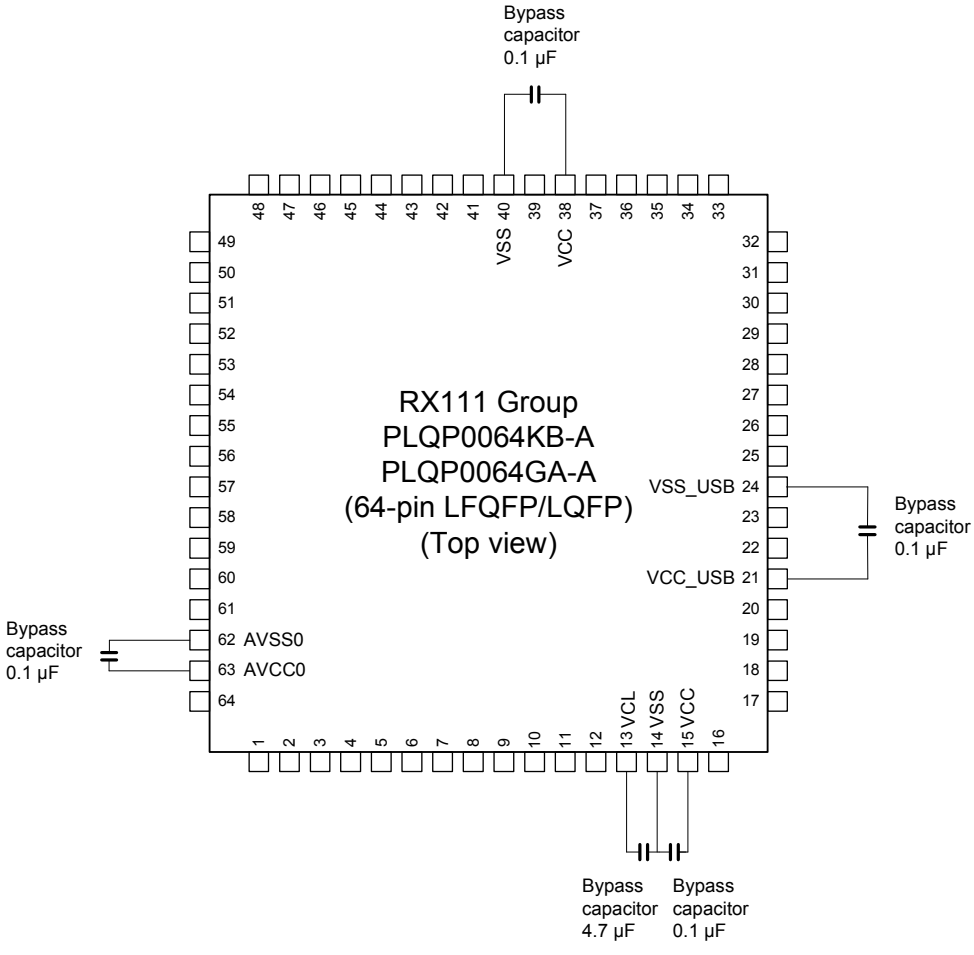
Note 1. $t_{w(por)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(por)}$ for 1.0 ms or more.

Figure 5.59 Power-On Reset Timing

5.12 Usage Notes

5.12.1 Connecting VCL Capacitor and Bypass Capacitors

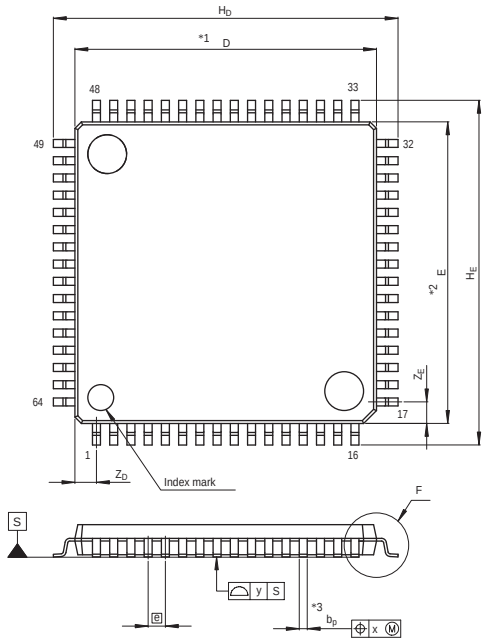
This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU to adjust automatically to the optimum level. A 4.7-µF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and VSS pin. Figure 5.63 to Figure 5.64 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin. Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor to the MCU power supply pins as close as possible. Use a recommended value of 0.1 µF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 30, 12-Bit A/D Converter (S12ADb) in the User's Manual: Hardware.
For notes on designing the printed circuit board, see the descriptions of the application note "Hardware Design Guide" (R01AN1411EJ). The latest version can be downloaded from Renesas Electronics Website.

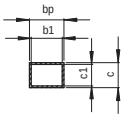


Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

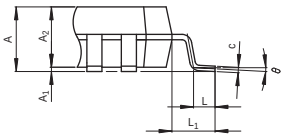
Figure 5.63 Connecting Capacitors (64 Pins)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure B 64-Pin LQFP (PLQP0064GA-A)

REVISION HISTORY	RX111 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.60	Apr 15, 2013	—	First edition, issued
0.90	May 15, 2013	Features	
		1	Changed
		1. Overview	
		2 to 4	Table 1.1 Outline of Specifications changed
		10 to 12	Table 1.4 Pin Functions changed
		13	Figure 1.3 Pin Assignments of the 64-Pin LQFP changed
		14	Figure 1.4 Pin Assignments of the 64-Pin WFLGA changed
		15	Figure 1.5 Pin Assignments of the 48-Pin LQFP/HWQFN changed
		18, 19	Table 1.5 List of Pins and Pin Functions (64-Pin LQFP) changed, Note 1 added
		20, 21	Table 1.6 List of Pins and Pin Functions (64-Pin WFLGA) changed, Note 1 added
		22, 23	Table 1.7 List of Pins and Pin Functions (48-Pin LQFP/HWQFN) changed, Note 1 added
		24, 25	Table 1.8 List of Pins and Pin Functions (40-Pin HWQFN) changed, Note 1 added
		26	Table 1.9 List of Pins and Pin Functions (36-Pin WFLGA) changed, Note 1 added
		4. I/O Registers	
		33 to 48	Table 5.1 List of I/O Registers (Address Order) changed
1.00	Jun 19, 2013	1. Overview	
		9	Figure 1.2 Block Diagram changed
		20, 21	Table 1.6 List of Pins and Pin Functions (64-Pin WFLGA) changed
		26	Table 1.9 List of Pins and Pin Functions (36-Pin WFLGA) changed
		4. I/O Registers	
		33 to 48	Table 4.1 List of I/O Registers (Address Order) changed
		5. Electrical Characteristics	
		49 to 99	Added
1.20	Sep 29, 2014	1. Overview	
		2 to 4	Table 1.1 Outline of Specifications: ROM capacity and RAM capacity changed, Unique ID added
		6, 7	Table 1.3 List of Products, changed
		8	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed
		9	Figure 1.2 Block Diagram changed
		10	Table 1.4 Pin Functions changed
		15	Figure 1.5 Pin Assignments of the 48-Pin LFQFP/HWQFN: Note added
		16	Figure 1.6 Pin Assignments of the 40-Pin HWQFN: Note added
		3. Address Space	
		30	Figure 3.1 Memory Map, changed
		4. I/O Registers	
		33 to 48	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics	
		49	Table 5.1 Absolute Maximum Ratings, Table 5.2 Recommended Operating Conditions, changed
		50	Table 5.3 DC Characteristics (1) and Table 5.4 DC Characteristics (2), changed
		51	Table 5.5 DC Characteristics (3), changed
		55, 56	Table 5.8 DC Characteristics (6), added
		56	Table 5.9 DC Characteristics (7), changed
		58	Table 5.10 DC Characteristics (8), added
		59	Table 5.13 DC Characteristics (11), changed
		61	Table 5.19 Output Values of Voltage (1) and Table 5.20 Output Values of Voltage (2), changed
		68	Table 5.22 Operation Frequency Value (Middle-Speed Operating Mode) changed, Note 4 added
		69	Table 5.24 Clock Timing, changed
		78	Table 5.32 Timing of On-Chip Peripheral Modules (1) changed
		81	Table 5.35 Timing of On-Chip Peripheral Modules (4), changed
		82	Table 5.36 Timing of On-Chip Peripheral Modules (5): Note 2 deleted
		83	Figure 5.37 SCK Clock Input Timing changed
		84	Figure 5.38 SCI Input/Output Timing: Clock Synchronous Mode changed