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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51116adfl-3a

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products (1/2)

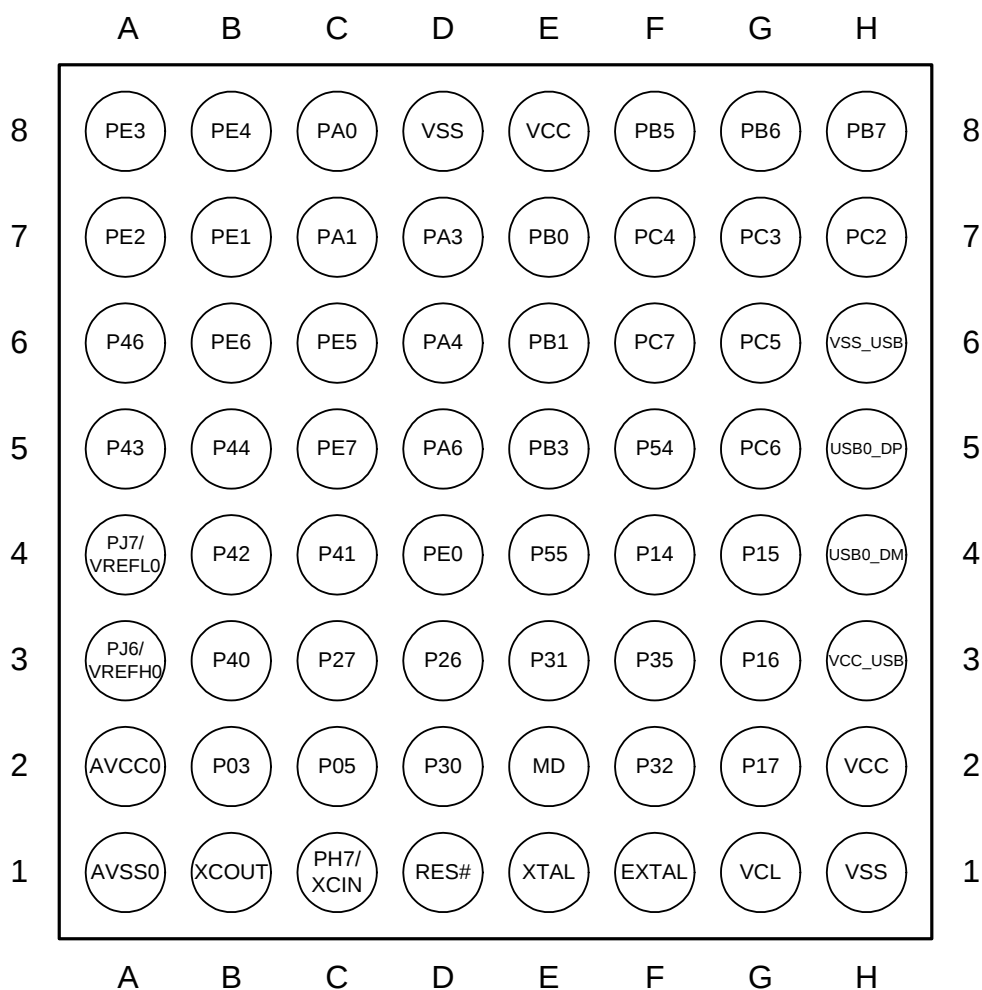
Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Maximum Operating Frequency	Operating Temperature
RX111	R5F51118AGFM	R5F51118AGFM#3A	PLQP0064KB-A	512 Kbytes	64 Kbytes	8 Kbytes	32 MHz	−40 to +105°C
	R5F51118AGFK	R5F51118AGFK#3A	PLQP0064GA-A					
	R5F51118AGFL	R5F51118AGFL#3A	PLQP0048KB-A					
	R5F51118AGNE	R5F51118AGNE#UA	PWQN0048KB-A					
	R5F51117AGFM	R5F51117AGFM#3A	PLQP0064KB-A	384 Kbytes				
	R5F51117AGFK	R5F51117AGFK#3A	PLQP0064GA-A					
	R5F51117AGFL	R5F51117AGFL#3A	PLQP0048KB-A					
	R5F51117AGNE	R5F51117AGNE#UA	PWQN0048KB-A					
	R5F51116AGFM	R5F51116AGFM#3A	PLQP0064KB-A	256 Kbytes	32 Kbytes			
	R5F51116AGFK	R5F51116AGFK#3A	PLQP0064GA-A					
	R5F51116AGFL	R5F51116AGFL#3A	PLQP0048KB-A					
	R5F51116AGNE	R5F51116AGNE#UA	PWQN0048KB-A					
	R5F51115AGFM	R5F51115AGFM#3A	PLQP0064KB-A	128 Kbytes	16 Kbytes			
	R5F51115AGFK	R5F51115AGFK#3A	PLQP0064GA-A					
	R5F51115AGFL	R5F51115AGFL#3A	PLQP0048KB-A					
	R5F51115AGNE	R5F51115AGNE#UA	PWQN0048KB-A					
	R5F51114AGFM	R5F51114AGFM#3A	PLQP0064KB-A	96 Kbytes				
	R5F51114AGFK	R5F51114AGFK#3A	PLQP0064GA-A					
	R5F51114AGFL	R5F51114AGFL#3A	PLQP0048KB-A					
	R5F51114AGNE	R5F51114AGNE#UA	PWQN0048KB-A					
	R5F51113AGFM	R5F51113AGFM#3A	PLQP0064KB-A	64 Kbytes	10 Kbytes			
	R5F51113AGFK	R5F51113AGFK#3A	PLQP0064GA-A					
	R5F51113AGFL	R5F51113AGFL#3A	PLQP0048KB-A					
	R5F51113AGNE	R5F51113AGNE#UA	PWQN0048KB-A					
	R5F51113AGNF	R5F51113AGNF#UA	PWQN0040KC-A	32 Kbytes				
	R5F51111AGFM	R5F51111AGFM#3A	PLQP0064KB-A					
	R5F51111AGFK	R5F51111AGFK#3A	PLQP0064GA-A					
	R5F51111AGFL	R5F51111AGFL#3A	PLQP0048KB-A					
	R5F51111AGNE	R5F51111AGNE#UA	PWQN0048KB-A	16 Kbytes	8 Kbytes			
	R5F51111AGNF	R5F51111AGNF#UA	PWQN0040KC-A					
	R5F5111JAGFM	R5F5111JAGFM#3A	PLQP0064KB-A					
	R5F5111JAGFK	R5F5111JAGFK#3A	PLQP0064GA-A					
	R5F5111JAGFL	R5F5111JAGFL#3A	PLQP0048KB-A					
	R5F5111JAGNE	R5F5111JAGNE#UA	PWQN0048KB-A					
	R5F5111JAGNF	R5F5111JAGNF#UA	PWQN0040KC-A					

Table 1.4 Pin Functions (3/3)

Classifications	Pin Name	I/O	Description
USB 2.0 host/ function module	USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver.
	USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver.
	USB0_VBUS	Input	USB cable connection monitor pin.
	USB0_EXICEN	Output	Low-power control signal for the OTG chip.
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for the OTG chip.
	USB0_OVRCURA, USB0_OVRCURB	Input	External overcurrent detection pins.
	USB0_ID	Input	Mini-AB connector ID input pin during operation in OTG mode.
12-bit A/D converter	AN000 to AN004, AN006, AN008 to AN015	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.
I/O ports	P03, P05	I/O	2-bit input/output pins.
	P14 to P17	I/O	4-bit input/output pins.
	P26, P27	I/O	2-bit input/output pins.
	P30 to P32, P35	I/O	4-bit input/output pins (P35 input pin).
	P40 to P44, P46	I/O	6-bit input/output pins.
	P54, P55	I/O	2-bit input/output pins.
	PA0, PA1, PA3, PA4, PA6	I/O	5-bit input/output pins.
	PB0, PB1, PB3, PB5 to PB7	I/O	6-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH7	Input	1-bit input pin.
	PJ6, PJ7	I/O	2-bit input/output pins.

Note 1. For external clock input.

RX111 Group
PWLG0064KA-A
(64-pin WFLGA)
(Upper perspective view)



Note:

- This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table "List of Pins and Pin Functions (64-Pin WFLGA)".
- For the position of A1 pin in the package, see "Package Dimensions".

Figure 1.4 Pin Assignments of the 64-Pin WFLGA

Table 1.5 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC)	Communication (SCle, SCIf, RSPI, RIIC, USB)	Others
42		PA4	MTIC5U/MTCLKA/MTIOC2B	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
43		PA3	MTIOC0D/MTCLKD/MTIOC1B/POE0#	RXD5/SMISO5/SSCL5/MISOA	IRQ6
44		PA1	MTIOC0B/MTCLKC/RTCOU	SCK5/SSLA2	
45		PA0	MTIOC4A	SSLA1	CACREF
46		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
47		PE4	MTIOC4D/MTIOC1A/MTIOC3A	MOSIA	IRQ4/AN012
48		PE3	MTIOC0A/MTIOC1B/MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/RSPCKA	IRQ3/AN011
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12	IRQ7/AN010
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/SSDA12	IRQ1/AN009
51		PE0	MTIOC2A/POE3#	SCK12	IRQ0/AN008
52		PE7			IRQ7/AN015
53		PE6			IRQ6/AN014
54		P46*2			AN006
55		P44*2			AN004
56		P43*2			AN003
57		P42*2			AN002
58		P41*2			AN001
59	VREFL0	PJ7*2			
60		P40*2			AN000
61	VREFH0	PJ6*2			
62	AVSS0				
63	AVCC0				
64		P05			DA1

Note 1. Not 5 V tolerant.

Note 2. The power source of the I/O buffer for these pins is AVCC0.

2.1 General-Purpose Registers (R0 to R15)

This CPU has 16 general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of 4, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

When executing an instruction after writing to multiple registers, only read the last I/O register written to and execute the instruction using that value; it is not necessary to execute the instruction using the values written to all the registers.

(3) Number of cycles necessary for accessing I/O registers

See Table 4.1 for details on the number of clock cycles necessary for accessing I/O registers.

The number of access cycles to I/O registers is obtained by following equation.*1

$$\begin{aligned} \text{Number of access cycles to I/O registers} = & \text{Number of bus cycles for internal main bus 1} + \\ & \text{Number of divided clock synchronization cycles} + \\ & \text{Number of bus cycles for internal peripheral buses 1 to 6} \end{aligned}$$

The number of bus cycles of internal peripheral buses 1 to 6 differs according to the register to be accessed.

When peripheral functions connected to internal peripheral buses 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.

The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DTC).

(4) Notes on sleep mode and mode transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

Table 4.1 List of I/O Registers (Address Order) (2/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 7026h	ICU	Interrupt Request Register 038	IR038	8	8	2 ICLK
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK
0008 703Fh	ICU	Interrupt Request Register 063	IR063	8	8	2 ICLK
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK
0008 7058h	ICU	Interrupt Request Register 088	IR088	8	8	2 ICLK
0008 7059h	ICU	Interrupt Request Register 089	IR089	8	8	2 ICLK
0008 705Ah	ICU	Interrupt Request Register 090	IR090	8	8	2 ICLK
0008 705Ch	ICU	Interrupt Request Register 092	IR092	8	8	2 ICLK
0008 705Dh	ICU	Interrupt Request Register 093	IR093	8	8	2 ICLK
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (13/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CCh	PORTC	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB
0008 C120h	PORT	Port Switching Register B	PSRB	8	8	2 or 3 PCLKB
0008 C121h	PORT	Port Switching Register A	PSRA	8	8	2 or 3 PCLKB
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2 or 3 PCLKB
0008 C145h	MPC	P05 Pin Function Control Register	P05PFS	8	8	2 or 3 PCLKB
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2 or 3 PCLKB
0008 C14Dh	MPC	P15 Pin Function Control Register	P15PFS	8	8	2 or 3 PCLKB
0008 C14Eh	MPC	P16 Pin Function Control Register	P16PFS	8	8	2 or 3 PCLKB
0008 C14Fh	MPC	P17 Pin Function Control Register	P17PFS	8	8	2 or 3 PCLKB
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2 or 3 PCLKB
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 or 3 PCLKB
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2 or 3 PCLKB
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2 or 3 PCLKB
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2 or 3 PCLKB
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2 or 3 PCLKB
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2 or 3 PCLKB
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2 or 3 PCLKB
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2 or 3 PCLKB
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2 or 3 PCLKB
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2 or 3 PCLKB
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2 or 3 PCLKB
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2 or 3 PCLKB
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2 or 3 PCLKB
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (15/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2 or 3 PCLKB
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3 or 4 PCLKB
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLK or more
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLK or more
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	16	3 or 4 PCLKB
000A 0018h	USB0	D0FIFO Port Register	D0FIFO	16	16	3 or 4 PCLKB
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	16	3 or 4 PCLKB
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3 or 4 PCLKB
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3 or 4 PCLKB
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3 or 4 PCLKB
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3 or 4 PCLKB
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3 or 4 PCLKB
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3 or 4 PCLKB
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more
000A 0090h	USB0	PIPE1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more
000A 0092h	USB0	PIPE1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more
000A 0094h	USB0	PIPE2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more
000A 0096h	USB0	PIPE2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more

Table 5.7 DC Characteristics (5) (2/2)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	Low-speed operating mode	Normal operating mode	No peripheral operation*8	ICLK = 32.768 kHz	I _{CC}	4.0	—	μA	
			All peripheral operation: Normal*9, *10	ICLK = 32.768 kHz		11.5	—		
			All peripheral operation: Max.*9, *10	ICLK = 32.768 kHz		—	40		
		Sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		2.2	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		7.1	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		1.8	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		5.3	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to the same frequency as ICLK.

Note 4. Values when $\text{VCC} = 3.3\text{ V}$.

Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.

Note 6. Clock supply to the peripheral functions is stopped. The clock source is PLL when ICLK = 12 MHz, and HOCO otherwise. FCLK and PCLK are set to divided by 64.

Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK = 12 MHz, and HOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.

Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.

Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.

Note 10. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to "transition to the module stop state is made".

[256-Kbyte or more flash memory]

Table 5.8 DC Characteristics (6) (1/2)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $V_{SS} = AVSS0 = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item					Symbol	Typ *4	Max	Unit	Test Conditions				
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz	I _{CC}	3.6	—	mA					
				ICLK = 16 MHz		2.4	—						
				ICLK = 8 MHz		1.8	—						
			All peripheral operation: Normal*3	ICLK = 32 MHz		13.4	—						
				ICLK = 16 MHz		7.5	—						
				ICLK = 8 MHz		4.5	—						
			All peripheral operation: Max.*3	ICLK = 32 MHz		—	27						
		Sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.9	—						
				ICLK = 16 MHz		1.5	—						
				ICLK = 8 MHz		1.3	—						
			All peripheral operation: Normal*3	ICLK = 32 MHz		7.6	—						
				ICLK = 16 MHz		4.4	—						
				ICLK = 8 MHz		2.8	—						
		Deep sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.1	—						
				ICLK = 16 MHz		1.0	—						
				ICLK = 8 MHz		0.9	—						
			All peripheral operation: Normal*3	ICLK = 32 MHz		5.8	—						
				ICLK = 16 MHz		3.4	—						
				ICLK = 8 MHz		2.1	—						
		Increase during flash rewrite*5					2.5			—			
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I _{CC}	2.1	—	mA					
				ICLK = 8 MHz		1.4	—						
				ICLK = 1 MHz		0.8	—						
			All peripheral operation: Normal*7	ICLK = 12 MHz		5.9	—						
				ICLK = 8 MHz		4.2	—						
				ICLK = 1 MHz		1.3	—						
			All peripheral operation: Max.*7	ICLK = 12 MHz		—	12.2						
		Sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.4	—						
ICLK = 8 MHz				0.9		—							
ICLK = 1 MHz				0.7		—							
All peripheral operation: Normal*7			ICLK = 12 MHz	3.6		—							
			ICLK = 8 MHz	2.5		—							
			ICLK = 1 MHz	1.1		—							
Deep sleep mode		No peripheral operation*6	ICLK = 12 MHz	1.1		—							
			ICLK = 8 MHz	0.6		—							
			ICLK = 1 MHz	0.6		—							
		All peripheral operation: Normal*7	ICLK = 12 MHz	2.9		—							
			ICLK = 8 MHz	2.0		—							
			ICLK = 1 MHz	0.9		—							
Increase during flash rewrite*5						2.5	—						

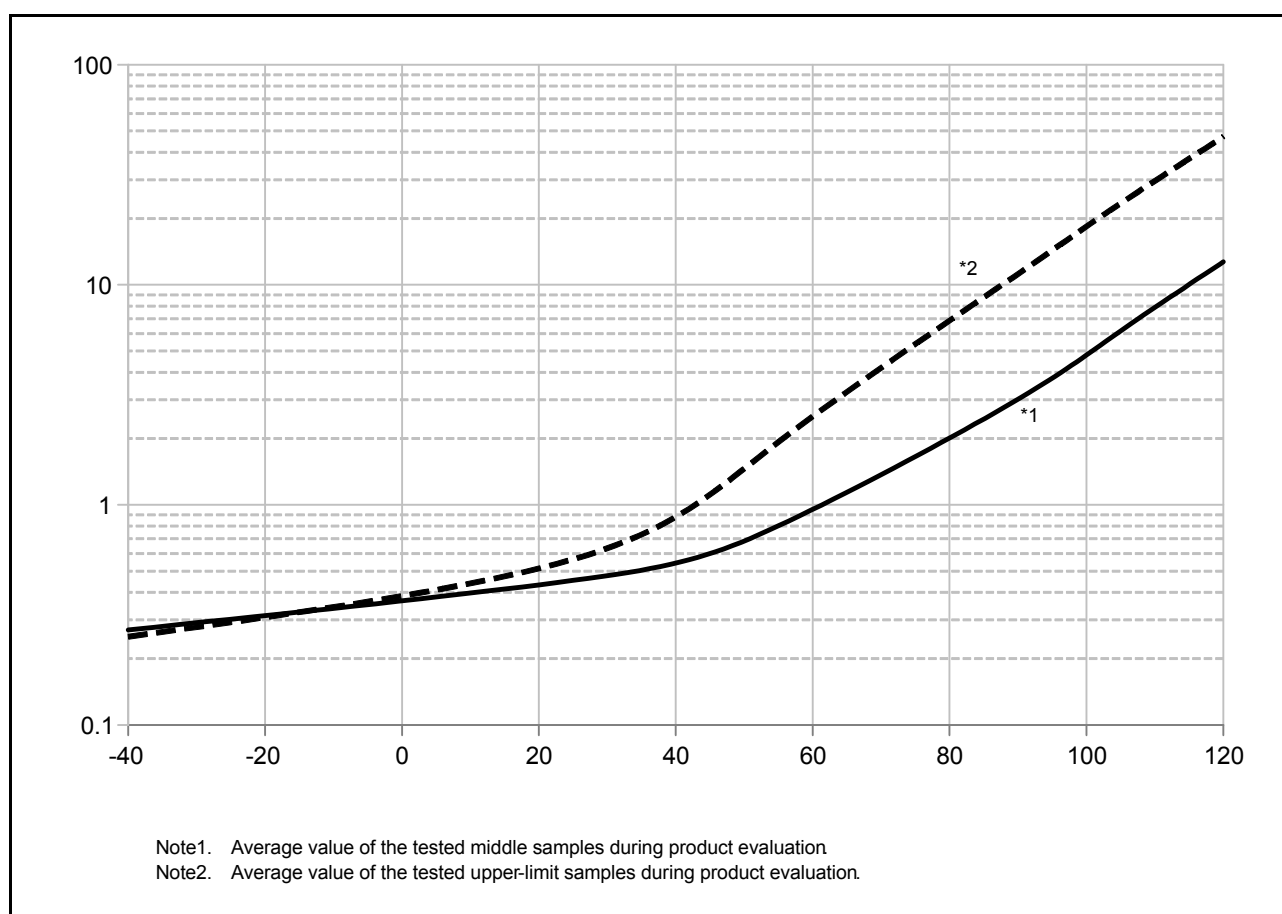


Figure 5.10 Temperature Dependency in Software Standby Mode (Reference Data)

Table 5.11 DC Characteristics (9)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	300	mW	D version ($T_a = -40\text{ to }85^\circ\text{C}$)
		—	105		G version ($T_a = -40\text{ to }105^\circ\text{C}$)*2

Note 1. Total power dissipated by the entire chip (including output currents).

Note 2. Please contact Renesas Electronics sales office for derating under $T_a = +85^\circ\text{C}$ to 105°C . Derating is the systematic reduction of load for the sake of improved reliability.

Table 5.14 DC Characteristics (12)Conditions: $0\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V	
	During fast startup time*2		0.02	—	2		
	Voltage monitoring 1 reset enabled at startup*3, *4		0.02	—	—		

Note: When powering on AVCC0 and VCC, power them on at the same time or VCC first.

Note 1. When OFS1.(STUPLVD1REN, FASTSTUP) = 11b.

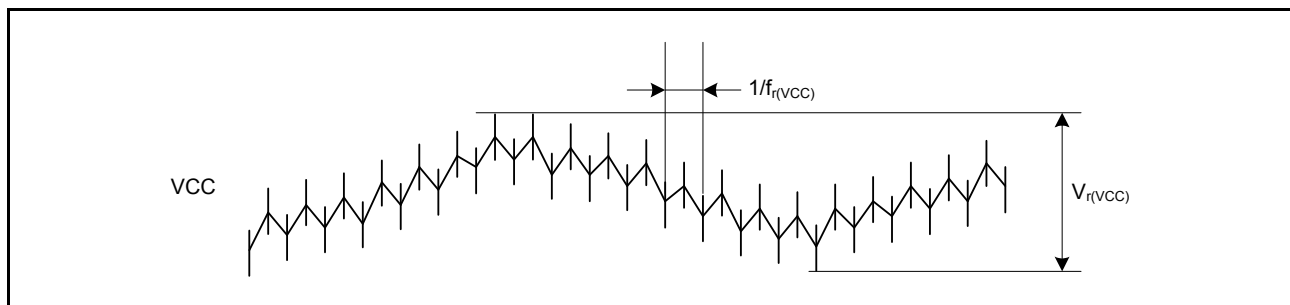
Note 2. When OFS1.(STUPLVD1REN, FASTSTUP) = 10b.

Note 3. When OFS1.STUPLVD1REN = 0.

Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

Table 5.15 DC Characteristics (13)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$ The ripple voltage must meet the allowable ripple frequency $f_{r(\text{VCC})}$ within the range between the VCC upper limit (3.6 V) and lower limit (1.8 V).When VCC change exceeds $\text{VCC} \pm 10\%$, the allowable voltage change rising/falling gradient $dt/d\text{VCC}$ must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r(\text{VCC})}$	—	—	10	kHz	Figure 5.11 $V_{r(\text{VCC})} \leq \text{VCC} \times 0.2$
		—	—	1	MHz	Figure 5.11 $V_{r(\text{VCC})} \leq \text{VCC} \times 0.08$
		—	—	10	MHz	Figure 5.11 $V_{r(\text{VCC})} \leq \text{VCC} \times 0.06$
Allowable voltage change rising/falling gradient	$dt/d\text{VCC}$	1.0	—	—	ms/V	When VCC change exceeds $\text{VCC} \pm 10\%$

**Figure 5.11 Ripple Waveform****Table 5.16 DC Characteristics (14)**Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	1.4	4.7	7.0	μF	

Note: • The recommended capacitance is 4.7 μF . Variations in connected capacitors should be within the above range.

Table 5.19 Output Voltage (1)Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $2.7\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $V_{SS} = AVSS0 = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	All output ports (except for RIIC, ports P40 to P44, P46, ports PJ6, PJ7)		V _{OL}	—	0.6	V	I _{OL} = 3.0 mA
				—	0.4		I _{OL} = 1.5 mA
	Ports P40 to P44, P46, ports PJ6, PJ7			—	0.4		I _{OL} = 0.4 mA
	RIIC pins	Standard mode		—	0.4		I _{OL} = 3.0 mA
		Fast mode		—	0.6		I _{OL} = 6.0 mA
High-level output voltage	All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7)		V _{OH}	VCC – 0.5	—	V	I _{OH} = –2.0 mA
	Ports P40 to P44, P46, ports PJ6, PJ7			AVCC0 – 0.5	—		I _{OH} = –0.1 mA

Table 5.20 Output Voltage (2)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 2.7\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 2.7\text{ V}$, $V_{SS} = AVSS0 = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7)	V_{OL}	—	0.6	V	$I_{OL} = 1.5\text{ mA}$
	Ports P40 to P44, P46, ports PJ6, PJ7		—	0.4		$I_{OL} = 0.4\text{ mA}$
High-level output voltage	All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7)	V_{OH}	$V_{CC} - 0.5$	—	V	$I_{OH} = -1.0\text{ mA}$
	Ports P40 to P44, P46, ports PJ6, PJ7		$AVCC0 - 0.5$	—		$I_{OH} = -0.1\text{ mA}$

5.3.4 Control Signal Timing

Table 5.31 Control Signal Timing

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

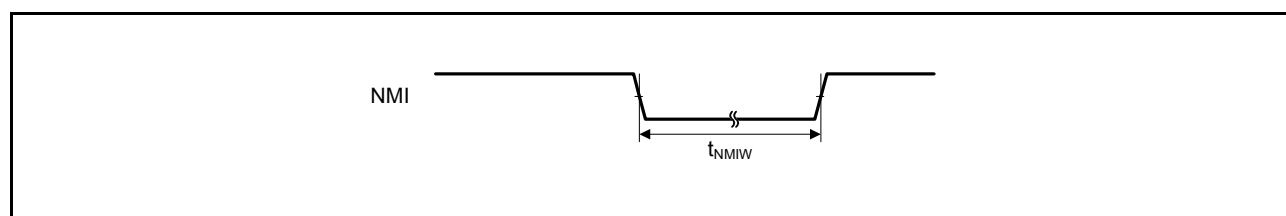
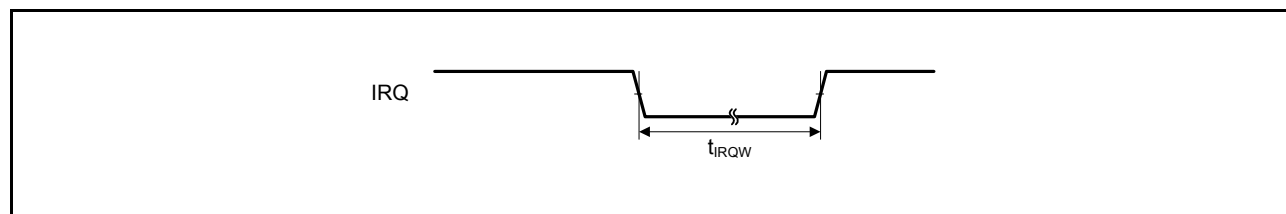
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	$t_{\text{Pcyc}} \times 2 \leq 200\text{ ns}$
		$t_{\text{Pcyc}} \times 2^{*1}$	—	—			$t_{\text{Pcyc}} \times 2 > 200\text{ ns}$
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	$t_{\text{NMICK}} \times 3 \leq 200\text{ ns}$
		$t_{\text{NMICK}} \times 3.5^{*2}$	—	—			$t_{\text{NMICK}} \times 3 > 200\text{ ns}$
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	$t_{\text{Pcyc}} \times 2 \leq 200\text{ ns}$
		$t_{\text{Pcyc}} \times 2^{*1}$	—	—			$t_{\text{Pcyc}} \times 2 > 200\text{ ns}$
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	$t_{\text{IRQCK}} \times 3 \leq 200\text{ ns}$
		$t_{\text{IRQCK}} \times 3.5^{*3}$	—	—			$t_{\text{IRQCK}} \times 3 > 200\text{ ns}$

Note: • 200 ns minimum in software standby mode.

Note 1. t_{Pcyc} indicates the cycle of PCLKB.

Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.

Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

**Figure 5.36 NMI Interrupt Input Timing****Figure 5.37 IRQ Interrupt Input Timing**

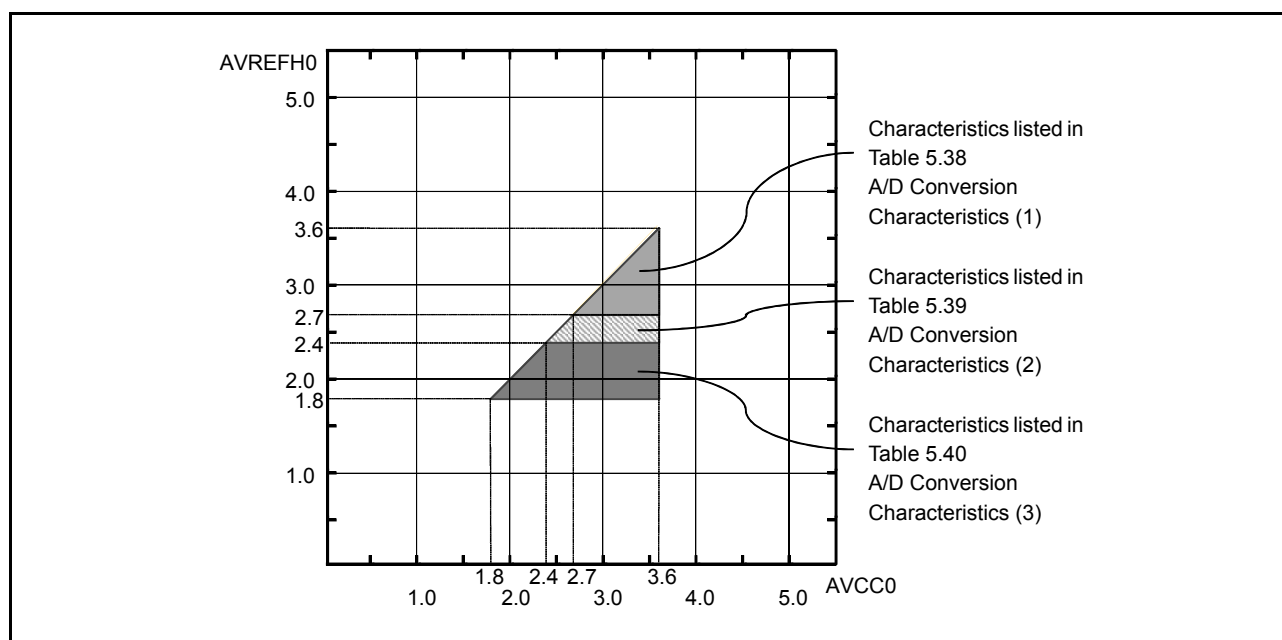


Figure 5.56 AVCC0 to AVREFH0 Voltage Range

Table 5.39 A/D Conversion Characteristics (2)

Conditions: $2.4\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $2.4\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $2.4\text{ V} \leq V_{REFH0} \leq AV_{CC0}$, $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		4	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 1.0 kΩ	2.062 (0.625)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 09h
		2.750 (1.313)*2	—	—	μs	Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±6.0	LSB	
Full-scale error		—	±1.25	±6.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.40 A/D Conversion Characteristics (3)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $1.8\text{ V} \leq V_{REFH0} \leq AV_{CC0}$, $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5.0 kΩ	4.875 (1.250)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 09h
		6.250 (2.625)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±24.0	LSB	
Full-scale error		—	±1.25	±24.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.75	±32.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.25	±12.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

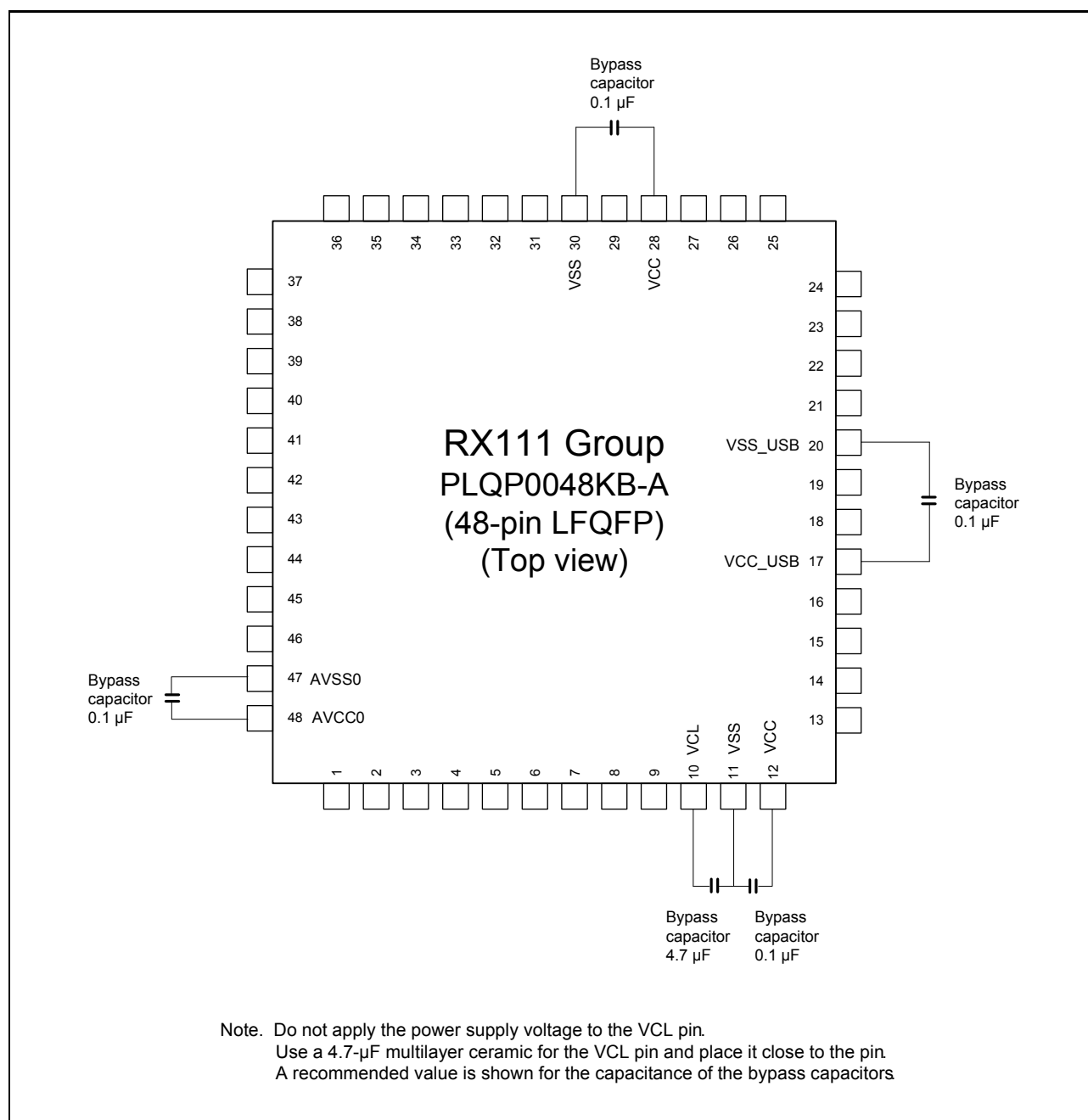


Figure 5.64 Connecting Capacitors (48-pin LQFP)

REVISION HISTORY	RX111 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.60	Apr 15, 2013	—	First edition, issued
0.90	May 15, 2013	Features	
		1	Changed
		1. Overview	
		2 to 4	Table 1.1 Outline of Specifications changed
		10 to 12	Table 1.4 Pin Functions changed
		13	Figure 1.3 Pin Assignments of the 64-Pin LQFP changed
		14	Figure 1.4 Pin Assignments of the 64-Pin WFLGA changed
		15	Figure 1.5 Pin Assignments of the 48-Pin LQFP/HWQFN changed
		18, 19	Table 1.5 List of Pins and Pin Functions (64-Pin LQFP) changed, Note 1 added
		20, 21	Table 1.6 List of Pins and Pin Functions (64-Pin WFLGA) changed, Note 1 added
		22, 23	Table 1.7 List of Pins and Pin Functions (48-Pin LQFP/HWQFN) changed, Note 1 added
		24, 25	Table 1.8 List of Pins and Pin Functions (40-Pin HWQFN) changed, Note 1 added
		26	Table 1.9 List of Pins and Pin Functions (36-Pin WFLGA) changed, Note 1 added
		4. I/O Registers	
		33 to 48	Table 5.1 List of I/O Registers (Address Order) changed
1.00	Jun 19, 2013	1. Overview	
		9	Figure 1.2 Block Diagram changed
		20, 21	Table 1.6 List of Pins and Pin Functions (64-Pin WFLGA) changed
		26	Table 1.9 List of Pins and Pin Functions (36-Pin WFLGA) changed
		4. I/O Registers	
		33 to 48	Table 4.1 List of I/O Registers (Address Order) changed
		5. Electrical Characteristics	
1.20	Sep 29, 2014	49 to 99	Added
		1. Overview	
		2 to 4	Table 1.1 Outline of Specifications: ROM capacity and RAM capacity changed, Unique ID added
		6, 7	Table 1.3 List of Products, changed
		8	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed
		9	Figure 1.2 Block Diagram changed
		10	Table 1.4 Pin Functions changed
		15	Figure 1.5 Pin Assignments of the 48-Pin LQFP/HWQFN: Note added
		16	Figure 1.6 Pin Assignments of the 40-Pin HWQFN: Note added
		3. Address Space	
		30	Figure 3.1 Memory Map, changed
		4. I/O Registers	
		33 to 48	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics	
		49	Table 5.1 Absolute Maximum Ratings, Table 5.2 Recommended Operating Conditions, changed
		50	Table 5.3 DC Characteristics (1) and Table 5.4 DC Characteristics (2), changed
		51	Table 5.5 DC Characteristics (3), changed
		55, 56	Table 5.8 DC Characteristics (6), added
		56	Table 5.9 DC Characteristics (7), changed
		58	Table 5.10 DC Characteristics (8), added
		59	Table 5.13 DC Characteristics (11), changed
		61	Table 5.19 Output Values of Voltage (1) and Table 5.20 Output Values of Voltage (2), changed
		68	Table 5.22 Operation Frequency Value (Middle-Speed Operating Mode) changed, Note 4 added
		69	Table 5.24 Clock Timing, changed
		78	Table 5.32 Timing of On-Chip Peripheral Modules (1) changed
		81	Table 5.35 Timing of On-Chip Peripheral Modules (4), changed
		82	Table 5.36 Timing of On-Chip Peripheral Modules (5): Note 2 deleted
		83	Figure 5.37 SCK Clock Input Timing changed
		84	Figure 5.38 SCI Input/Output Timing: Clock Synchronous Mode changed

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.