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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51117adfl-3a

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products (1/2)

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Maximum Operating Frequency	Operating Temperature			
RX111	R5F51118AGFM	R5F51118AGFM#3A	PLQP0064KB-A	512 Kbytes	64 Kbytes	8 Kbytes	32 MHz	-40 to +105°C			
	R5F51118AGFK	R5F51118AGFK#3A	PLQP0064GA-A								
	R5F51118AGFL	R5F51118AGFL#3A	PLQP0048KB-A								
	R5F51118AGNE	R5F51118AGNE#UA	PWQN0048KB-A								
	R5F51117AGFM	R5F51117AGFM#3A	PLQP0064KB-A	384 Kbytes							
	R5F51117AGFK	R5F51117AGFK#3A	PLQP0064GA-A								
	R5F51117AGFL	R5F51117AGFL#3A	PLQP0048KB-A								
	R5F51117AGNE	R5F51117AGNE#UA	PWQN0048KB-A								
	R5F51116AGFM	R5F51116AGFM#3A	PLQP0064KB-A	256 Kbytes	32 Kbytes						
	R5F51116AGFK	R5F51116AGFK#3A	PLQP0064GA-A								
	R5F51116AGFL	R5F51116AGFL#3A	PLQP0048KB-A								
	R5F51116AGNE	R5F51116AGNE#UA	PWQN0048KB-A								
	R5F51115AGFM	R5F51115AGFM#3A	PLQP0064KB-A	128 Kbytes	16 Kbytes						
	R5F51115AGFK	R5F51115AGFK#3A	PLQP0064GA-A								
	R5F51115AGFL	R5F51115AGFL#3A	PLQP0048KB-A								
	R5F51115AGNE	R5F51115AGNE#UA	PWQN0048KB-A								
	R5F51114AGFM	R5F51114AGFM#3A	PLQP0064KB-A	96 Kbytes							
	R5F51114AGFK	R5F51114AGFK#3A	PLQP0064GA-A								
	R5F51114AGFL	R5F51114AGFL#3A	PLQP0048KB-A								
	R5F51114AGNE	R5F51114AGNE#UA	PWQN0048KB-A								
	R5F51113AGFM	R5F51113AGFM#3A	PLQP0064KB-A	64 Kbytes	10 Kbytes						
	R5F51113AGFK	R5F51113AGFK#3A	PLQP0064GA-A								
	R5F51113AGFL	R5F51113AGFL#3A	PLQP0048KB-A								
	R5F51113AGNE	R5F51113AGNE#UA	PWQN0048KB-A								
	R5F51113AGNF	R5F51113AGNF#UA	PWQN0040KC-A	32 Kbytes							
	R5F51111AGFM	R5F51111AGFM#3A	PLQP0064KB-A								
	R5F51111AGFK	R5F51111AGFK#3A	PLQP0064GA-A								
	R5F51111AGFL	R5F51111AGFL#3A	PLQP0048KB-A								
	R5F51111AGNE	R5F51111AGNE#UA	PWQN0048KB-A								
	R5F51111AGNF	R5F51111AGNF#UA	PWQN0040KC-A	16 Kbytes	8 Kbytes						
	R5F5111JAGFM	R5F5111JAGFM#3A	PLQP0064KB-A								
	R5F5111JAGFK	R5F5111JAGFK#3A	PLQP0064GA-A								
	R5F5111JAGFL	R5F5111JAGFL#3A	PLQP0048KB-A								
	R5F5111JAGNE	R5F5111JAGNE#UA	PWQN0048KB-A								
	R5F5111JAGNF	R5F5111JAGNF#UA	PWQN0040KC-A								

Table 1.4 Pin Functions (3/3)

Classifications	Pin Name	I/O	Description
USB 2.0 host/ function module	USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver.
	USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver.
	USB0_VBUS	Input	USB cable connection monitor pin.
	USB0_EXICEN	Output	Low-power control signal for the OTG chip.
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for the OTG chip.
	USB0_OVRCURA, USB0_OVRCURB	Input	External overcurrent detection pins.
	USB0_ID	Input	Mini-AB connector ID input pin during operation in OTG mode.
12-bit A/D converter	AN000 to AN004, AN006, AN008 to AN015	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.
I/O ports	P03, P05	I/O	2-bit input/output pins.
	P14 to P17	I/O	4-bit input/output pins.
	P26, P27	I/O	2-bit input/output pins.
	P30 to P32, P35	I/O	4-bit input/output pins (P35 input pin).
	P40 to P44, P46	I/O	6-bit input/output pins.
	P54, P55	I/O	2-bit input/output pins.
	PA0, PA1, PA3, PA4, PA6	I/O	5-bit input/output pins.
	PB0, PB1, PB3, PB5 to PB7	I/O	6-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH7	Input	1-bit input pin.
	PJ6, PJ7	I/O	2-bit input/output pins.

Note 1. For external clock input.

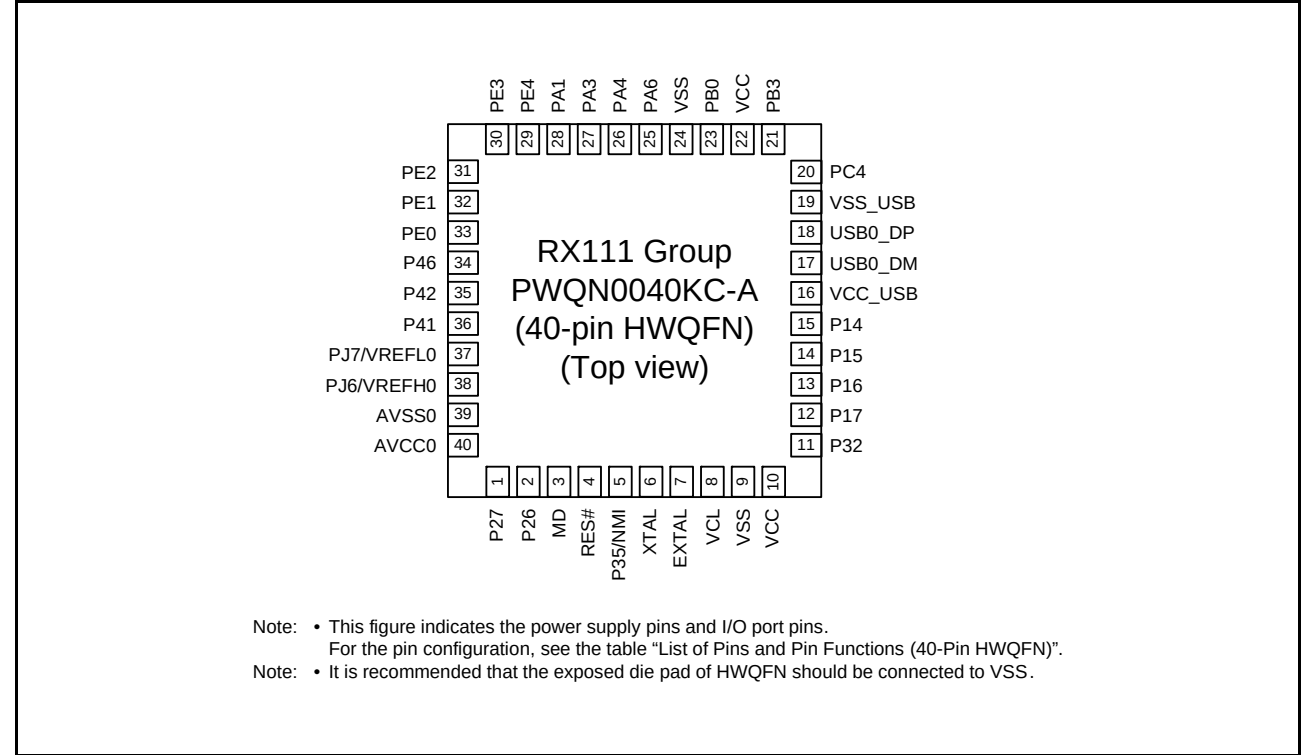


Figure 1.6 Pin Assignments of the 40-Pin HWQFN

Table 4.1 List of I/O Registers (Address Order) (7/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB
0008 8600h	MTU3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8601h	MTU4	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8602h	MTU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8603h	MTU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8604h	MTU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8605h	MTU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8606h	MTU4	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8607h	MTU4	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8608h	MTU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8609h	MTU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 860Ah	MTU	Timer Output Master Enable Register	TOER	8	8	2 or 3 PCLKB
0008 860Dh	MTU	Timer Gate Control Register	TGCR	8	8	2 or 3 PCLKB
0008 860Eh	MTU	Timer Output Control Register 1	TOCR1	8	8	2 or 3 PCLKB
0008 860Fh	MTU	Timer Output Control Register 2	TOCR2	8	8	2 or 3 PCLKB
0008 8610h	MTU3	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8612h	MTU4	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8614h	MTU	Timer Cycle Data Register	TCDR	16	16	2 or 3 PCLKB
0008 8616h	MTU	Timer Dead Time Data Register	TDDR	16	16	2 or 3 PCLKB
0008 8618h	MTU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 861Ah	MTU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 861Ch	MTU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 861Eh	MTU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8620h	MTU	Timer Subcounter	TCNTS	16	16	2 or 3 PCLKB
0008 8622h	MTU	Timer Cycle Buffer Register	TCBR	16	16	2 or 3 PCLKB
0008 8624h	MTU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 8626h	MTU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 8628h	MTU4	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 862Ah	MTU4	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 862Ch	MTU3	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 862Dh	MTU4	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8630h	MTU	Timer Interrupt Skipping Set Register	TITCR	8	8	2 or 3 PCLKB
0008 8631h	MTU	Timer Interrupt Skipping Counter	TITCNT	8	8	2 or 3 PCLKB
0008 8632h	MTU	Timer Buffer Transfer Set Register	TBTER	8	8	2 or 3 PCLKB
0008 8634h	MTU	Timer Dead Time Enable Register	TDER	8	8	2 or 3 PCLKB
0008 8636h	MTU	Timer Output Level Buffer Register	TOLBR	8	8	2 or 3 PCLKB
0008 8638h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8639h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8640h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	2 or 3 PCLKB
0008 8644h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	2 or 3 PCLKB
0008 8646h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	2 or 3 PCLKB
0008 8648h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (9/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 88A2h	MTU5	Timer General Register W	TGRW	16	16	2 or 3 PCLKB
0008 88A4h	MTU5	Timer Control Register W	TCRW	8	8	2 or 3 PCLKB
0008 88A6h	MTU5	Timer I/O Control Register W	TIORW	8	8	2 or 3 PCLKB
0008 88B2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 88B4h	MTU5	Timer Start Register	TSTR	8	8	2 or 3 PCLKB
0008 88B6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	2 or 3 PCLKB
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9004h	S12AD	A/D Channel Select Register A	ADANSA	16	16	2 or 3 PCLKB
0008 9008h	S12AD	A/D-Converted Value Addition Mode Select Register	ADADS	16	16	2 or 3 PCLKB
0008 900Ch	S12AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9010h	S12AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9012h	S12AD	A/D Converted Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9014h	S12AD	A/D Channel Select Register B	ADANSB	16	16	2 or 3 PCLKB
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSRDR	16	16	2 or 3 PCLKB
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 9030h	S12AD	A/D Data Register 8	ADDR8	16	16	2 or 3 PCLKB
0008 9032h	S12AD	A/D Data Register 9	ADDR9	16	16	2 or 3 PCLKB
0008 9034h	S12AD	A/D Data Register 10	ADDR10	16	16	2 or 3 PCLKB
0008 9036h	S12AD	A/D Data Register 11	ADDR11	16	16	2 or 3 PCLKB
0008 9038h	S12AD	A/D Data Register 12	ADDR12	16	16	2 or 3 PCLKB
0008 903Ah	S12AD	A/D Data Register 13	ADDR13	16	16	2 or 3 PCLKB
0008 903Ch	S12AD	A/D Data Register 14	ADDR14	16	16	2 or 3 PCLKB
0008 903Eh	S12AD	A/D Data Register 15	ADDR15	16	16	2 or 3 PCLKB
0008 9060h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 9061h	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 9070h	S12AD	A/D Sampling State Register T	ADSSTRT	8	8	2 or 3 PCLKB
0008 9071h	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB
0008 9073h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 9074h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 9075h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 9076h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB
0008 9078h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (14/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2 or 3 PCLKB
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2 or 3 PCLKB
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2 or 3 PCLKB
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2 or 3 PCLKB
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2 or 3 PCLKB
0008 C1A7h	MPC	PC7 Pin Function Control Register	PC7PFS	8	8	2 or 3 PCLKB
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2 or 3 PCLKB
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2 or 3 PCLKB
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2 or 3 PCLKB
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2 or 3 PCLKB
0008 C1D6h	MPC	PJ6 Pin Function Control Register	PJ6PFS	8	8	2 or 3 PCLKB
0008 C1D7h	MPC	PJ7 Pin Function Control Register	PJ7PFS	8	8	2 or 3 PCLKB
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4 or 5 PCLKB
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB
0008 C408h	RTC	Day-Of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)Conditions: $2.7\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $2.7\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	$\text{VCC} \times 0.7$	—	5.8	V	
	Ports P16, P17, port PA6, port PB0 (5 V tolerant)		$\text{VCC} \times 0.8$	—	5.8		
	Ports P03, P05, ports P14, P15, ports P26, P27, ports P30 to P32, P35, ports P54, P55, ports PA0, PA1, PA3, PA4, ports PB1, PB3, PB5 to PB7, ports PC2 to PC7, ports PE0 to PE7, port PH7, RES#		$\text{VCC} \times 0.8$	—	$\text{VCC} + 0.3$		
	RIIC input pin (except for SMBus)	V_{IL}	-0.3	—	$\text{VCC} \times 0.3$		
	Other than RIIC input pin		-0.3	—	$\text{VCC} \times 0.2$		
	RIIC input pin (except for SMBus)	ΔV_T	$\text{VCC} \times 0.05$	—	—		
	Other than RIIC input pin		$\text{VCC} \times 0.1$	—	—		
Input voltage (except for Schmitt trigger input pins)	MD	V_{IH}	$\text{VCC} \times 0.9$	—	$\text{VCC} + 0.3$	V	
	XTAL (external clock input)		$\text{VCC} \times 0.8$	—	$\text{VCC} + 0.3$		
	Ports P40 to P44, P46, ports PJ6, PJ7		$\text{AVCC0} \times 0.7$	—	$\text{AVCC0} + 0.3$		
	RIIC input pin (SMBus)		2.1	—	$\text{VCC} + 0.3$		
	MD	V_{IL}	-0.3	—	$\text{VCC} \times 0.1$		
	XTAL (external clock input)		-0.3	—	$\text{VCC} \times 0.2$		
	Ports P40 to P44, P46, ports PJ6, PJ7		-0.3	—	$\text{AVCC0} \times 0.3$		
	RIIC input pin (SMBus)		-0.3	—	0.8		

Table 5.7 DC Characteristics (5) (2/2)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	Low-speed operating mode	Normal operating mode	No peripheral operation*8	ICLK = 32.768 kHz	I _{CC}	4.0	—	μA	
			All peripheral operation: Normal*9, *10	ICLK = 32.768 kHz		11.5	—		
			All peripheral operation: Max.*9, *10	ICLK = 32.768 kHz		—	40		
		Sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		2.2	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		7.1	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		1.8	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		5.3	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to the same frequency as ICLK.

Note 4. Values when VCC = 3.3 V.

Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.

Note 6. Clock supply to the peripheral functions is stopped. The clock source is PLL when ICLK = 12 MHz, and HOCO otherwise. FCLK and PCLK are set to divided by 64.

Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK = 12 MHz, and HOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.

Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.

Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.

Note 10. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to "transition to the module stop state is made".

[256-Kbyte or more flash memory]

Table 5.8 DC Characteristics (6) (1/2)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{SS0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item					Symbol	Typ *4	Max	Unit	Test Conditions				
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz	I _{CC}	3.6	—	mA					
				ICLK = 16 MHz		2.4	—						
				ICLK = 8 MHz		1.8	—						
			All peripheral operation: Normal*3	ICLK = 32 MHz		13.4	—						
				ICLK = 16 MHz		7.5	—						
				ICLK = 8 MHz		4.5	—						
			All peripheral operation: Max.*3	ICLK = 32 MHz		—	27						
		Sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.9	—						
				ICLK = 16 MHz		1.5	—						
				ICLK = 8 MHz		1.3	—						
			All peripheral operation: Normal*3	ICLK = 32 MHz		7.6	—						
				ICLK = 16 MHz		4.4	—						
				ICLK = 8 MHz		2.8	—						
		Deep sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.1	—						
				ICLK = 16 MHz		1.0	—						
				ICLK = 8 MHz		0.9	—						
			All peripheral operation: Normal*3	ICLK = 32 MHz		5.8	—						
				ICLK = 16 MHz		3.4	—						
				ICLK = 8 MHz		2.1	—						
		Increase during flash rewrite*5					2.5			—			
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I _{CC}	2.1	—	mA					
				ICLK = 8 MHz		1.4	—						
				ICLK = 1 MHz		0.8	—						
			All peripheral operation: Normal*7	ICLK = 12 MHz		5.9	—						
				ICLK = 8 MHz		4.2	—						
				ICLK = 1 MHz		1.3	—						
			All peripheral operation: Max.*7	ICLK = 12 MHz		—	12.2						
		Sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.4	—						
ICLK = 8 MHz				0.9		—							
ICLK = 1 MHz				0.7		—							
All peripheral operation: Normal*7			ICLK = 12 MHz	3.6		—							
			ICLK = 8 MHz	2.5		—							
			ICLK = 1 MHz	1.1		—							
Deep sleep mode		No peripheral operation*6	ICLK = 12 MHz	1.1		—							
			ICLK = 8 MHz	0.6		—							
			ICLK = 1 MHz	0.6		—							
		All peripheral operation: Normal*7	ICLK = 12 MHz	2.9		—							
			ICLK = 8 MHz	2.0		—							
			ICLK = 1 MHz	0.9		—							
Increase during flash rewrite*5						2.5	—						

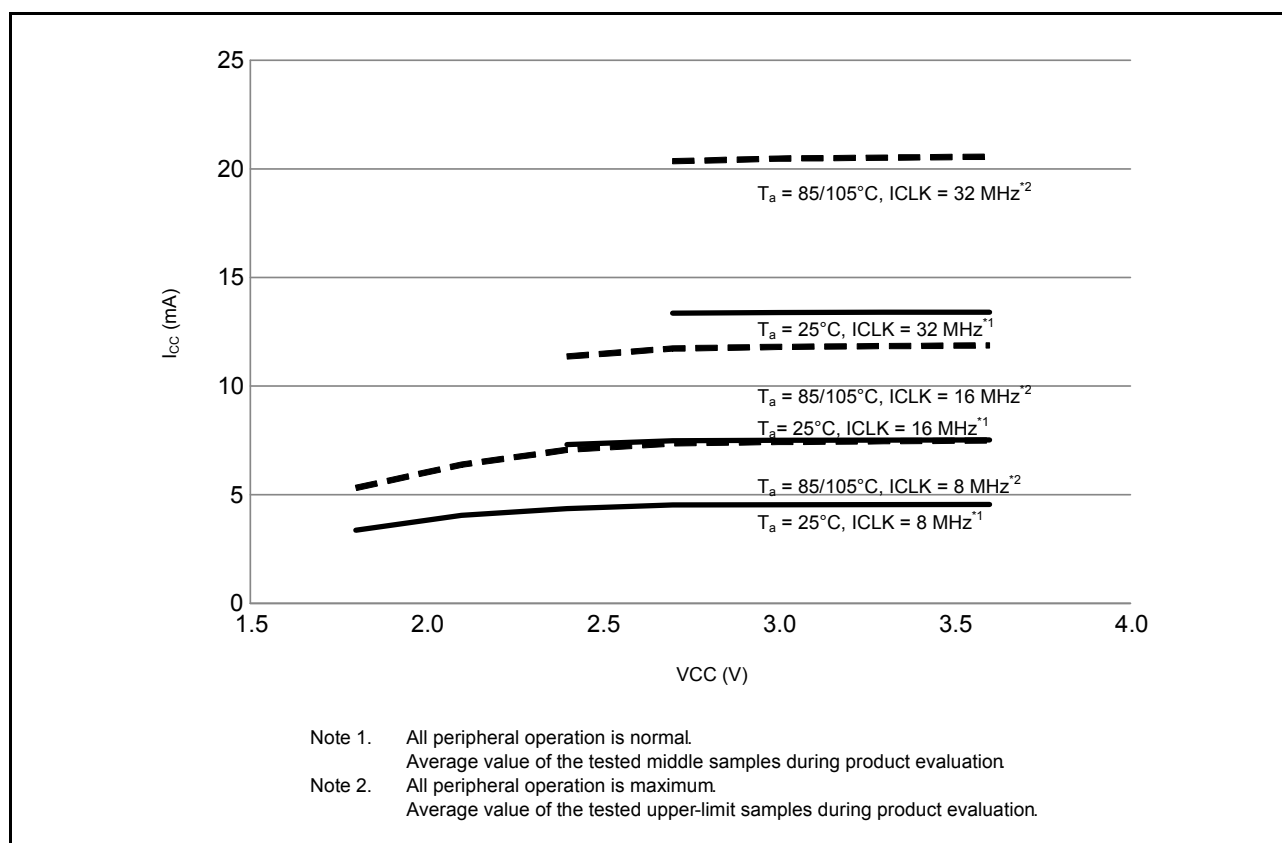


Figure 5.4 Voltage Dependency in High-Speed Operating Mode (Reference Data)

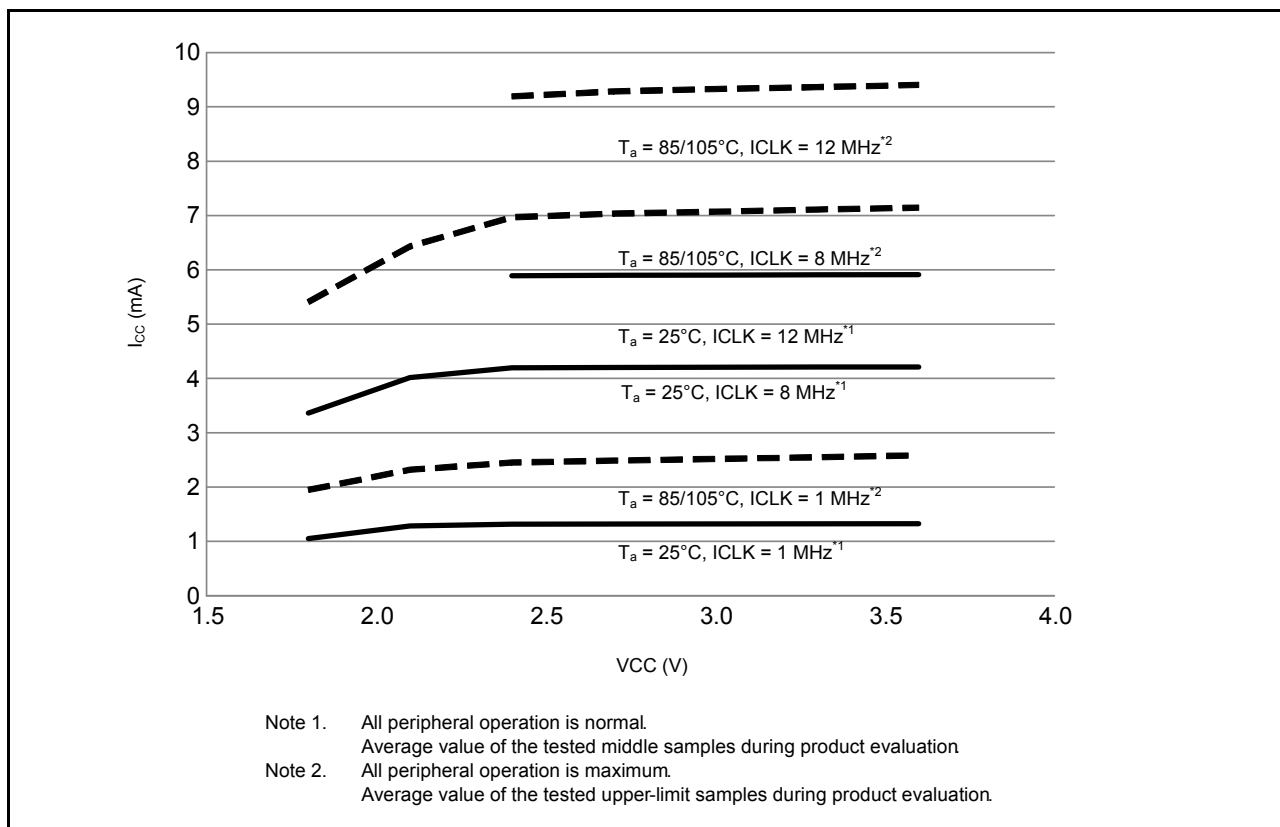


Figure 5.5 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)

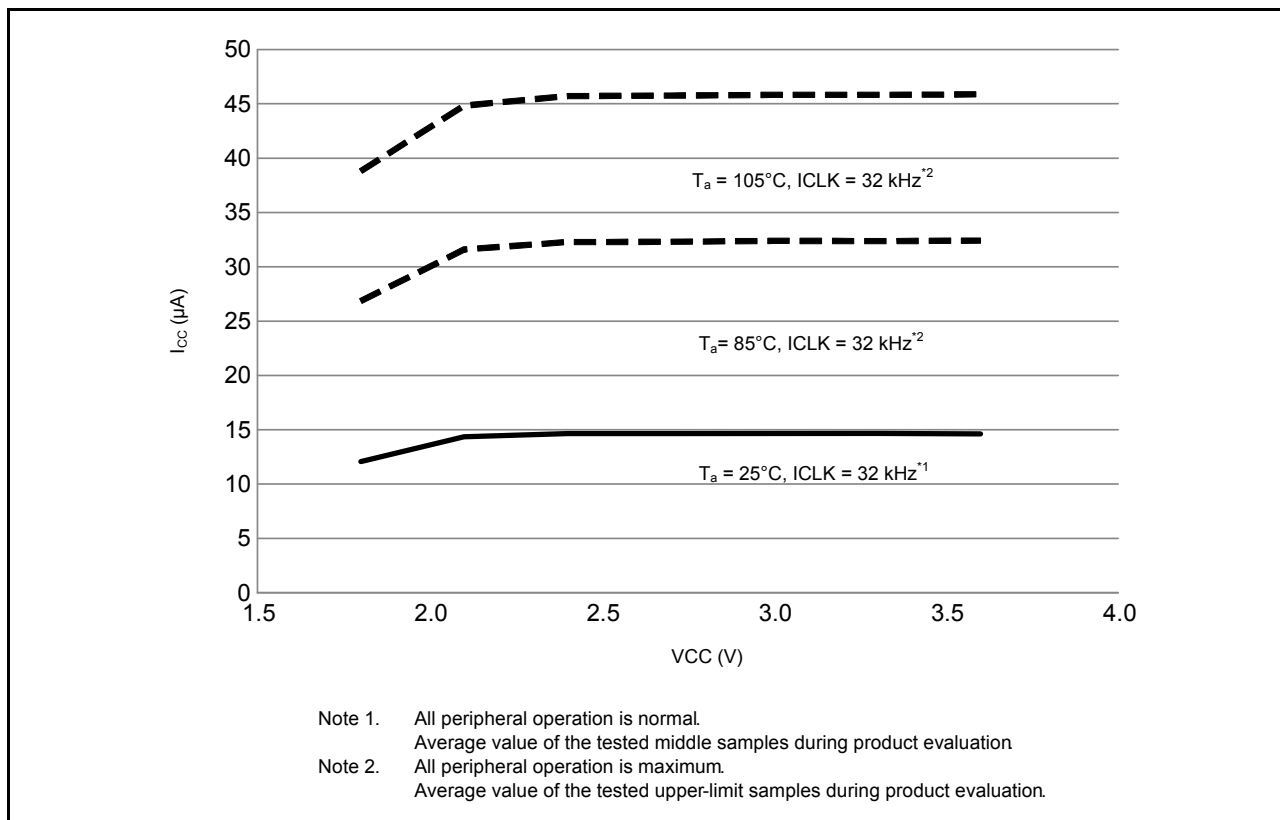


Figure 5.6 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

Table 5.12 DC Characteristics (10)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.*7	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	—	0.7	1.2	mA	
	Waiting for A/D (all units)		—	—	0.3	μA	
	During D/A conversion (per channel)*5		—	—	1.5	mA	
Reference power supply current	During A/D conversion (at high-speed conversion)	I_{REFH0}	—	25	52	μA	
	Waiting for A/D conversion (all units)		—	—	60	nA	
Temperature sensor*6		I_{TEMP}	—	75	—	μA	
LDV1, 2	Per channel	I_{LVD}	—	0.15	—	μA	
USB operating current	During USB communication operation under the following settings and conditions - Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 - Connect peripheral devices via a 1-meter USB cable from the USB port.	I_{USBH}^{*2}	—	4.3 (VCC) 0.9 (VCC_USB) *4	—	mA	
	During USB communication operation under the following settings and conditions - Function controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 - Connect the host device via a 1-meter USB cable from the USB port.	I_{USBF}^{*2}	—	3.6 (VCC) 1.1 (VCC_USB) *4	—	mA	
	During suspended state under the following setting and conditions - Function controller operation is set to full-speed mode (pull up the USB0_DP pin) - Software standby mode - Connect the host device via a 1-meter USB cable from the USB port.	I_{SUSP}^{*3}	—	0.35 (VCC) 170 (VCC_USB) *4	—	μA	

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.

Note 2. Current consumed only by the USB module.

Note 3. Includes the current supplied from the pull-up resistor of the USB0_DP pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.

Note 4. When $\text{VCC} = \text{VCC_USB} = 3.3\text{ V}$.

Note 5. The value of the current flowing to VCC.

Note 6. Current consumed by the power supply (VCC).

Note 7. When $\text{VCC} = \text{AVCC0} = \text{VCC_USB} = 3.3\text{ V}$.**Table 5.13 DC Characteristics (11)**Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.16 to Figure 5.18 show the characteristics of the RIIC output pin.

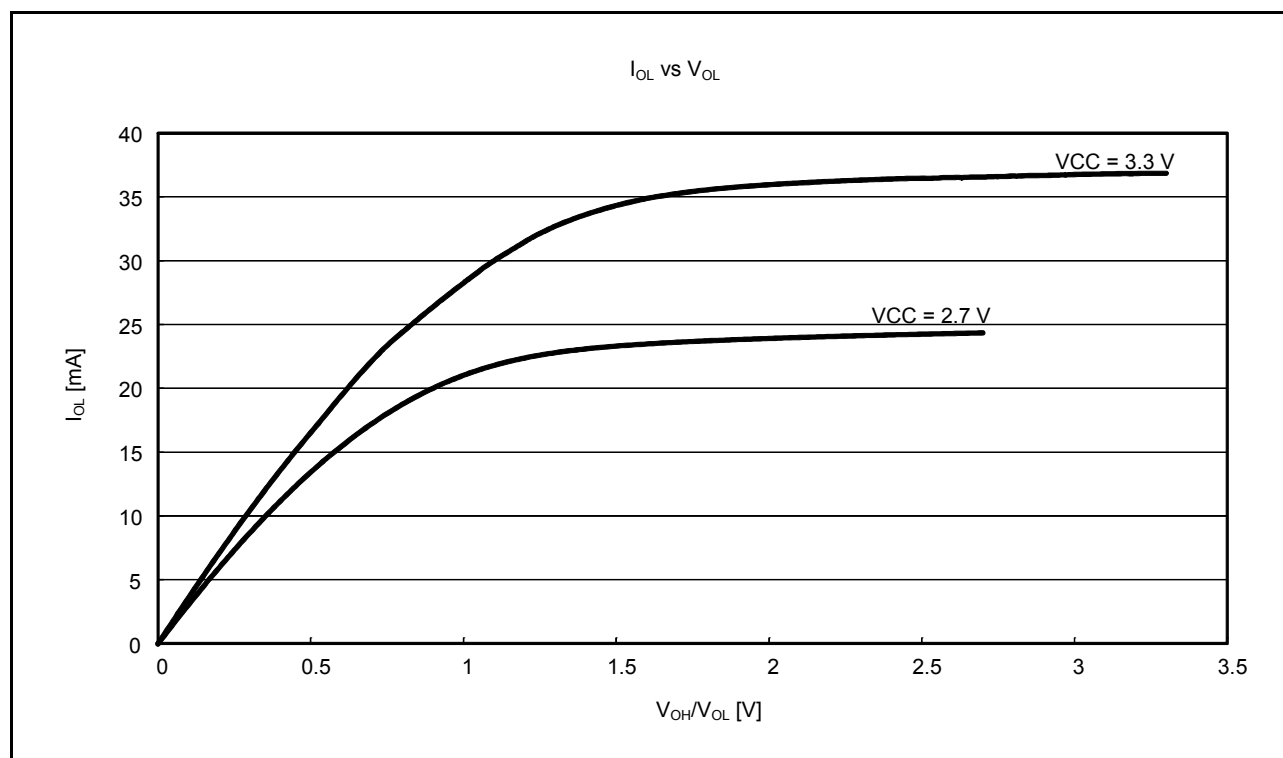


Figure 5.16 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at $T_a = 25^\circ\text{C}$ (Reference Data)

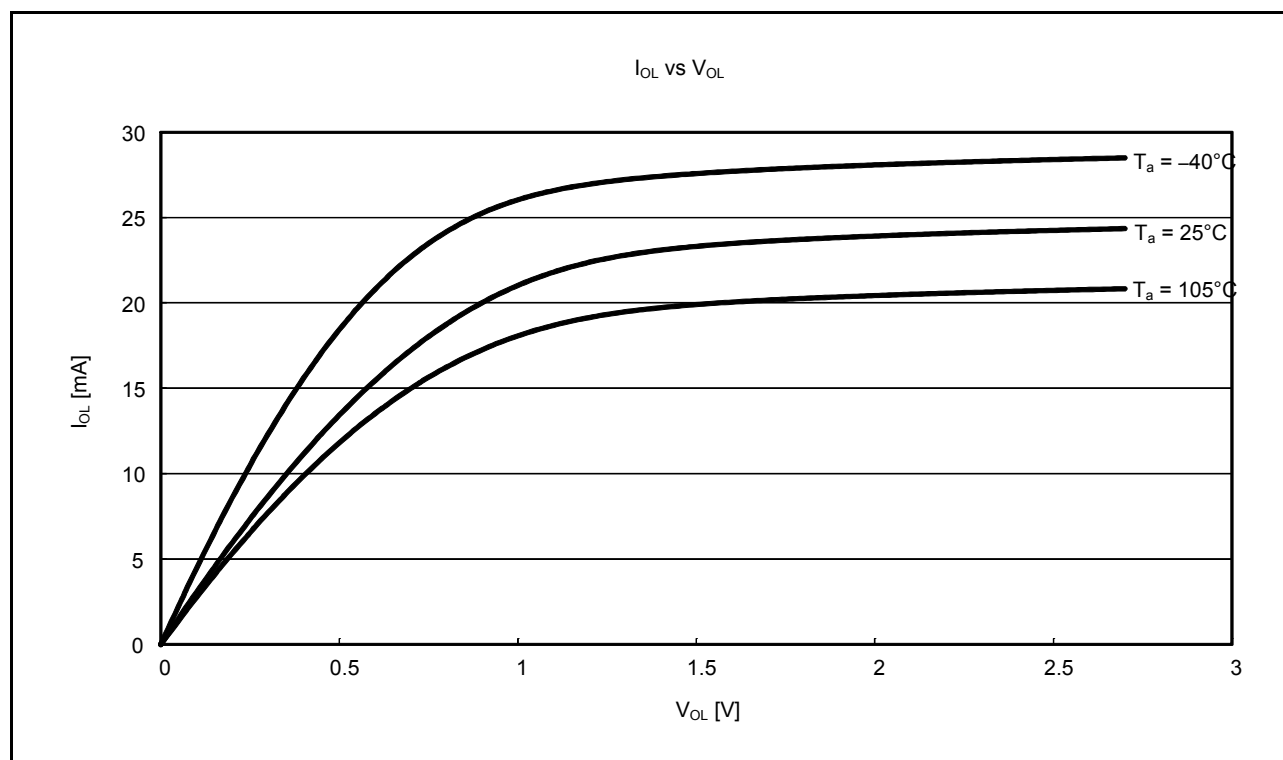


Figure 5.17 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at $V_{CC} = 2.7$ V (Reference Data)

5.3.2 Reset Timing

Table 5.25 Reset Timing

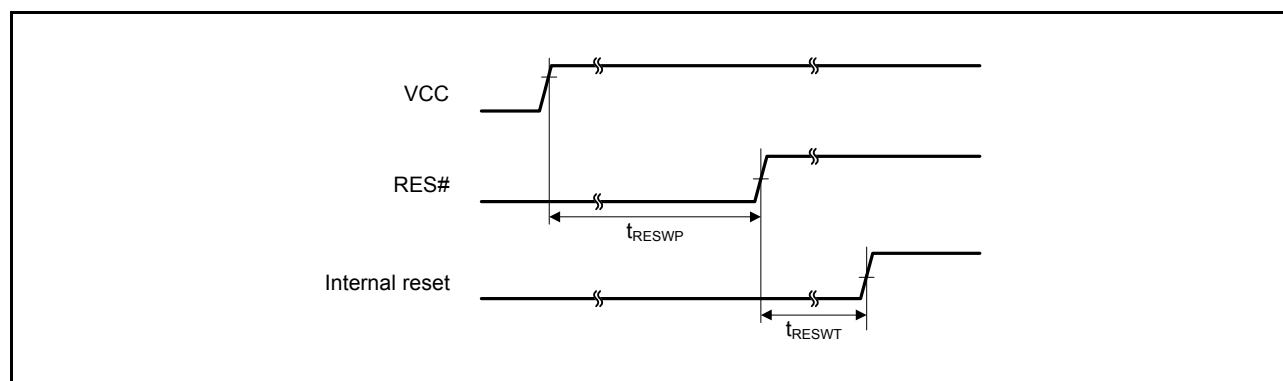
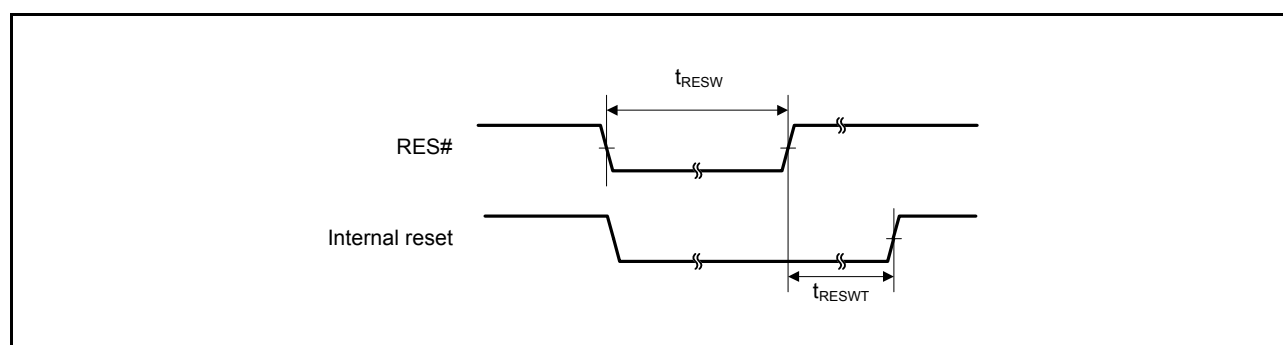
Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 5.31
	Other than above	t_{RESW}	30	—	—	μs	Figure 5.32
Wait time after RES# cancellation (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 5.31
	During fast startup time*2	t_{RESWT}	—	560	—	μs	
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	114	—	μs	Figure 5.32
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 5.33
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*3		t_{RESW2}	—	300	—	μs	
Wait time after software reset cancellation		t_{RESW2}	—	168	—	μs	

Note 1. When $\text{OFS1}.\text{(STUPLVD1REN, FASTSTUP)} = 11\text{b}$.

Note 2. When $\text{OFS1}.\text{(STUPLVD1REN, FASTSTUP)} \neq 11\text{b}$.

Note 3. When $\text{IWDTCCR.CKS}[3:0] = 0000\text{b}$.

**Figure 5.31 Reset Input Timing at Power-On****Figure 5.32 Reset Input Timing (1)**

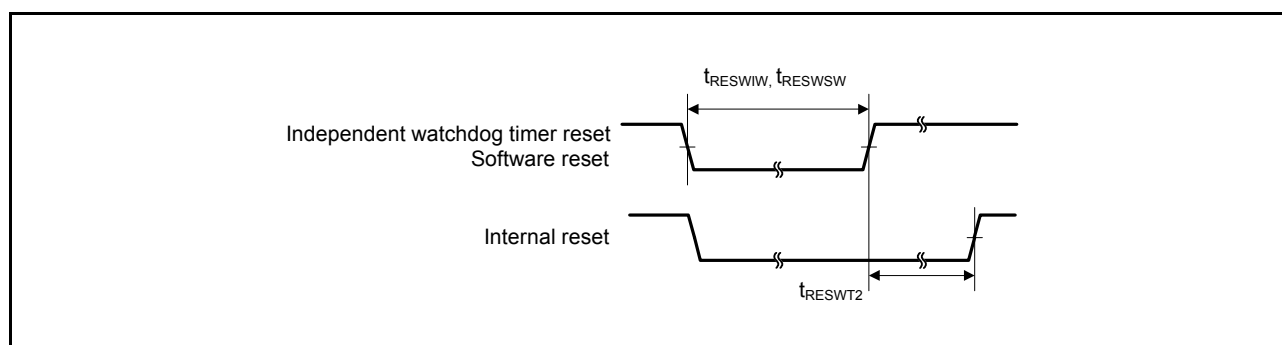
**Figure 5.33** Reset Input Timing (2)

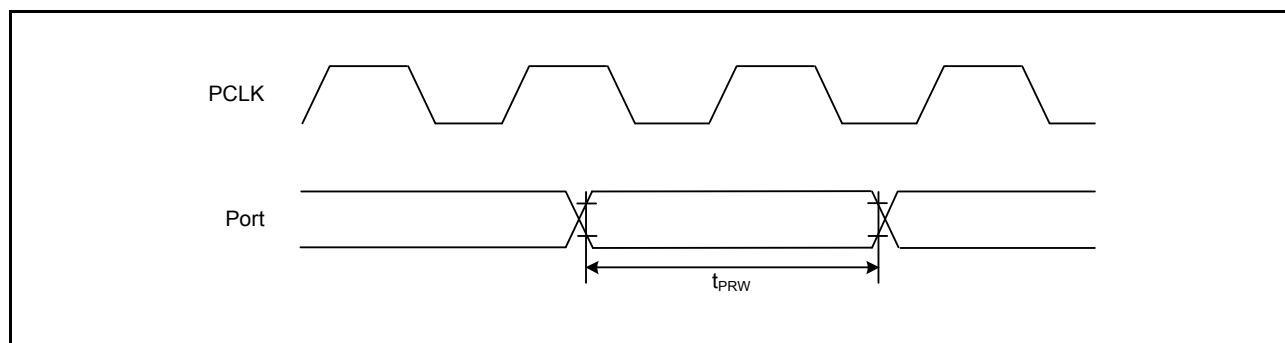
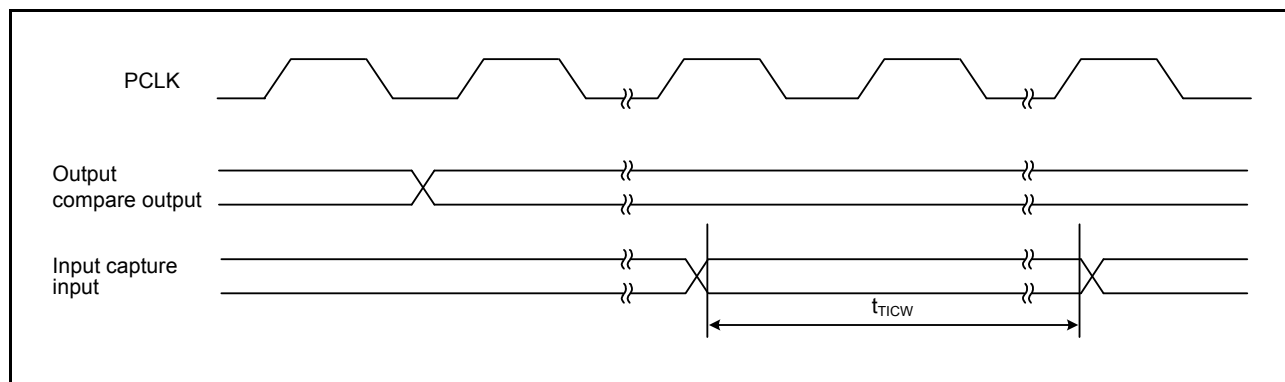
Table 5.36 Timing of On-Chip Peripheral Modules (5)

Conditions: $2.7\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $2.7\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $fPCLKB \leq 32\text{ MHz}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Max.	Unit	Test Conditions
Simple I ² C (Standard mode)	SDA0 input rise time	t_{Sr}	—	1000	ns
	SDA0 input fall time	t_{Sf}	—	300	ns
	SDA0 input spike pulse removal time	t_{SP}	0	$4 \times t_{pcyc}^{*1}$	ns
	Data input setup time	t_{SDAS}	250	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL0, SDA0 capacitive load	C_b	—	400	pF
Simple I ² C (Fast mode)	SCL0, SDA0 input rise time	t_{Sr}	—	300	ns
	SCL0, SDA0 input fall time	t_{Sf}	—	300	ns
	SCL0, SDA0 input spike pulse removal time	t_{SP}	0	$4 \times t_{pcyc}^{*1}$	ns
	Data input setup time	t_{SDAS}	100	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL0, SDA0 capacitive load	C_b	—	400	pF

Note: • t_{pcyc} : PCLK cycle

Note 1. This applies when the SMR.CKS[1:0] bits = 00b and the SNFR.NFCS[2:0] bits = 010b while the SNFR.NFE bit = 1 and the digital filter is enabled.

**Figure 5.38 I/O Port Input Timing****Figure 5.39 MTU2 Input/Output Timing**

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

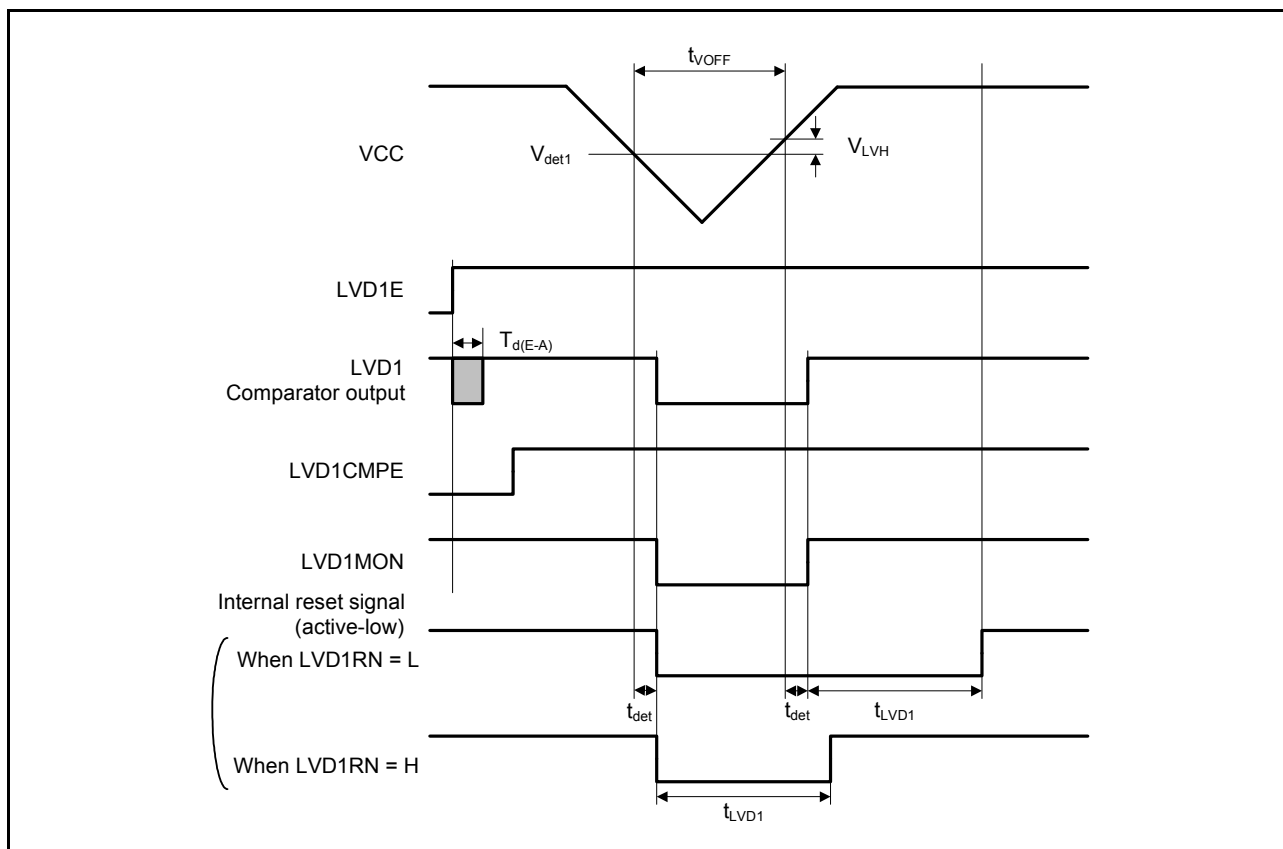
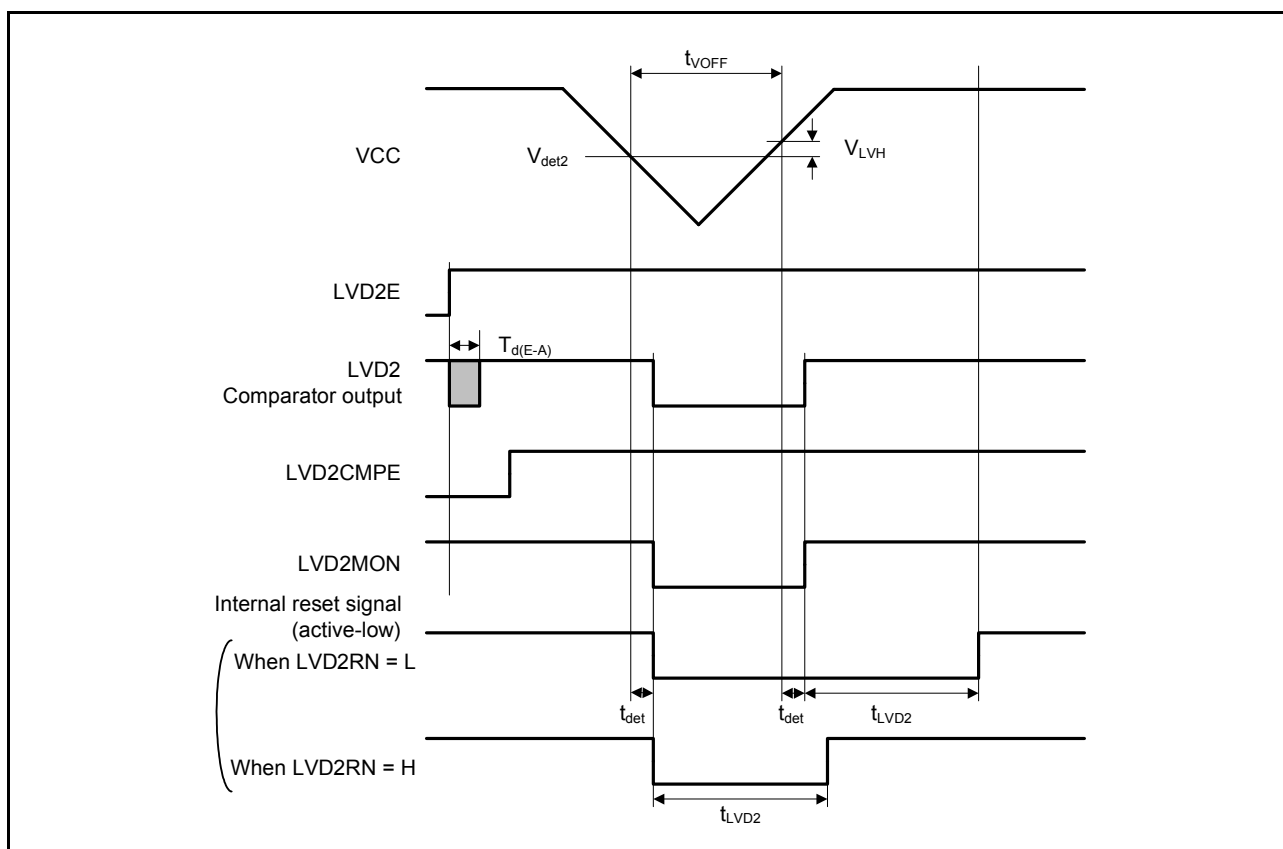
Figure 5.60 Voltage Detection Circuit Timing (V_{det1})Figure 5.61 Voltage Detection Circuit Timing (V_{det2})

Table 5.50 ROM (Flash Memory for Code Storage) Characteristics (3)Middle-speed operating mode Conditions: $1.8\text{ V} \leq \text{VCC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$ Temperature range for the programming/erasure operation: $T_a = -40$ to $+85^\circ\text{C}$

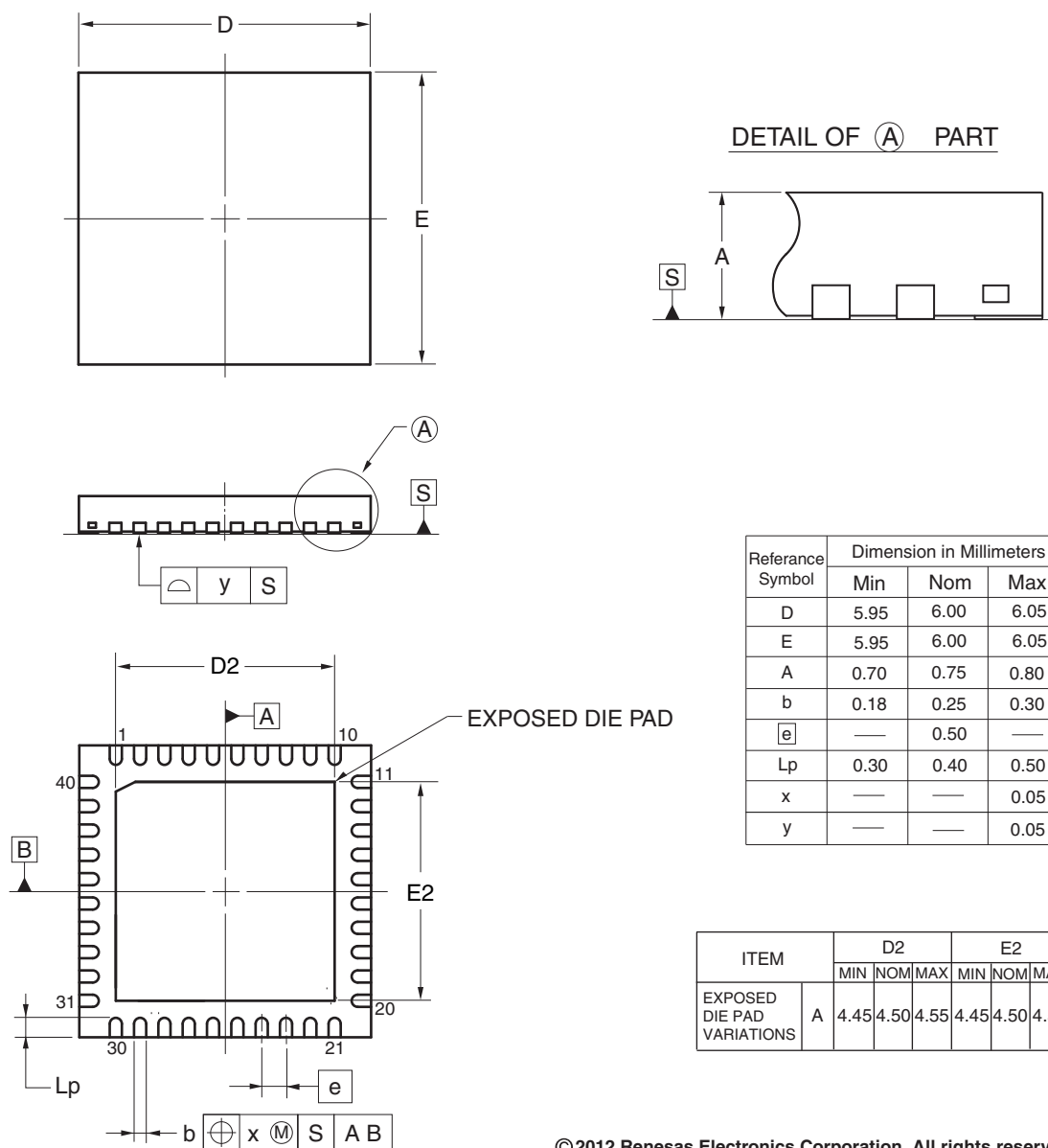
Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4-byte	t_{P4}	—	143	1330	—	96.8	932	μs
Erasure time	1-Kbyte	t_{E1K}	—	8.3	269	—	5.85	219	ms
	256-Kbyte	t_{E256K}	—	407	928	—	93	520	ms
Blank check time	4-byte	t_{BC4}	—	—	78	—	—	50	μs
	1-Kbyte	t_{BC1K}	—	—	1.61	—	—	0.369	ms
Erase operation forcible stop time		t_{SED}	—	—	33.6	—	—	25.6	μs
Start-up area switching setting time		t_{SAS}	—	13.2	549	—	7.6	445	ms
Access window time		t_{AWS}	—	13.2	549	—	7.6	445	ms
ROM mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	μs
ROM mode transition wait time 2		t_{MS}	3	—	—	3	—	—	μs

Note: • Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: • The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: • The frequency accuracy of FCLK should be $\pm 3.5\%$. Confirm the frequency accuracy of the clock source.

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-4	0.09



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Figure F 40-Pin HWQFN (PWQN0040KC-A)