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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, SCI, SPI, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51117adfm-3a

Table 1.7 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC)	Communication (SCle, SCIf, RSPI, RIIC, USB)	Others
1		P27	MTIOC2B	SCK1/SCK12	IRQ3/CMPA2/CACREF/ADTRG0#
2		P26	MTIOC2A	TXD1/SMOSI1/SSDA1/USB0_VBUSEN	
3	MD				FINED
4	RES#				
5	XCOUT				
6	XCIN	PH7			
7	UPSEL	P35			NMI
8	XTAL				
9	EXTAL				
10	VCL				
11	VSS				
12	VCC				
13		P17	MTIOC0C/MTIOC3A/MTIOC3B/POE8#	SCK1/MISOA/SDA0/RXD12/RXD12/SMISO12/SSCL12	IRQ7
14		P16	MTIOC3C/MTIOC3D/RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL0/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB	IRQ6/ADTRG0#
15		P15	MTIOC0B/MTCLKB	RXD1/SMISO1/SSCL1/RSPCKA	IRQ5/CLKOUT
16	UB#	P14	MTIOC0A/MTIOC3A/MTCLKA	CTS1#/RTS1#/SS1#/SSLA0/TXD12/TXD12/SIOX12/SMOSI12/SSDA12/USB0_OVRCURA	IRQ4
17	VCC_USB				
18				USB0_DM	
19				USB0_DP	
20	VSS_USB				
21		PC7	MTIOC3A/MTCLKB	TXD1/SMOSI1/SSDA1/MISOA/USB0_OVRCURB	CACREF
22		PC6	MTIOC3C/MTCLKA	RXD1/SMISO1/SSCL1/MOSIA/USB0_EXICEN	
23		PC5	MTIOC3B/MTCLKD	SCK1/RSPCKA/USB0_ID	
24		PC4	MTIOC3D/MTCLKC/POE0#	SCK5/SSLA0/USB0_VBUS*1/USB0_VBUSEN	IRQ2/CLKOUT
25		PB5/PC3	MTIOC2A/MTIOC1B/POE1#		
26		PB3/PC2	MTIOC0A/MTIOC3B/MTIOC4A/POE3#	USB0_OVRCURA	
27		PB1/PC1	MTIOC0C/MTIOC4C		IRQ4
28	VCC				
29		PB0/PC0	MTIC5W/MTIOC0C/RTCOUT	SCL0/RSPCKA	IRQ2/ADTRG0#
30	VSS				
31		PA6	MTIC5V/MTCLKB/MTIOC2A/POE2#	CTS5#/RTS5#/SS5#/SDA0/MOSIA	IRQ3
32		PA4	MTIC5U/MTCLKA/MTIOC2B	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
33		PA3	MTIOC0D/MTCLKD/MTIOC1B/POE0#	RXD5/SMISO5/SSCL5/MISOA	IRQ6
34		PA1	MTIOC0B/MTCLKC/RTCOUT	SCK5/SSLA2	
35		PE4	MTIOC4D/MTIOC1A/MTIOC3A	MOSIA	IRQ4/AN012
36		PE3	MTIOC0A/MTIOC1B/MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/RSPCKA	IRQ3/AN011
37		PE2	MTIOC4A	RXD12/RXD12/SMISO12/SSCL12	IRQ7/AN010
38		PE1	MTIOC4C	TXD12/TXD12/SIOX12/SMOSI12/SSDA12	IRQ1/AN009

Table 1.7 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC)	Communication (SCle, SCIf, RSPI, RIIC, USB)	Others
39		PE0	MTIOC2A/POE3#	SCK12	IRQ0/AN008
40		PE7			IRQ7/AN015
41		P46*2			AN006
42		P42*2			AN002
43		P41*2			AN001
44	VREFL0	PJ7*2			
45		P40*2			AN000
46	VREFH0	PJ6*2			
47	AVSS0				
48	AVCC0				

Note 1. Not 5 V tolerant.

Note 2. The power source of the I/O buffer for these pins is AVCC0.

Table 1.9 List of Pins and Pin Functions (36-Pin WFLGA)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC)	Communication (SCle, SCIf, RSPI, RiIC, USB)	Others
A1	AVSS0				
A2	AVCC0				
A3	VREFH0	PJ6*2			
A4		P42*2			AN002
A5		P41*2			AN001
A6		PE2	MTIOC4A	RXD12/RXD12/SMISO12/SSCL12	IRQ7/AN010
B1	RES#				
B2		P27	MTIOC2B	SCK1/SCK12	IRQ3/CMPA2/CACREF/ADTRG0#
B3	VREFL0	PJ7*2			
B4		PE0	MTIOC2A/POE3#	SCK12	IRQ0/AN008
B5		PE1	MTIOC4C	TXD12/TXD12/SIOX12/SMOSI12/SSDA12	IRQ1/AN009
B6		PA3	MTIOC0D/MTCLKD/MTIOC1B/POE0#	RXD5/SMISO5/SSCL5/MISOA	IRQ6
C1	XTAL				
C2	MD				FINED
C3		PE3	MTIOC0A/MTIOC1B/MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/RSPCKA	IRQ3/AN011
C4		PE4	MTIOC1A/MTIOC3A/MTIOC4D	MOSIA	IRQ4/AN012
C5		PA4	MTIOC2B/MTIC5U/MTCLKA	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5
C6	VSS				
D1	EXTAL				
D2	UPSEL	P35			NMI
D3	UB#	P14	MTIOC0A/MTIOC3A/MTCLKA	CTS1#/RTS1#/SS1#/SSLA0/TXD12/TXD12/SIOX12/SMOSI12/SSDA12/USB0_OVRCURA	IRQ4
D4		PA6	MTIC5V/MTCLKB/MTIOC2A/POE2#	CTS5#/RTS5#/SS5#/SDA0/MOSIA	IRQ3
D5		PB3	MTIOC0A/MTIOC3B/MTIOC4A/POE3#	USB0_OVRCURA	
D6		PB0	MTIOC0C/MTIC5W	SCL0/RSPCKA	IRQ2/ADTRG0#
E1	VCL				
E2		P17	MTIOC0C/MTIOC3A/MTIOC3B/POE8#	SCK1/MISOA/SDA0/RXD12/RXD12/SMISO12/SSCL12	IRQ7
E3		P16	MTIOC3C/MTIOC3D	TXD1/SMOSI1/SSDA1/SCL0/MOSIA/USB0_VBUSEN/USB0_OVRCURB/USB0_VBUS	IRQ6/ADTRG0#
E4		P15	MTIOC0B/MTCLKB	RXD1/SMISO1/SSCL1/RSPCKA	IRQ5/CLKOUT
E5		PC4	MTIOC3D/MTCLKC/POE0#	SCK5/SSLA0/USB0_VBUSEN/USB0_VBUS*1	IRQ2/CLKOUT
E6	VCC				
F1	VSS				
F2	VCC				
F3	VCC_USB				
F4				USB0_DM	
F5				USB0_DP	
F6	VSS_USB				

Note 1. Not 5 V tolerant.

Note 2. The power source of the I/O buffer for these pins is AVCC0.

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory map.

Table 4.1 List of I/O Registers (Address Order) (9/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 88A2h	MTU5	Timer General Register W	TGRW	16	16	2 or 3 PCLKB
0008 88A4h	MTU5	Timer Control Register W	TCRW	8	8	2 or 3 PCLKB
0008 88A6h	MTU5	Timer I/O Control Register W	TIORW	8	8	2 or 3 PCLKB
0008 88B2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 88B4h	MTU5	Timer Start Register	TSTR	8	8	2 or 3 PCLKB
0008 88B6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	2 or 3 PCLKB
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9004h	S12AD	A/D Channel Select Register A	ADANSA	16	16	2 or 3 PCLKB
0008 9008h	S12AD	A/D-Converted Value Addition Mode Select Register	ADADS	16	16	2 or 3 PCLKB
0008 900Ch	S12AD	A/D-Converted Value Addition Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9010h	S12AD	A/D Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9012h	S12AD	A/D Converted Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9014h	S12AD	A/D Channel Select Register B	ADANSB	16	16	2 or 3 PCLKB
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSRDR	16	16	2 or 3 PCLKB
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 9030h	S12AD	A/D Data Register 8	ADDR8	16	16	2 or 3 PCLKB
0008 9032h	S12AD	A/D Data Register 9	ADDR9	16	16	2 or 3 PCLKB
0008 9034h	S12AD	A/D Data Register 10	ADDR10	16	16	2 or 3 PCLKB
0008 9036h	S12AD	A/D Data Register 11	ADDR11	16	16	2 or 3 PCLKB
0008 9038h	S12AD	A/D Data Register 12	ADDR12	16	16	2 or 3 PCLKB
0008 903Ah	S12AD	A/D Data Register 13	ADDR13	16	16	2 or 3 PCLKB
0008 903Ch	S12AD	A/D Data Register 14	ADDR14	16	16	2 or 3 PCLKB
0008 903Eh	S12AD	A/D Data Register 15	ADDR15	16	16	2 or 3 PCLKB
0008 9060h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 9061h	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 9070h	S12AD	A/D Sampling State Register T	ADSSTRT	8	8	2 or 3 PCLKB
0008 9071h	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB
0008 9073h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 9074h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 9075h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 9076h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB
0008 9078h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (10/16)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A029h	SCI1	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A02Ah	SCI1	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A02Bh	SCI1	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A02Ch	SCI1	I ² C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A0A6h	SCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A0A9h	SCI5	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A0AAh	SCI5	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A0ABh	SCI5	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A0ACh	SCI5	I ² C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2 or 3 PCLKB
0008 B102h	ELC	Event Link Setting Register 1	ELSR1	8	8	2 or 3 PCLKB
0008 B103h	ELC	Event Link Setting Register 2	ELSR2	8	8	2 or 3 PCLKB
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2 or 3 PCLKB
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2 or 3 PCLKB
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2 or 3 PCLKB
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2 or 3 PCLKB
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2 or 3 PCLKB
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2 or 3 PCLKB
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2 or 3 PCLKB
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2 or 3 PCLKB
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2 or 3 PCLKB
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2 or 3 PCLKB
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2 or 3 PCLKB
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2 or 3 PCLKB
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2 or 3 PCLKB
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2 or 3 PCLKB
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2 or 3 PCLKB

Table 5.7 DC Characteristics (5) (2/2)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	Low-speed operating mode	Normal operating mode	No peripheral operation*8	ICLK = 32.768 kHz	I _{CC}	4.0	—	μA	
			All peripheral operation: Normal*9, *10	ICLK = 32.768 kHz		11.5	—		
			All peripheral operation: Max.*9, *10	ICLK = 32.768 kHz		—	40		
		Sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		2.2	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		7.1	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		1.8	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		5.3	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to the same frequency as ICLK.

Note 4. Values when VCC = 3.3 V.

Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.

Note 6. Clock supply to the peripheral functions is stopped. The clock source is PLL when ICLK = 12 MHz, and HOCO otherwise. FCLK and PCLK are set to divided by 64.

Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK = 12 MHz, and HOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.

Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.

Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.

Note 10. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to "transition to the module stop state is made".

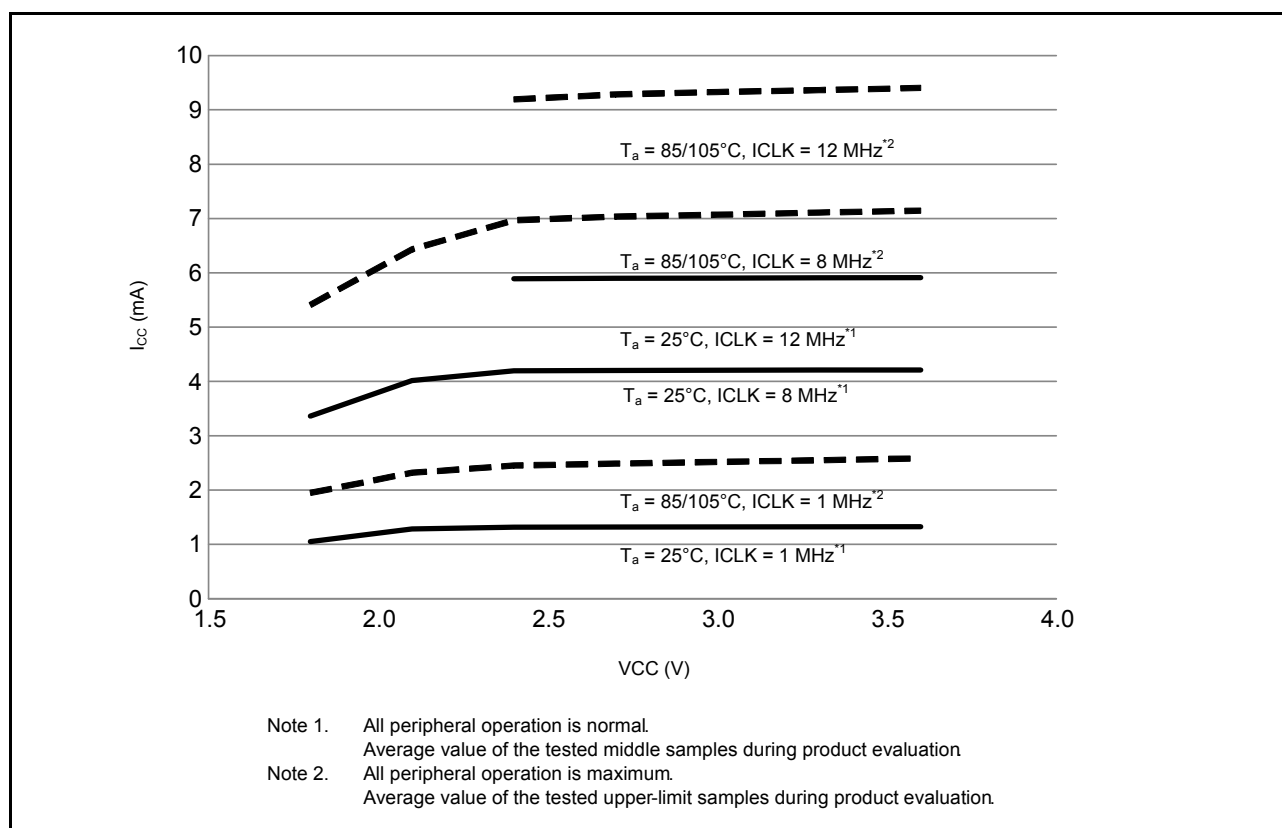


Figure 5.5 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)

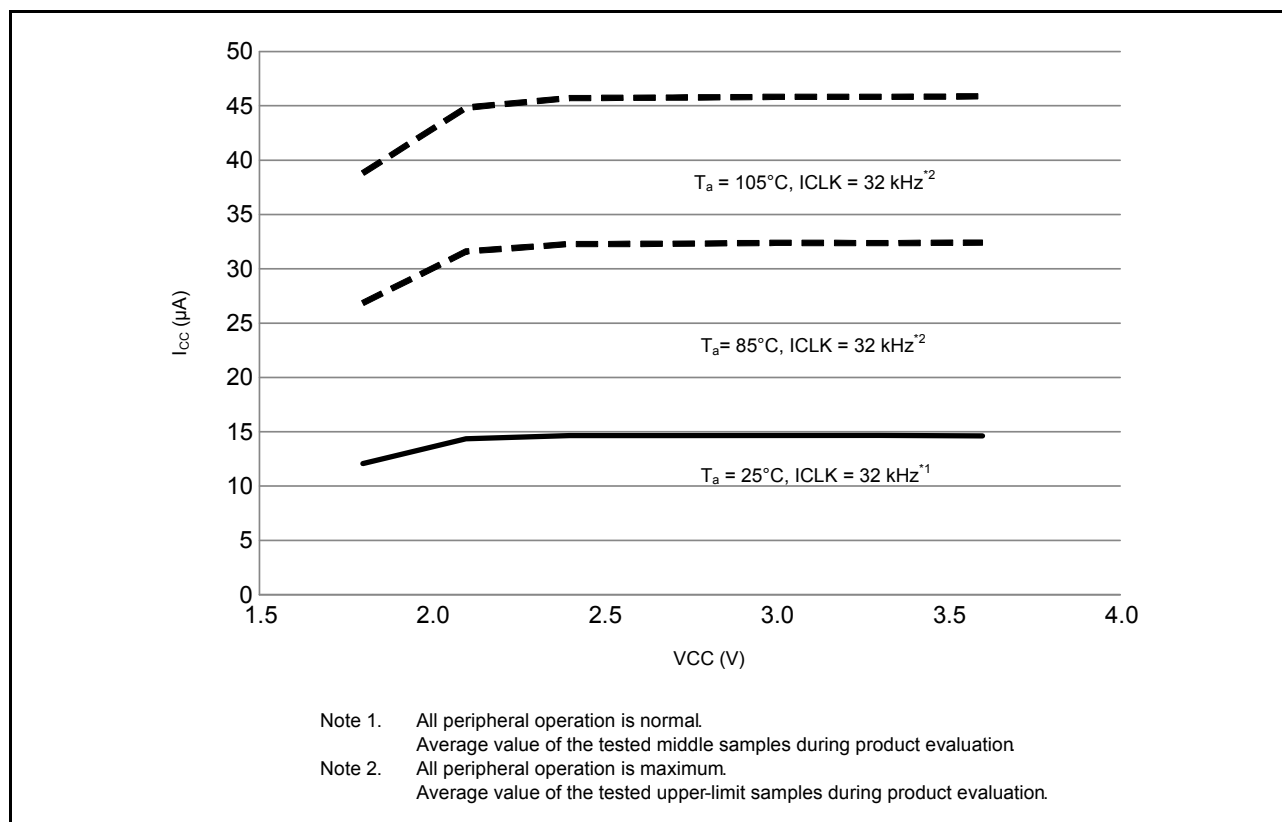


Figure 5.6 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

[128-Kbyte or less flash memory]

Table 5.9 DC Characteristics (7)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	$T_a = 25^\circ\text{C}$	I_{CC}	0.35	0.53	
		$T_a = 55^\circ\text{C}$		0.58	1.45	
		$T_a = 85^\circ\text{C}$		1.60	7.30	
		$T_a = 105^\circ\text{C}$		3.30	16.50	
	Increment for RTC operation*4		0.31	—		RCR3.RTCDV[2:0] = 010b
			1.09	—		RCR3.RTCDV[2:0] = 100b
	Increment for IWDG operation		0.37	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. The IWDG and LVD are stopped.

Note 3. $\text{VCC} = 3.3\text{ V}$.

Note 4. Includes the oscillation circuit.

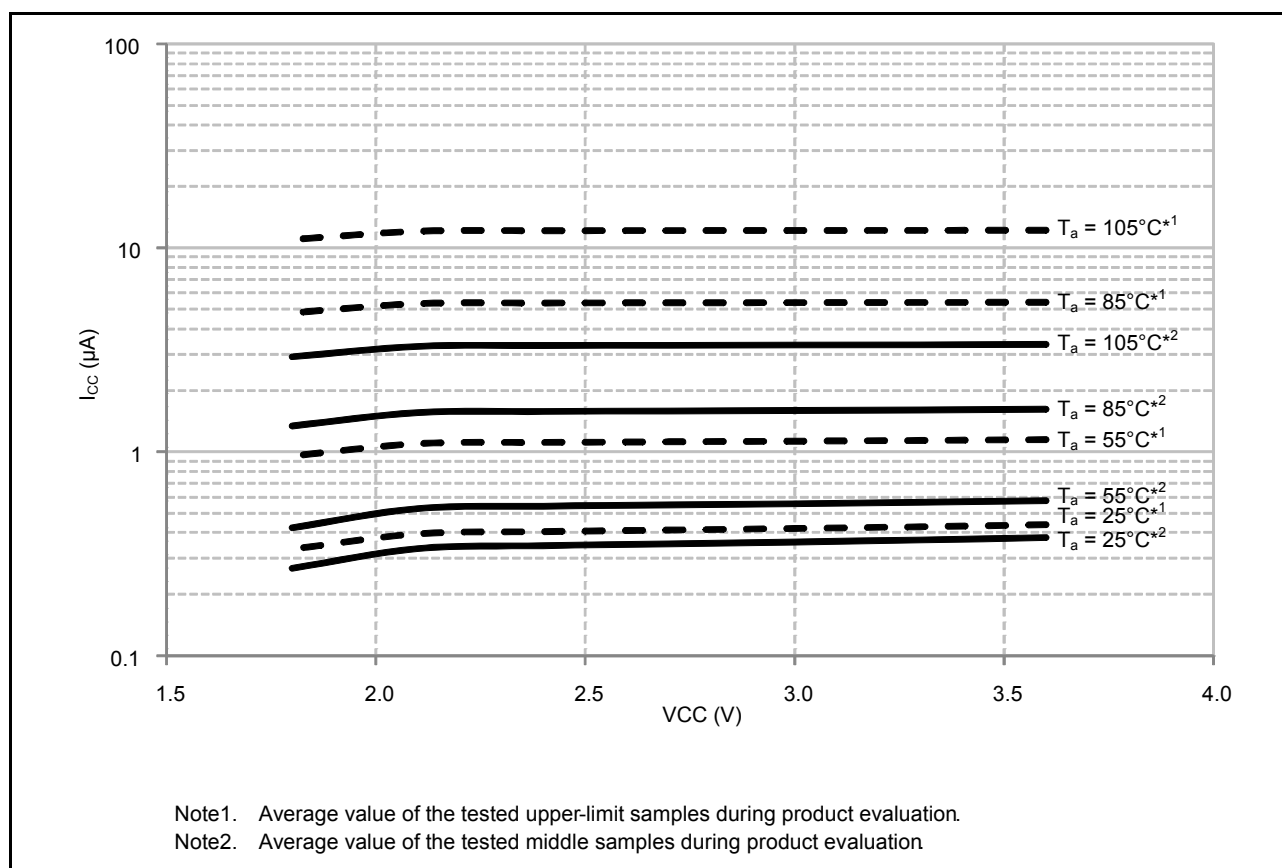
**Figure 5.7 Voltage Dependency in Software Standby Mode (Reference Data)**

Table 5.17 Permissible Output Currents (1)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $T_a = -40\text{ to }+85^\circ\text{C}$ (D version)

Item		Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7	I_{OL}	0.4	mA
	Ports other than above		8.0	
Permissible output low current (maximum value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7		0.4	
	Ports other than above		8.0	
Permissible output low current	Total of ports P40 to P44, P46, ports PJ6, PJ7	ΣI_{OL}	2.4	
	Total of ports P03, P05, ports P26, P27, ports P30, P31		30	
	Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7		30	
	Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7		30	
	Total of all output pins		60	
Permissible output high current (average value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7	I_{OH}	-0.1	
	Ports other than above		-4.0	
Permissible output high current (maximum value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7		-0.1	
	Ports other than above		-4.0	
Permissible output high current	Total of ports P40 to P44, P46, ports PJ6, PJ7	ΣI_{OH}	-0.6	
	Total of ports P03, P05, ports P26, P27, ports P30, P31		-10	
	Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7		-15	
	Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7		-15	
	Total of all output pins		-40	

Note: Do not exceed the permissible total supply current.

Table 5.18 Permissible Output Currents (2)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$ (G version)

Item		Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7	I_{OL}	0.4	mA
	Ports other than above		8.0	
Permissible output low current (maximum value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7		0.4	
	Ports other than above		8.0	
Permissible output low current	Total of ports P40 to P44, P46, ports PJ6, PJ7	ΣI_{OL}	1.6	
	Total of ports P03, P05, ports P26, P27, ports P30, P31		20	
	Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7		20	
	Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7		20	
	Total of all output pins		40	
Permissible output high current (average value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7	I_{OH}	-0.1	
	Ports other than above		-4.0	
Permissible output high current (maximum value per pin)	Ports P40 to P44, P46, ports PJ6, PJ7		-0.1	
	Ports other than above		-4.0	
Permissible output high current	Total of ports P40 to P44, P46, ports PJ6, PJ7	ΣI_{OH}	-0.6	
	Total of ports P03, P05, ports P26, P27, ports P30, P31		-10	
	Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7		-15	
	Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7		-15	
	Total of all output pins		-40	

Note: Do not exceed the permissible total supply current.

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.16 to Figure 5.18 show the characteristics of the RIIC output pin.

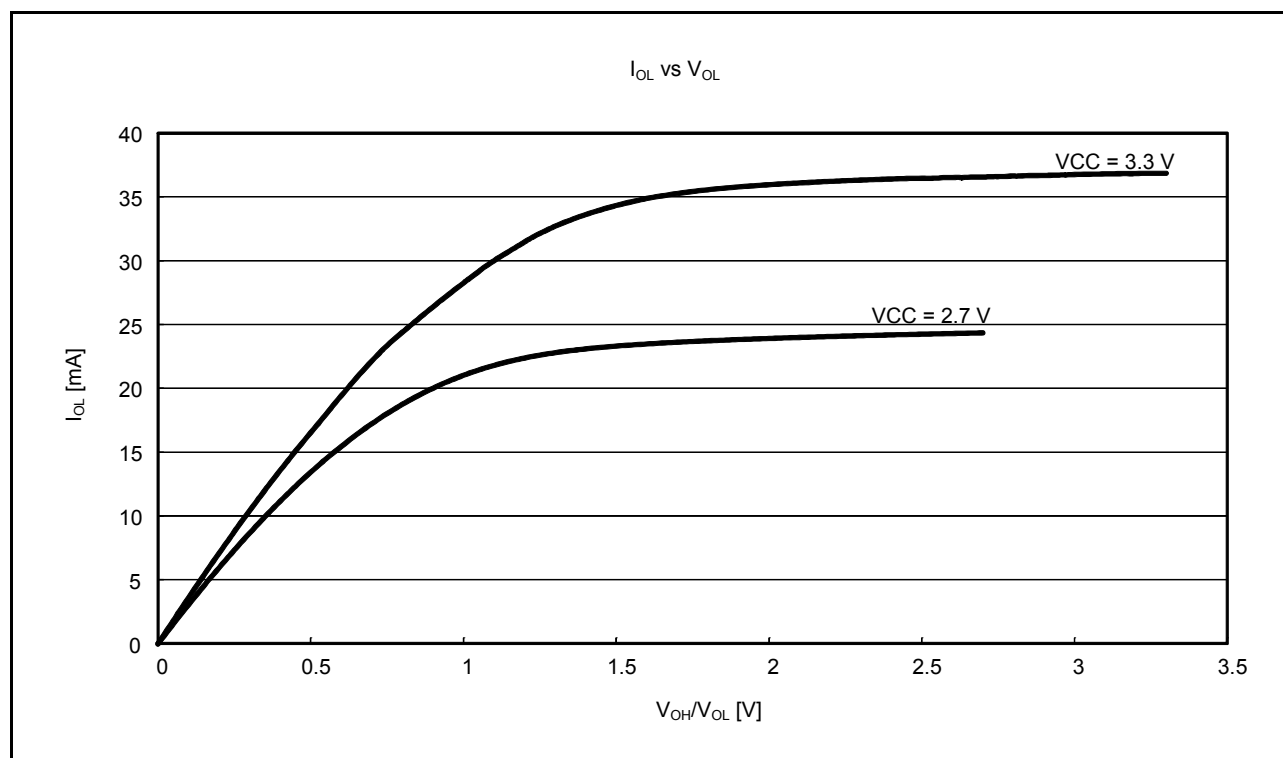


Figure 5.16 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at $T_a = 25^\circ\text{C}$ (Reference Data)

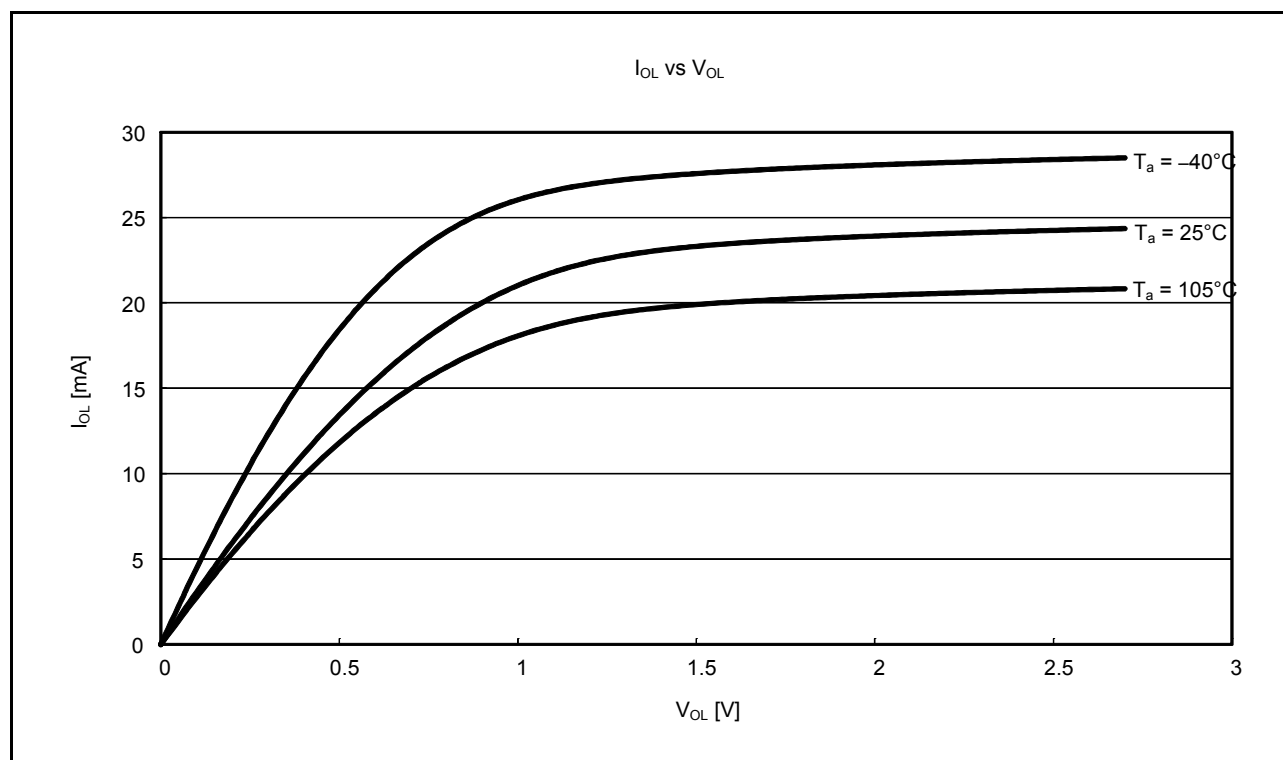


Figure 5.17 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at $V_{CC} = 2.7$ V (Reference Data)

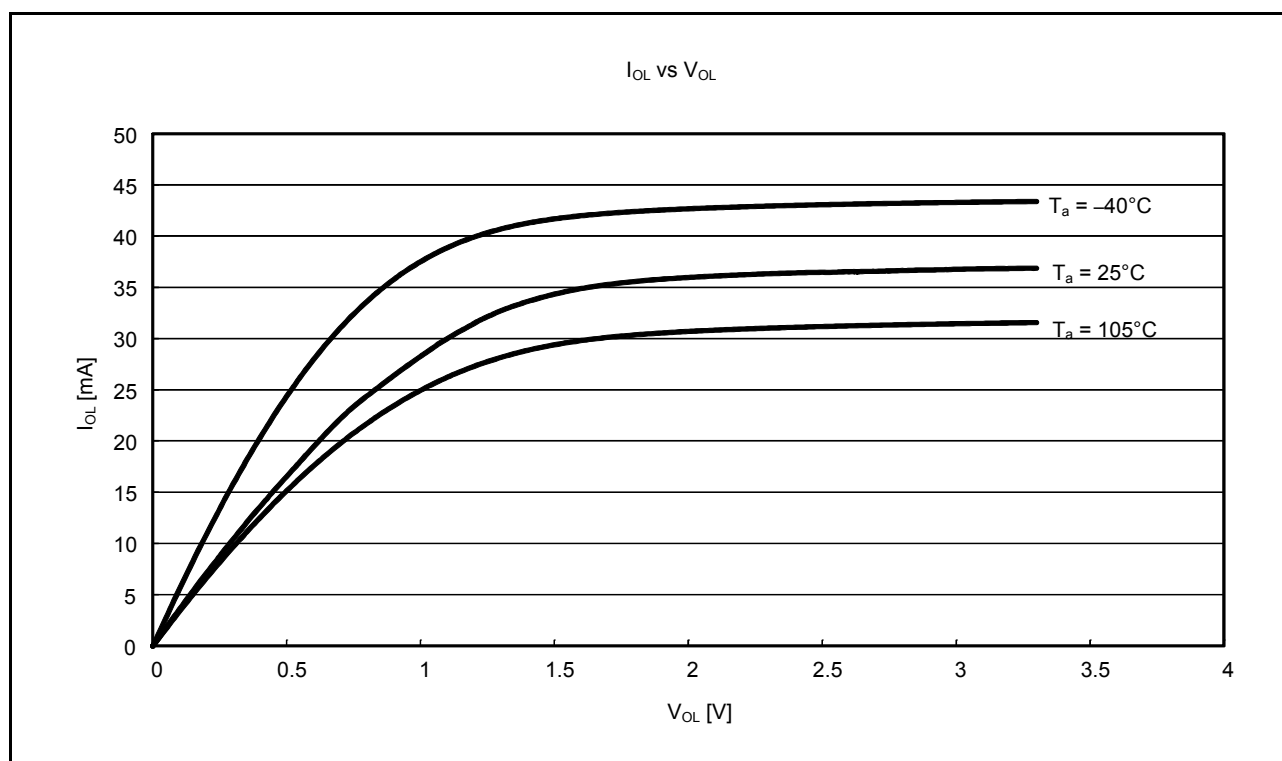


Figure 5.18 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at $V_{CC} = 3.3$ V (Reference Data)

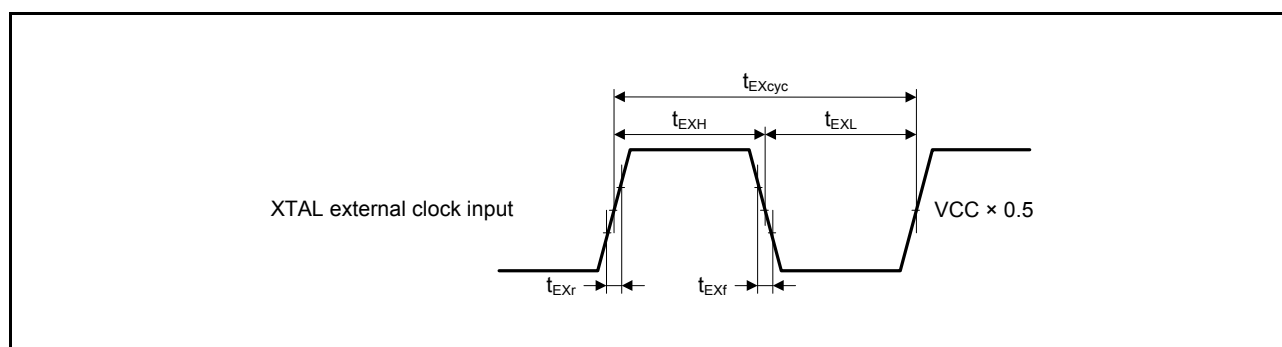


Figure 5.23 XTAL External Clock Input Timing

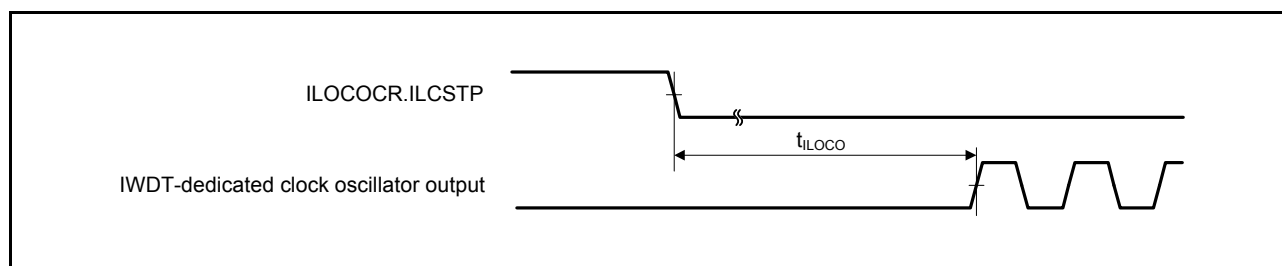


Figure 5.24 IWDt-Dedicated Clock Oscillation Start Timing

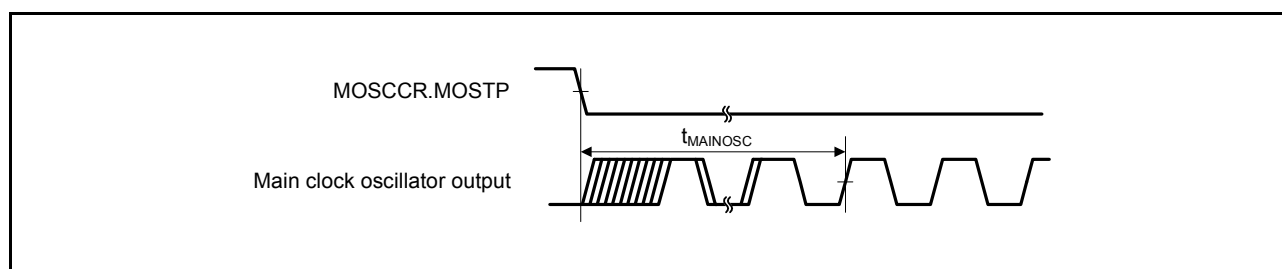


Figure 5.25 Main Clock Oscillation Start Timing

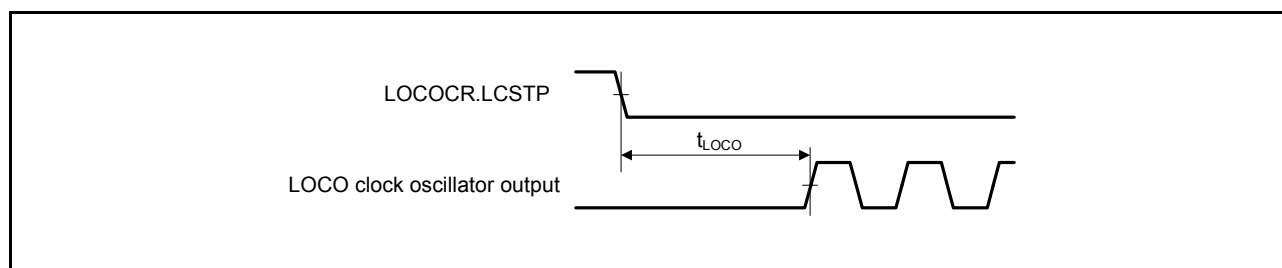


Figure 5.26 LOCO Clock Oscillation Start Timing

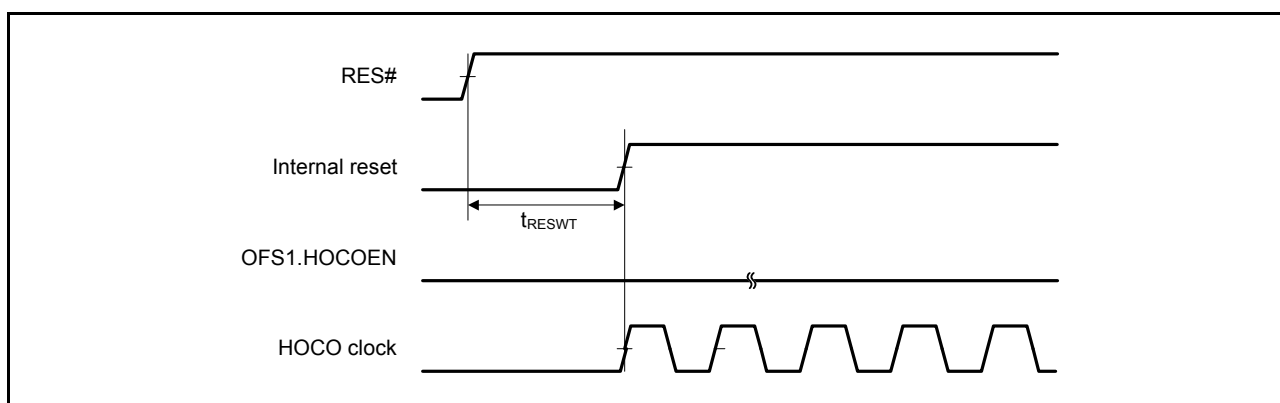


Figure 5.27 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

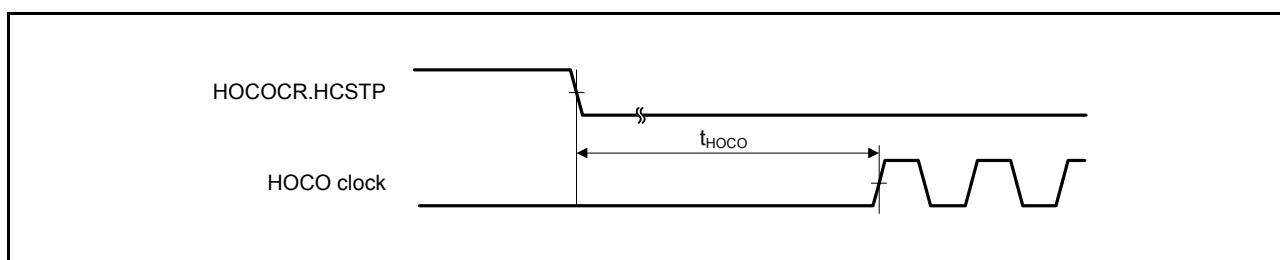


Figure 5.28 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

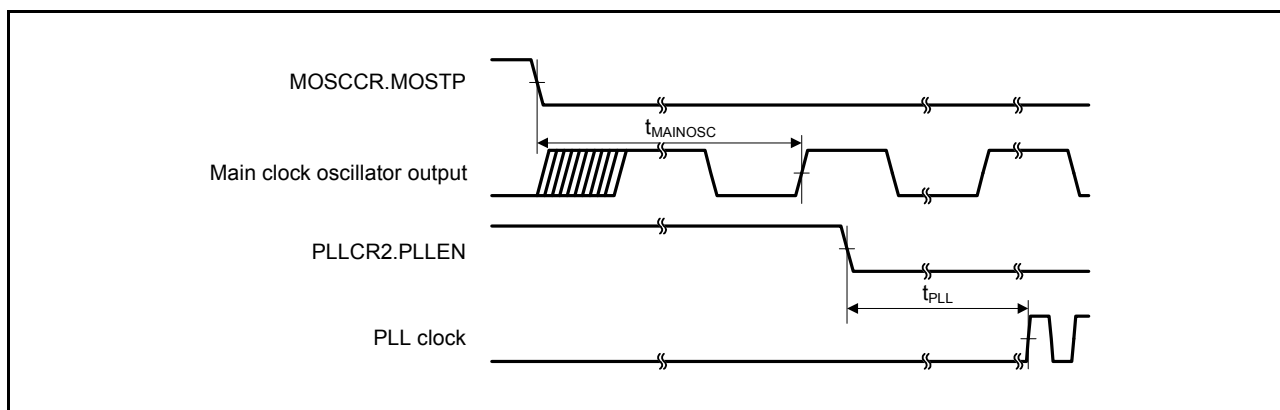


Figure 5.29 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

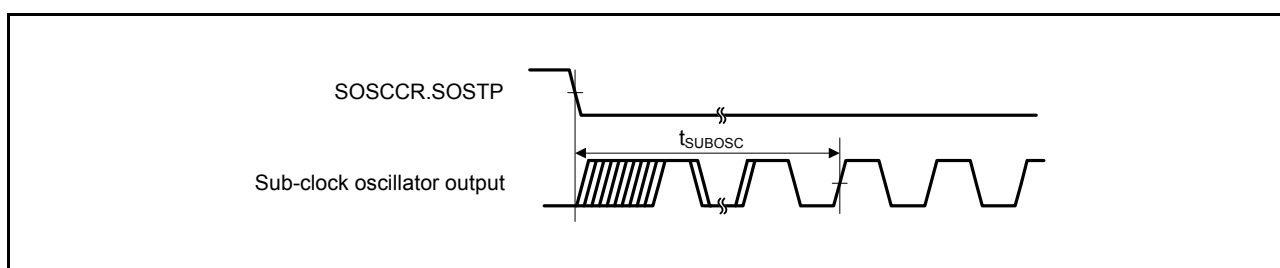


Figure 5.30 Sub-Clock Oscillation Start Timing

Table 5.29 Timing of Recovery from Low Power Consumption Modes (4)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	$t_{\text{DSL P}}$	—	2	3.5	μs
	Middle-speed mode*3	$t_{\text{DSL P}}$	—	3	4	μs
	Low-speed mode*4	$t_{\text{DSL P}}$	—	400	500	μs

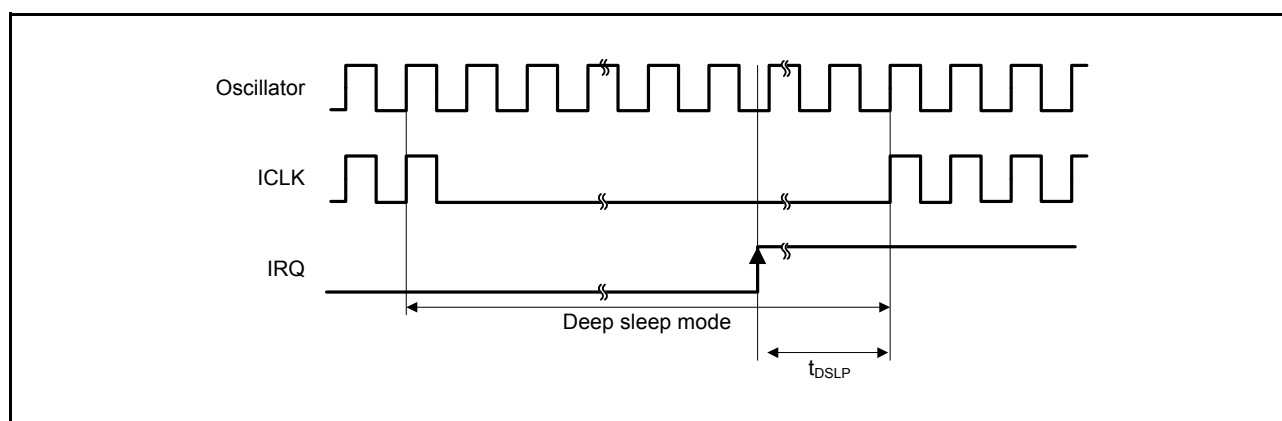
Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. Oscillators continue oscillating in deep sleep mode.

Note 2. When the frequency of the system clock is 32 MHz.

Note 3. When the frequency of the system clock is 12 MHz.

Note 4. When the frequency of the system clock is 32.768 kHz.

**Figure 5.35 Deep Sleep Mode Cancellation Timing****Table 5.30 Timing of Recovery from Low Power Consumption Modes (5) Operating Mode Transition Time**Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating mode	8 MHz	—	10	—	μs
Middle-speed operating mode	High-speed operating mode	8 MHz	—	37.5	—	μs
Low-speed operating mode	Middle-speed operating mode, high-speed operating mode	32.768 kHz	—	213.62	—	μs
Middle-speed operating mode, high-speed operating mode	Low-speed operating mode	32.768 kHz	—	183.11	—	μs

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

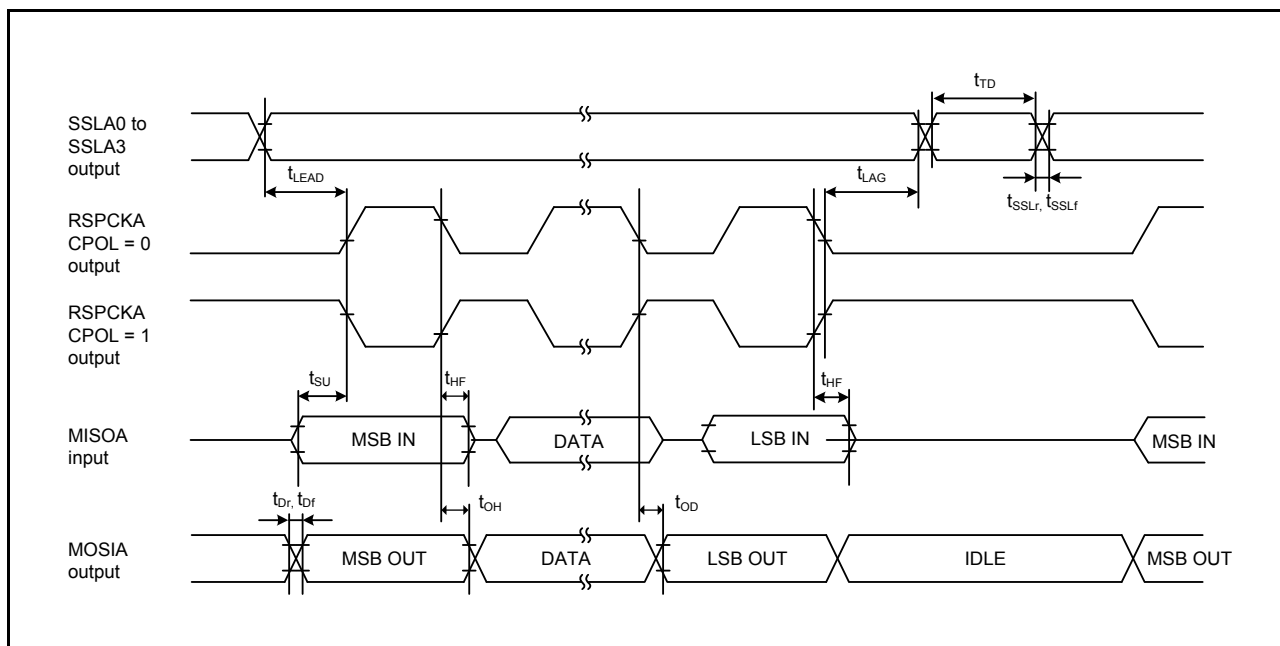


Figure 5.48 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2)

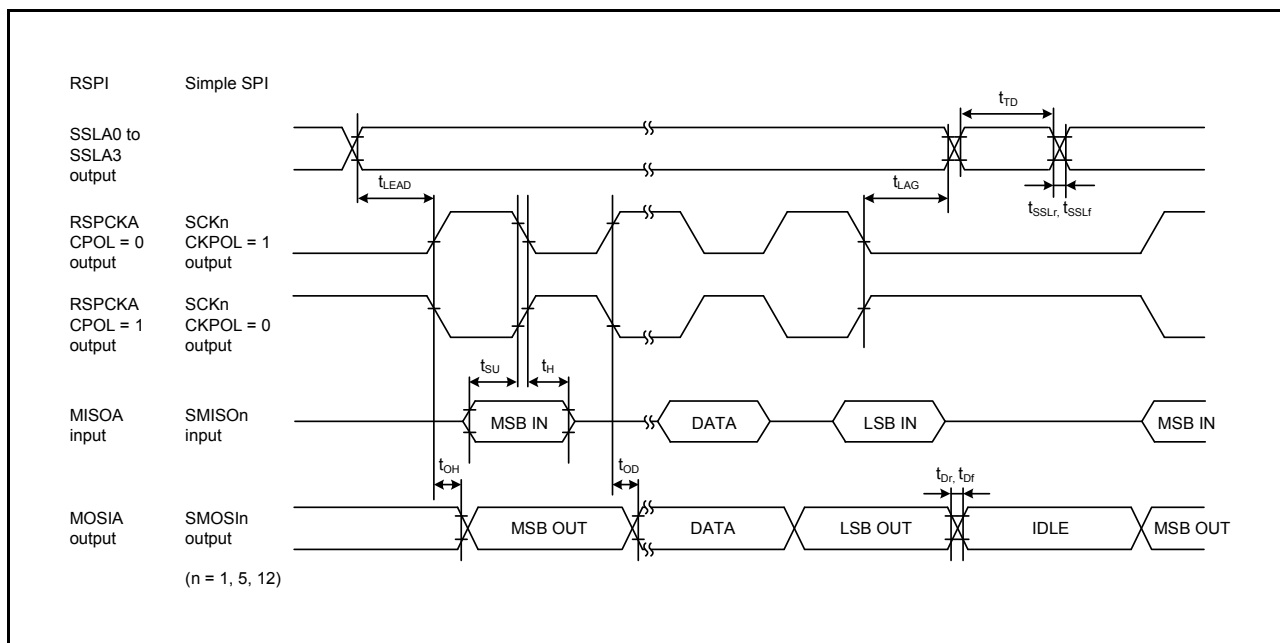


Figure 5.49 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 0)

Table 5.39 A/D Conversion Characteristics (2)

Conditions: $2.4\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $2.4\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $2.4\text{ V} \leq V_{REFH0} \leq AV_{CC0}$, $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		4	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 1.0 kΩ	2.062 (0.625)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 09h
		2.750 (1.313)*2	—	—	μs	Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±6.0	LSB	
Full-scale error		—	±1.25	±6.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.40 A/D Conversion Characteristics (3)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $1.8\text{ V} \leq V_{REFH0} \leq AV_{CC0}$, $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5.0 kΩ	4.875 (1.250)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 09h
		6.250 (2.625)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 14h
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±24.0	LSB	
Full-scale error		—	±1.25	±24.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.75	±32.0	LSB	
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.25	±12.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

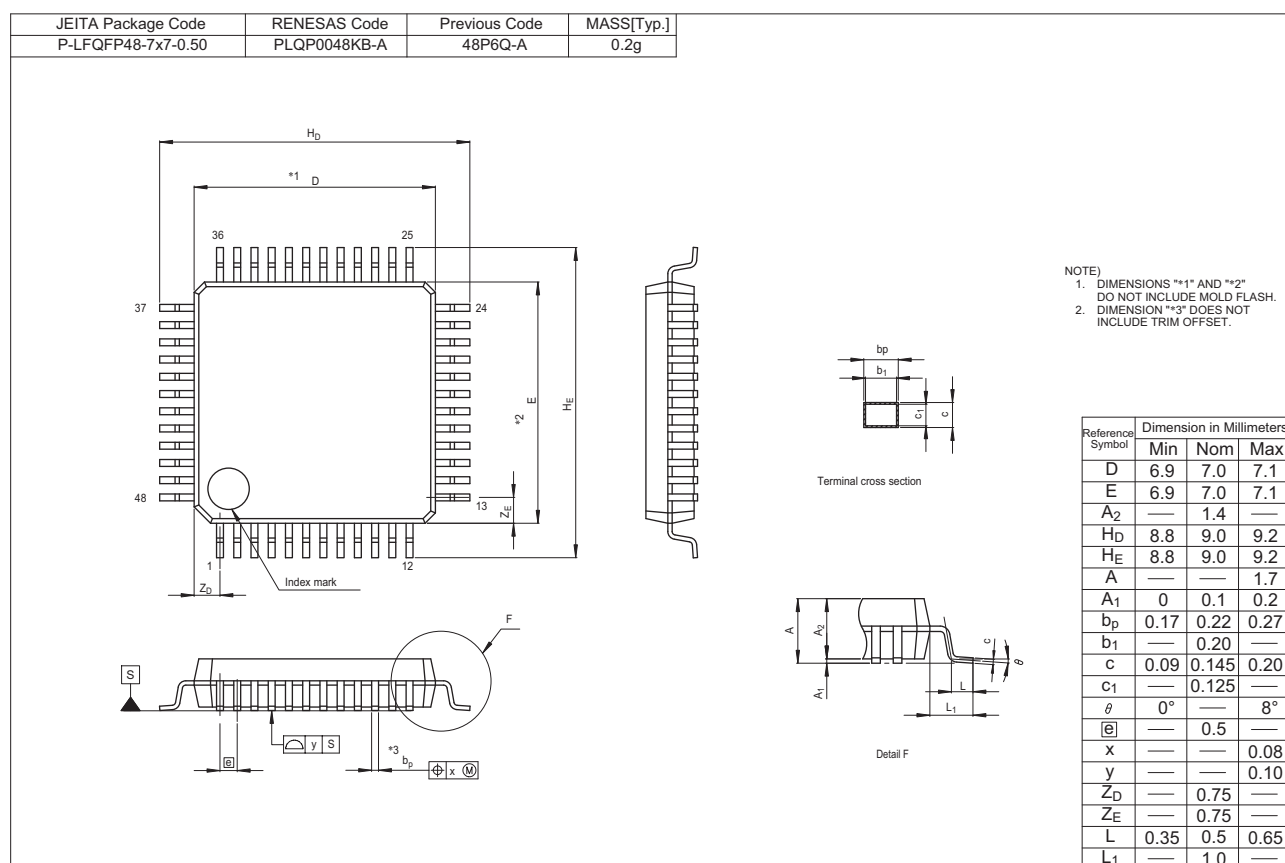


Figure D 48-Pin LFQFP (PLQP0048KB-A)