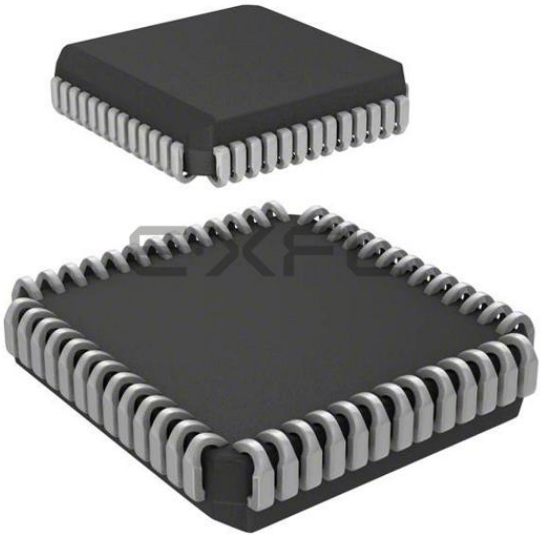

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	15KB (15K x 8)
Program Memory Type	OTP
EEPROM Size	256 x 8
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.1x19.1)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705b16ncfn

D
MC68HC05B16

E
MC68HC705B16

F
MC68HC705B16N

E1LAT — EEPROM programming latch enable bit

1 (set) – Address and data can be latched into the EEPROM for further program or erase operations, providing the E1PGM bit is cleared.

0 (clear) – Data can be read from the EEPROM. The E1ERA bit and the E1PGM bit are reset to zero when E1LAT is '0'.

STOP, power-on and external reset clear the E1LAT bit.

Note: After the t_{ERA1} erase time or t_{PROG1} programming time, the E1LAT bit has to be reset to zero in order to clear the E1ERA bit and the E1PGM bit.

E1PGM — EEPROM charge pump enable/disable

1 (set) – Internal charge pump generator switched on.

0 (clear) – Internal charge pump generator switched off.

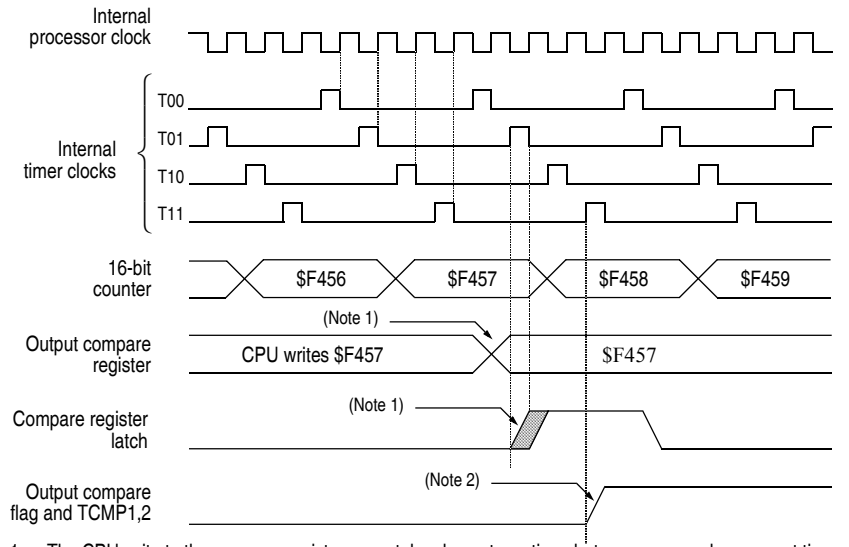
When the charge pump generator is on, the resulting high voltage is applied to the EEPROM array. This bit cannot be set before the data is selected, and once this bit has been set it can only be cleared by clearing the E1LAT bit.

A summary of the effects of setting/clearing bits 0, 1 and 2 of the control register are give in Table 3-1.

Table 3-1 EEPROM control bits description

E1ERA	E1LAT	E1PGM	Description
0	0	0	Read condition
0	1	0	Ready to load address/data for program/erase
0	1	1	Byte programming in progress
1	1	0	Ready for byte erase (load address)
1	1	1	Byte erase in progress

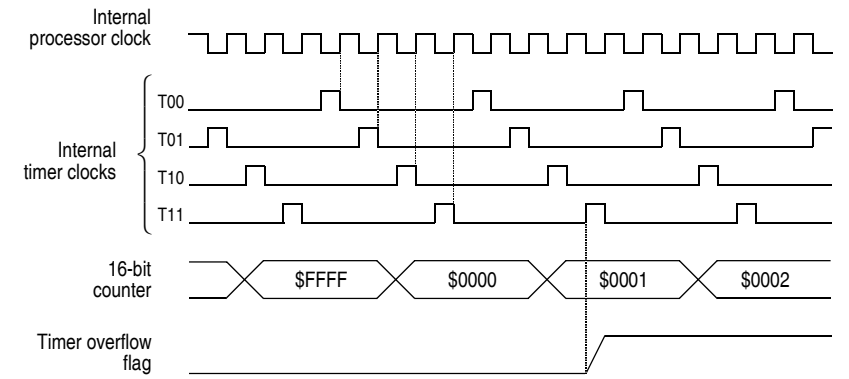
Note: All combinations are not shown in the above table, since the E1PGM and E1ERA bits are cleared when the E1LAT bit is at zero, and will result in a read condition.



Note: 1 The CPU write to the compare registers may take place at any time, but a compare only occurs at timer state T01. Thus a four cycle difference may exist between the write to the compare register and the actual compare.

1) The output compare flag is set at the timer state T11 that follows the comparison match ($F457 in this example).

Figure 5-4 Timer state timing diagram for output compare



Note: The timer overflow flag is set at timer state T11 (transition of counter from $FFFF to $0000). It is cleared by a read of the timer status register during the internal processor clock high time, followed by a read of the counter low register.

Figure 5-5 Timer state timing diagram for timer overflow

The SM bit is cleared by external or power-on reset. The SM bit is automatically cleared when entering STOP mode.

Note: The bits that are shown shaded in the above representation are explained individually in the relevant sections of this manual. The complete register plus an explanation of each bit can be found in Section 3.8

7.2 PLM clock selection

The slow/fast mode of the PLM D/A converters is selected by bits 1, 2, and 3 of the miscellaneous register at address $000C (SFA bit for PLMA and SFB bit for PLMB). The slow/fast mode has no effect on the D/A converters' 8-bit resolution (see Figure 7-3).

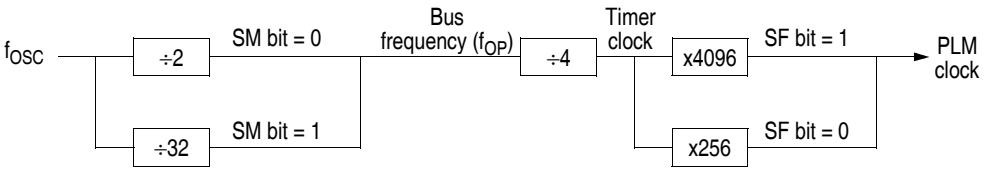


Figure 7-3 PLM clock selection

7.3 PLM during STOP mode

On entering STOP mode, the PLM outputs remain at their particular level. When STOP mode is exited by an interrupt, the PLM systems resume regular operation. If STOP mode is exited by power-on or external reset the registers values are forced to $00.

7.4 PLM during WAIT mode

The PLM system is not affected by WAIT mode and continues normal operation.

9.1.5 Functions affected by reset

When processing stops within the MCU for any reason, i.e. power-on reset, external reset or the execution of a STOP or WAIT instruction, various internal functions of the MCU are affected. Table 9-1 shows the resulting action of any type of system reset, but not necessarily in the order in which they occur.

Table 9-1 Effect of $\overline{\text{RESET}}$, POR, STOP and WAIT

Function/effect	$\overline{\text{RESET}}$	POR	WAIT	STOP
Timer prescaler set to zero	x	x	–	–
Timer counter set to $FFFC	x	x	–	–
All timer enable bits cleared (disable)	x	x	–	–
Data direction registers cleared (inputs)	x	x	–	–
Stack pointer set to $00FF	x	x	–	–
Force internal address bus to restart	x	x	–	–
Vector $1FFE, $1FFF	x	x	–	–
Interrupt mask bit (I-bit CCR) set to 1	x	x	–	–
Interrupt mask bit (I-bit CCR) cleared	–	–	x	x
Set interrupt enable bit (INTE)	x	x	–	–
Set POR bit in miscellaneous register	–	x	–	–
Reset STOP latch	x	x	–	–
Reset $\overline{\text{IRQ}}$ latch	x	x	–	–
Reset WAIT latch	x	x	–	–
SCI disabled	x	x	–	–
SCI status bits cleared (except TDRE and TC)	x	x	–	–
SCI interrupt enable bits cleared	x	x	–	–
SCI status bits TDRE and TC set	x	x	–	–
Oscillator disabled for 4064 cycles	–	x	–	x
Timer clock cleared	–	x	–	x
SCI clock cleared	–	x	–	x
A/D disabled	x	x	–	x
SM bit in the miscellaneous register cleared	x	x	–	x
Watchdog counter reset	x	x	x	x
WDOG bit in the miscellaneous register reset	x	x	–	x
EEPROM control bits (see Section 3.5.1)	x	x	–	x

x = Described action takes place

– = Described action does not take place

9.2.3.2 Miscellaneous register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous	$000C	POR	INTP	INTN	INTE	SFA	SFB	SM	WDOG	?001 000?

Note: The bits shown shaded in the above representation are explained individually in the relevant sections of this manual. The complete register plus an explanation of each bit can be found in Section 3.8.

INTP, INTN — External interrupt sensitivity options

These two bits allow the user to select which edge the $\overline{\text{IRQ}}$ pin is sensitive to as shown in Table 9-3. Both bits can be written to only while the I-bit is set, and are cleared by power-on or external reset. Therefore the device is initialised with negative edge and low level sensitivity.

Table 9-3 $\overline{\text{IRQ}}$ sensitivity

INTP	INTN	$\overline{\text{IRQ}}$ sensitivity
0	0	Negative edge and low level sensitive
0	1	Negative edge only
1	0	Positive edge only
1	1	Positive and negative edge sensitive

INTE — External interrupt enable

1 (set) – External interrupt function ($\overline{\text{IRQ}}$) enabled.

0 (clear) – External interrupt function ($\overline{\text{IRQ}}$) disabled.

The INTE bit can be written to only while the I-bit is set, and is set by power-on or external reset, thus enabling the external interrupt function.

Table 9-3 describes the various triggering options available for the $\overline{\text{IRQ}}$ pin, however it is important to re-emphasize here that in order to avoid any conflict and spurious interrupt, it is only possible to change the external interrupt options while the I-bit is set. Any attempt to change the external interrupt option while the I-bit is clear will be unsuccessful. If an external interrupt is pending, it will automatically be cleared when selecting a different interrupt option.

Note: If the external interrupt function is disabled by the INTE bit and an external interrupt is sensed by the edge detector circuitry, then the interrupt request is latched and the interrupt stays pending until the INTE bit is set. The internal latch of the external interrupt is cleared in the first part of the service routine (except for the low level

11.2 DC electrical characteristics

Table 11-2 DC electrical characteristics for 5V operation

(V_{DD} = 5 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{LOAD} = – 10 µA I_{LOAD} = +10 µA	 V_{OH} V_{OL}	 V_{DD} – 0.1 —	 — —	 — 0.1	V
Output high voltage (I_{LOAD} = 0.8 mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2 Output high voltage (I_{LOAD} = 1.6 mA) TDO, SCLK, PLMA, PLMB	 V_{OH} V_{OH}	 V_{DD} – 0.8 V_{DD} – 0.8	 V_{DD} – 0.4 V_{DD} – 0.4	 — —	V
Output low voltage (I_{LOAD} = 1.6 mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB Output low voltage (I_{LOAD} = 1.6 mA) $\overline{RESET}$	 V_{OL} V_{OL}	 — 	 0.1 0.4	 0.4 1	V
Input high voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$,TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Supply current[3] RUN (SM = 0) (See Figure 11-1) RUN (SM = 1) (See Figure 11-2) WAIT (SM = 0) (See Figure 11-3) WAIT (SM = 1) (See Figure 11-4) STOP 0 to 70 (standard) – 40 to 85 (extended) – 40 to 105 (extended) – 40 to 125 (automotive)	 I_{DD}	 — — — — — — — —	 3.5 0.5 1 0.35 2 — — —	 6 1.5 2 1 10 20 60 60	 mA mA mA mA µA µA µA µA
High-Z leakage current PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	±0.2	±1	µA
Input current (0 to 70) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	±0.2 ±0.2	±1 ±1	mA
Input current (– 40 to 125) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI,	I_{IN}	—	—	±5	µA
Capacitance Ports (as input or output), $\overline{RESET}$, TDO, SCLK $\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI PD0/AN0–PD7/AN7 (A/D off) PD0/AN0–PD7/AN7 (A/D on)	 C_{OUT} C_{IN} C_{IN} C_{IN}	 — — — —	 — — 12 22	 12 8 — —	 pF pF pF pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

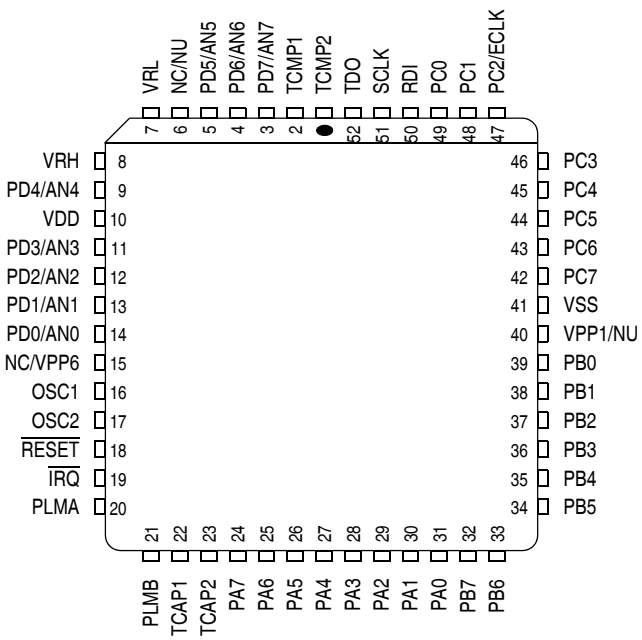
(2) Typical values are at mid point of voltage range and at 25°C only.

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 4.2MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and $V_{IH} = V_{DD}$ – 0.2 V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

12
MECHANICAL DATA

12.1 MC68HC05B family pin configurations

12.1.1 52-pin plastic leaded chip carrier (PLCC)



Device	Pin 6	Pin 15	Pin 40
MC68HC05B4	NC	NC	NU
MC68HC05B6	NC	NC	VPP1
MC68HC05B8	NC	NC	VPP1
MC68HC05B16	NC	NC	VPP1
MC68HC05B32	NC	NC	VPP1
MC68HC705B5	NC	VPP6	NU
MC68HC705B16	NU	VPP6	VPP1
MC68HC705B16N	NU	VPP6	VPP1
MC68HC705B32	NU	VPP6	VPP1

NC = Not connected

NU = Non-user pin (Should be tied to V_{SS} in an electrically noisy environment)

Figure 12-1 52-pin PLCC pinout for the MC68HC05B6

Table B-1 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EEPROM/ECLK control	$0007	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(3)	$0100							EE1P	SEC	Not affected

(1) This bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent upon the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

(3) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

C.5.1 Erased EPROM verification

The flowchart in Figure C-3 and Figure C-4 shows that the on-chip bootstrap routines can be used to check if the EPROM is erased (all $00s). If a non $00 byte is detected, the red LED stays on and the routine will stay in a loop. Only when the whole EPROM content is verified as erased will the green LED be turned on.

C.5.2 EPROM parallel bootstrap load

When this mode is selected, the EPROM is loaded in increasing address order with non EPROM segments being skipped by the loader. Simultaneous programming is performed by reading four bytes of data before actual programming is performed, thus dividing the loading time of the internal EPROM by four.

When PD2=0, the programming time is set to 5 milliseconds and the program/verify routine takes approximately 15 seconds.

Parallel data is entered through Port A, while the 13-bit address is output on port B and PC0 to PC4. If the data comes from an external EPROM, the handshake can be disabled by connecting together PC5 and PC6. If the data is supplied via a parallel interface, handshaking will be provided by PC5 and PC6 according to the timing diagram of Figure C-5.

During programming, the green LED flashes at about 3 Hz.

Upon completion of the programming operation, the EPROM content is checked against the external data source. If programming is verified the green LED stays on, while an error causes the red LED to be turned on. Figure C-6 shows a circuit that can be used to program the EPROM (or to load and execute data in the RAM).

Note: The entire EPROM can be loaded from the external source; if it is desired to leave a segment undisturbed, the data for this segment should be all zeros.

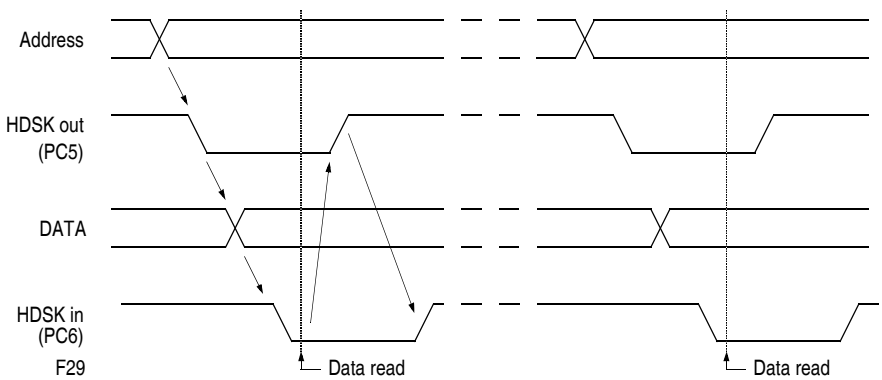


Figure C-5 Timing diagram with handshake

E.1 Features

- 15 kbytes EPROM
- 352 bytes of RAM
- 576 bytes bootstrap ROM
- Simultaneous programming of up to 8 bytes of EPROM
- Optional pull-down resistors available on all port B and port C pins
- 52-pin PLCC and 64-pin QFP packages
- High speed version not available

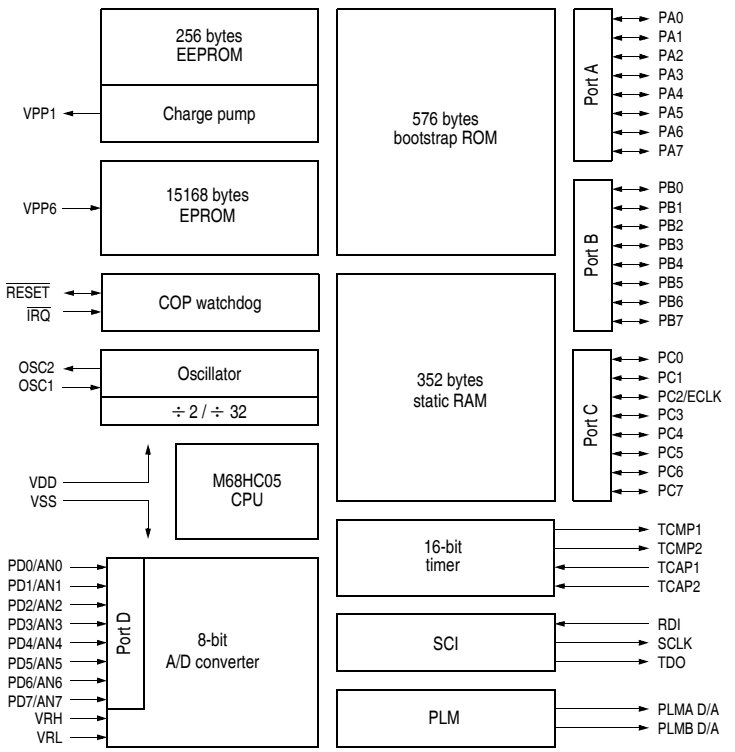


Figure E-1 MC68HC705B16 block diagram

Note: The electrical characteristics of the MC68HC05B6 as provided in Section 11 do not apply to the MC68HC705B16. Data specific to the MC68HC705B16 can be found in this appendix.

ECLK

See Section 4.3.

E1ERA — EEPROM erase/programming bit

Providing the E1LAT and E1PGM bits are at logic one, this bit indicates whether the access to the EEPROM is for erasing or programming purposes.

1 (set) – An erase operation will take place.

0 (clear) – A programming operation will take place.

Once the program/erase EEPROM address has been selected, E1ERA cannot be changed.

E1LAT — EEPROM programming latch enable bit

1 (set) – Address and data can be latched into the EEPROM for further program or erase operations, providing the E1PGM bit is cleared.

0 (clear) – Data can be read from the EEPROM. The E1ERA bit and the E1PGM bit are reset to zero when E1LAT is '0'.

STOP, power-on and external reset clear the E1LAT bit.

Note: After the t_{ERA1} erase time or t_{PROG1} programming time, the E1LAT bit has to be reset to zero in order to clear the E1ERA bit and the E1PGM bit.

E1PGM — EEPROM charge pump enable/disable

1 (set) – Internal charge pump generator switched on.

0 (clear) – Internal charge pump generator switched off.

When the charge pump generator is on, the resulting high voltage is applied to the EEPROM array. This bit cannot be set before the data is selected, and once this bit has been set it can only be cleared by clearing the E1LAT bit.

A summary of the effects of setting/clearing bits 0, 1 and 2 of the control register are given in Table E-3.

Table E-3 EEPROM control bits description

E1ERA	E1LAT	E1PGM	Description
0	0	0	Read condition
0	1	0	Ready to load address/data for program/erase
0	1	1	Byte programming in progress
1	1	0	Ready for byte erase (load address)
1	1	1	Byte erase in progress

Note: The E1PGM and E1ERA bits are cleared when the E1LAT bit is at zero.

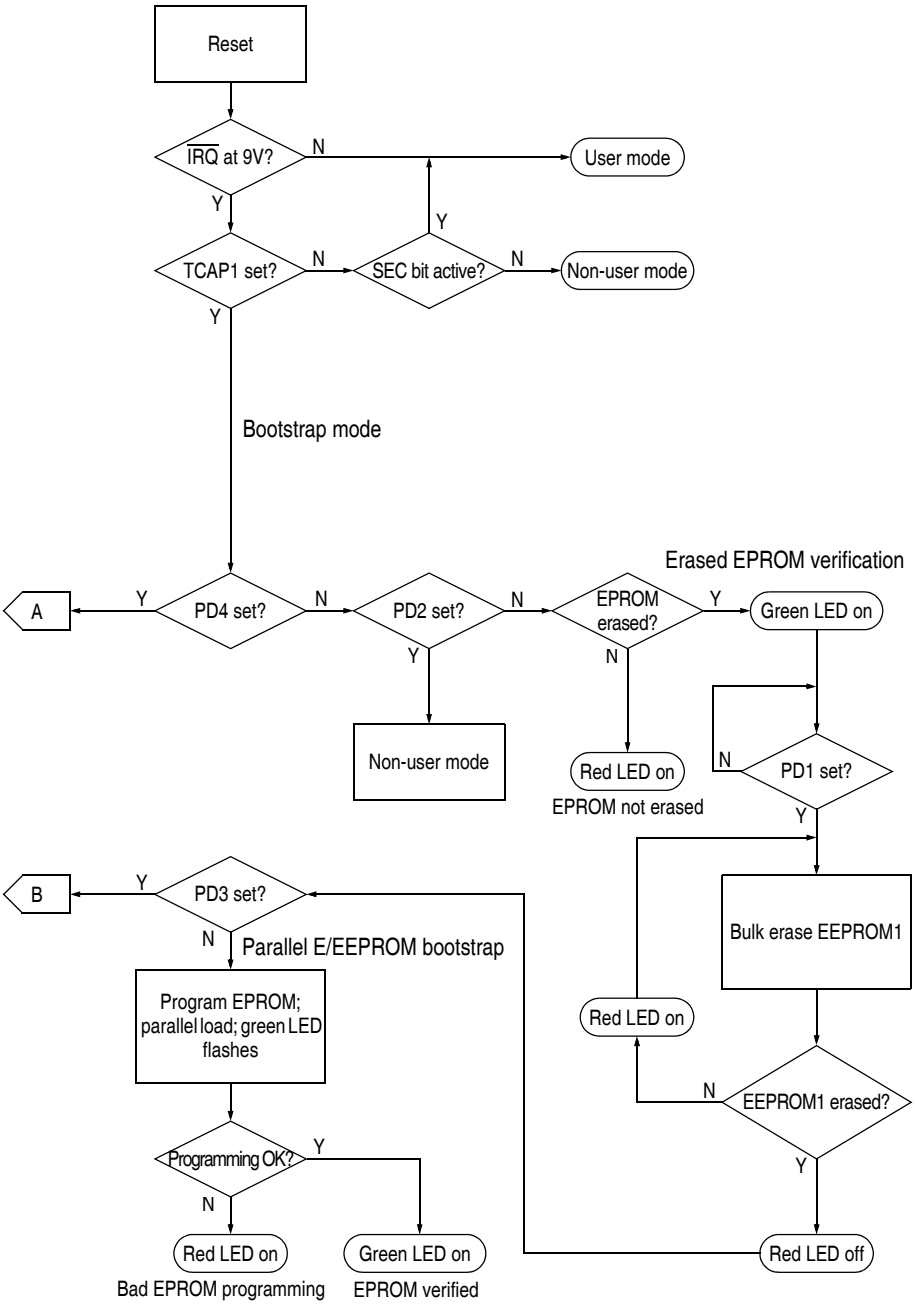


Figure E-3 Modes of operation flow chart (1 of 2)

Table F-1 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EPROM/EEPROM/ECLK control	$0007			E6LAT	E6PGM	ECLK	E1ERA	E1LAT	E1PGM	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(3)	$0100							EE1P	SEC	Not affected
Mask option register (MOR)(4)	$3DFE				RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) This bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent upon the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

(3) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

(4) This register is implemented in EPROM; therefore reset has no effect on the individual bits.

F.5.3 Serial RAM loader

This mode is similar to the RAM load/execute program for the MC68HC05B6 described in Section 2.2, with the additional features listed below. Table F-4 shows the entry conditions required for this mode.

If the first byte is less than $B0, the bootloader behaves exactly as the MC68HC05B6, i.e. count byte followed by data stored in $0050 to $00FF. If the count byte is larger than RAM I (176 bytes) then the code continues to fill RAM II. In this case the count byte is ignored and the program execution begins at $0051 once the total RAM area is filled or if no data is received for 5 milliseconds.

The user must take care when using branches or jumps as his code will be relocated in RAM I and II. If the user intends to use the stack in his program, he should send NOP's to fill the desired stack area.

In the RAM bootloader mode, all interrupt vectors are mapped to pseudo-vectors in RAM (see Table F-5). This allows programmers to use their own service-routine addresses. Each pseudo-vector is allowed three bytes of space rather than the two bytes for normal vectors, because an explicit jump (JMP) opcode is needed to cause the desired jump to the users service-routine address.

Table F-5 Bootstrap vector targets in RAM

Vector targets in RAM	
SCI interrupt	$0063
Timer overflow	$0060
Timer output compare	$005D
Timer input capture	$005A
$\overline{\text{IRQ}}$	$0057
SWI	$0054

F.5.3.1 Jump to start of RAM ($0051)

The Jump to start of RAM program will be executed when the device is brought out of reset with PD1 and PD4 at '1' and PD2 and PD3 at '0'.

F.6 Absolute maximum ratings

Table F-6 Absolute maximum ratings

Rating	Symbol	Value	Unit
Supply voltage(1)	V_{DD}	– 0.5 to +7.0	V
Input voltage (Except V_{PP1} and V_{PP6})	V_{IN}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input voltage – Self-check mode ($\overline{IRQ}$ pin only)	V_{IN}	V_{SS} – 0.5 to $2V_{DD}$ + 0.5	V
Operating temperature range – Standard (MC68HC705B16N) – Extended (MC68HC705B16NC) – Industrial (MC68HC705B16NV) – Automotive (MC68HC705B16NM)	T_A	T_L to T_H 0 to +70 –40 to +85 –40 to +105 –40 to +125	°C
Storage temperature range	T_{STG}	– 65 to +150	°C
Current drain per pin (excluding VDD and VSS)(2) – Source – Sink	 I_D I_S	 25 45	 mA mA

(1) All voltages are with respect to V_{SS}.

(2) Maximum current drain per pin is for one pin at a time, limited by an external resistor.

Note: This device contains circuitry designed to protect against damage due to high electrostatic voltages or electric fields. However, it is recommended that normal precautions be taken to avoid the application of any voltages higher than those given in the maximum ratings table to this high impedance circuit. For maximum reliability all unused inputs should be tied to either V_{SS} or V_{DD}.

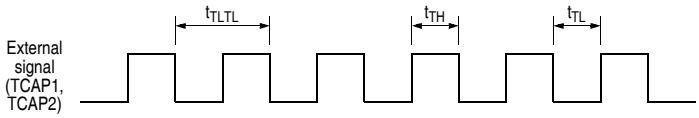


Figure F-10 Timer relationship

F.10 EPROM electrical characteristics

Table F-13 DC electrical characteristics for 5V operation

(V_{DD} = 5 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = 25°C)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
EPROM					
Absolute maximum voltage	V_{PP6} max	V_{DD}	—	18	V
Programming voltage	V_{PP6}	15	15.5	16	V
Programming current	I_{PP6}	—	50	64	mA
Read voltage	V_{PP6R}	V_{DD}	V_{DD}	V_{DD}	V

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25°C only.

Table F-14 Control timing for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = 25°C)

Characteristic	Symbol	Min	Max	Unit
EPROM programming time	t_{PROG}	5	20	ms

Table F-15 Control timing for 3.3V operation

(V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = 25°C)

Characteristic	Symbol	Min	Max	Unit
EPROM programming time	t_{PROG}	5	20	ms

H

MC68HC705B32

Maskset errata

This errata section outlines the differences between two previously available masksets (D59J and D40J) and all other masksets. Unless otherwise stated, the main body of Appendix G refers to all these other masksets with any differences being noted in this errata section.

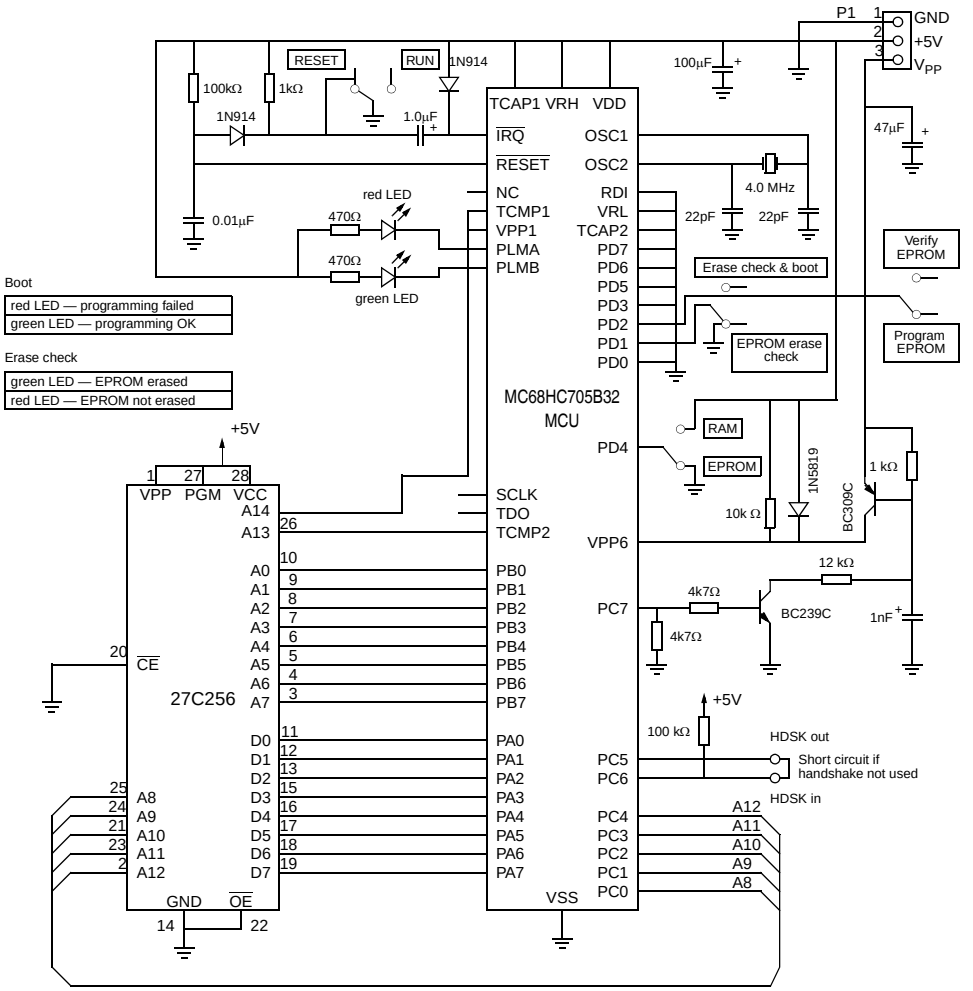
- For the D59J and D40J masksets, the MCU only requires that a logic zero is applied to the $\overline{\text{RESET}}$ input for 1.5 t_{CYC}.
- For D59J, 16 cycle POR delay option (t_{PORL}) is not available
- For the D59J maskset, oscillator divide ratio DIV10 is forced in Bootstrap mode. On all other revisions DIV2 is forced.

For the D59J:

The STOP Idd is greater than the expected value of 120μA at 5 volts Vdd at a temperature of 20°C with the CAN module enabled and in SLEEP mode. Typically the STOP Idd is in the region of 2.0 milliamps at 20°C.

The fault lies with the design of the EPROM array. When the STOP instruction is executed, the next opcode in memory is present on the data bus. A fault in the EPROM write data latch circuitry causes a latch to be driven to logic 0 on both sides when the data bus for that bit is logic 1. This results in increasing STOP Idd of 450μA per data bus bit set to a logic 1. If all data bus bits are set to logic 1 (i.e. next opcode is $FF, STX 0,X) the STOP Idd shall be in the region of 3.6mA.

The minimum STOP Idd is achieved by ensuring the opcode immediately following the STOP instruction is data $00. This corresponds to BRSET 0,ADDRESS,LABEL. If the label points to the next sequential instruction in memory then this has the effect of a 5 cycle NOP but note that the carry bit in the condition code register may be altered by the BRSET instruction.



Note: This circuit is recommended for programming only at 25°C and not for use in the end application, or at temperatures other than 25°C. If used in the end application, VPP6 should be tied to VDD to avoid damaging the device.

Figure H-7 EPROM parallel bootstrap schematic diagram