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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	15KB (15K x 8)
Program Memory Type	OTP
EEPROM Size	256 x 8
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	56-SDIP (0.600", 15.24mm)
Supplier Device Package	56-PSDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc705b16nbe

2.5.9 RDI (Receive data in)

The RDI pin is the input pin of the SCI receiver.

2.5.10 TDO (Transmit data out)

The TDO pin is the output pin of the SCI transmitter.

2.5.11 SCLK

The SCLK pin is the clock output pin of the SCI transmitter.

2.5.12 PLMA

The PLMA pin is the output of pulse length modulation converter A.

2.5.13 PLMB

The PLMB pin is the output of pulse length modulation converter B.

2.5.14 VPP1

The VPP1 pin is the output of the charge pump for the EEPROM1 array.

2.5.15 VRH

The VRH pin is the positive reference voltage for the A/D converter.

2.5.16 VRL

The VRL pin is the negative reference voltage for the A/D converter.

2.5.17 PA0 – PA7/PB0 – PB7/PC0 – PC7

These 24 I/O lines comprise ports A, B and C. The state of any pin is software programmable, and all the pins are configured as inputs during power-on or reset.

Under software control the PC2 pin can output the internal E-clock (see Section 4.2).

2.5.18 PD0/AN0–PD7/AN7

This 8-bit input only port (D) shares its pins with the A/D converter. When enabled, the A/D converter uses pins PD0/AN0 – PD7/AN7 as its analog inputs. On reset, the A/D converter is disabled which forces the port D pins to be input only port pins (see Section 8.5).

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3.4 Self-check ROM

There are two areas of self-check ROM (ROMI and ROMII) located from $0200 to $02BF (192 bytes) and $1F00 to $1FEF (240 bytes) respectively.

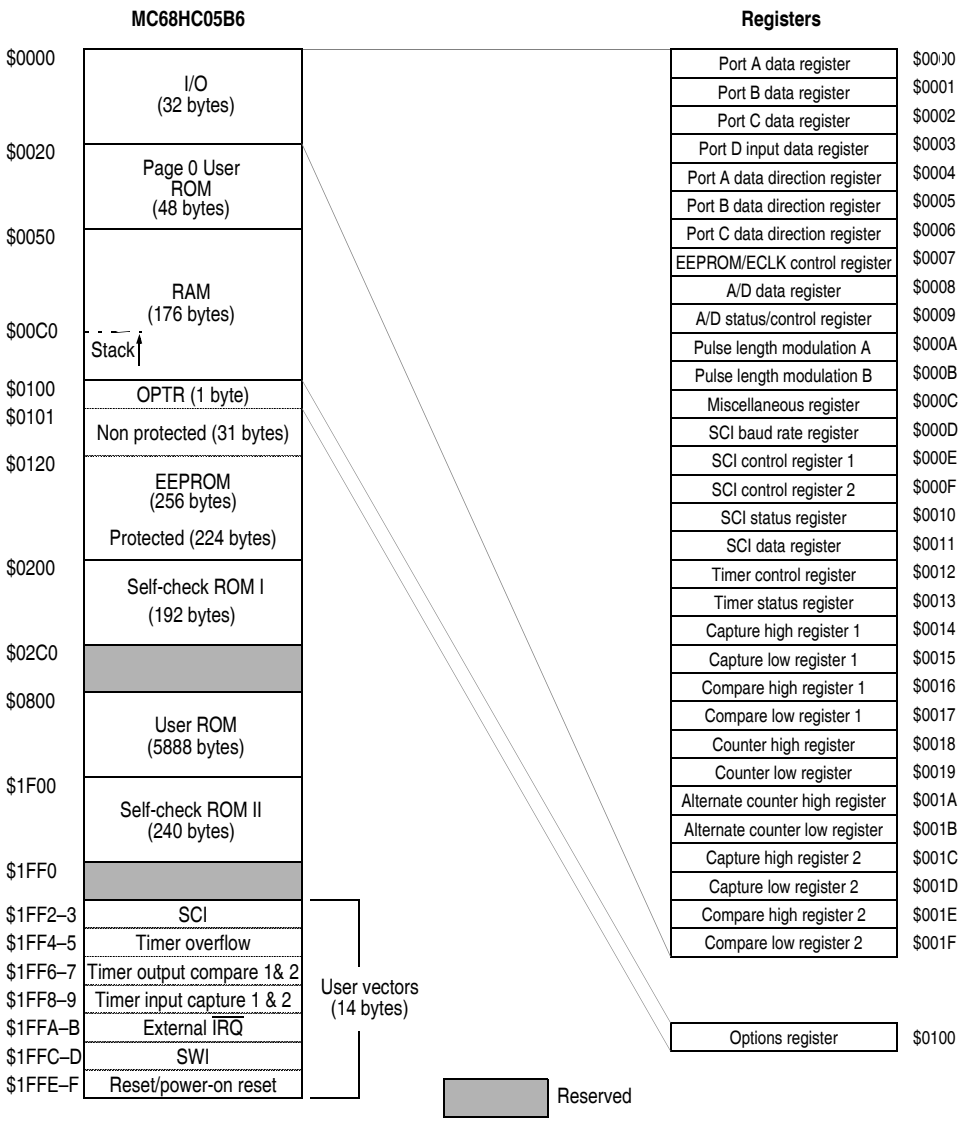

Figure 3-1 Memory map of the MC68HC05B6

3.5 EEPROM

The user EEPROM consists of 256 bytes of memory located from address $0100 to $01FF. 255 bytes are general purpose and 1 byte is used by the option register. The non-volatile EEPROM is byte erasable.

An internal charge pump provides the EEPROM voltage (V_{PP1}), which removes the need to supply a high voltage for erase and programming functions. The charge pump is a capacitor/diode ladder network which will give a very high impedance output of around 20-30 MΩ. The voltage of the charge pump is visible at the VPP1 pin. During normal operation of the device, where programming/erasing of the EEPROM array will occur, VPP1 should never be connected to either VDD or VSS as this could prevent the charge pump reaching the necessary programming voltage. Where it is considered dangerous to leave VPP1 unconnected for reasons of excessive noise in a system, it may be tied to V_{DD}; this will protect the EEPROM data but will also increase power consumption, and therefore it is recommended that the protect bit function is used for regular protection of EEPROM data (see Section 3.5.5).

In order to achieve a higher degree of security for stored data, there is no capability for bulk or row erase operations.

The EEPROM control register ($0007) provides control of the EEPROM programming and erase operations.

Warning: The VPP1 pin should never be connected to VSS, as this could cause permanent damage to the device.

3.5.1 EEPROM control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EEPROM/ECLK control	$0007	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000

ECLK

See Section 4.3 for a description of this bit.

E1ERA — EEPROM erase/programming bit

Providing the E1LAT and E1PGM bits are at logic one, this bit indicates whether the access to the EEPROM is for erasing or programming purposes.

1 (set) – An erase operation will take place.

0 (clear) – A programming operation will take place.

Once the program/erase EEPROM address has been selected, E1ERA cannot be changed.

5.1.1 Counter register and alternate counter register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100

The double-byte, free-running counter can be read from either of two locations, $18-$19 (counter register) or $1A-$1B (alternate counter register). A read from only the less significant byte (LSB) of the free-running counter ($19 or $1B) receives the count value at the time of the read. If a read of the free-running counter or alternate counter register first addresses the more significant byte (MSB) ($18 or $1A), the LSB is transferred to a buffer. This buffer value remains fixed after the first MSB read, even if the user reads the MSB several times. This buffer is accessed when reading the free-running counter or alternate counter register LSB and thus completes a read sequence of the total counter value. In reading either the free-running counter or alternate counter register, if the MSB is read, the LSB must also be read to complete the sequence. If the timer overflow flag (TOF) is set when the counter register LSB is read then a read of the timer status register (TSR) will clear the flag.

The alternate counter register differs from the counter register only in that a read of the LSB does not clear TOF. Therefore, where it is critical to avoid the possibility of missing timer overflow interrupts due to clearing of TOF, the alternate counter register should be used.

The free-running counter is set to $FFFC during power-on and external reset and is always a read-only register. During a power-on reset, the counter begins running after the oscillator start-up delay. Because the free-running counter is 16 bits preceded by a fixed divide-by-4 prescaler, the value in the free-running counter repeats every 262,144 internal bus clock cycles. TOF is set when the counter overflows (from $FFFF to $0000); this will cause an interrupt if TOIE is set.

In some particular timing control applications it may be desirable to reset the 16-bit free running counter under software control. When the low byte of the counter ($19 or $1B) is written to, the counter is configured to its reset value ($FFFC).

The divide-by-4 prescaler is also reset and the counter resumes normal counting operation. All of the flags and enable bits remain unaltered by this operation. If access has previously been made to the high byte of the free-running counter ($18 or $1A), then the reset counter operation terminates the access sequence.

Warning: This operation may affect the function of the watchdog system (see Section 9.1.4). The PLM results will also be affected while resetting the counter.

10.1.1 Accumulator (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

10.1.2 Index register (X)

The index register is an 8-bit register, which can contain the indexed addressing value used to create an effective address. The index register may also be used as a temporary storage area.

10.1.3 Program counter (PC)

The program counter is a 16-bit register, which contains the address of the next byte to be fetched.

10.1.4 Stack pointer (SP)

The stack pointer is a 16-bit register, which contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the ten most significant bits are permanently set to 0000000011. These ten bits are appended to the six least significant register bits to produce an address within the range of $00C0 to $00FF. Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and overwrites the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.

10.1.5 Condition code register (CCR)

The CCR is a 5-bit register in which four bits are used to indicate the results of the instruction just executed, and the fifth bit indicates whether interrupts are masked. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.

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Table 11-7 Control timing for 3.3V operation

(V_{DD} = 3.3Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	2.0	MHz
External clock option	f_{OSC}	dc	2.0	MHz
Internal operating frequency (f_{OSC}/2)				
Using crystal	f_{OP}	—	1.0	MHz
Using external clock	f_{OP}	dc	1.0	MHz
Cycle time (see Figure 9-1)	t_{CYC}	1000	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		5	µs
A/D converter stabilization time	t_{ADON}		500	µs
External $\overline{\text{RESET}}$ input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on $\overline{\text{RESET}}$ output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog $\overline{\text{RESET}}$ output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	30	—	ms
– 40 to 85 (extended)	t_{ERA}	30	—	ms
– 40 to 125 (automotive)	t_{ERA}	30	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	30	—	ms
– 40 to 85 (extended)	t_{PROG}	30	—	ms
– 40 to 125 (automotive)	t_{PROG}	30	—	ms
Timer (see Figure 11-13)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	250	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	250	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width(5)	t_{OH}, t_{OL}	200	—	ns
Write/Erase endurance(6)(7)	—	10000		cycles
Data retention(6)(7)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{CYC}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.

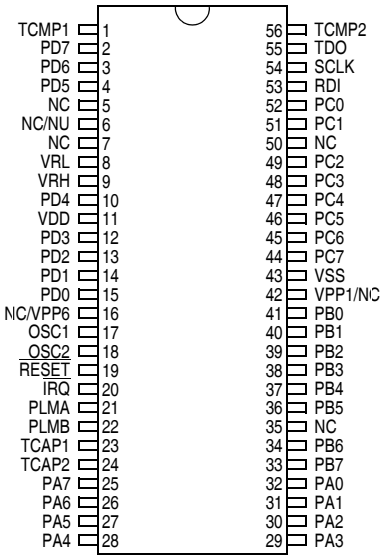
(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

(5) t_{OH} and t_{OL} should not total less than 500ns.

(6) At a temperature of 85°C

(7) Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

12.1.3 56-pin shrink dual in line package (SDIP)



Device	Pin 6	Pin 16	Pin 42
MC68HC05B4	NC	NC	NC
MC68HC05B6	NC	NC	VPP1
MC68HC05B8	NC	NC	VPP1
MC68HC05B16	NC	NC	VPP1
MC68HC05B32	NC	NC	VPP1
MC68HC705B5	NC	VPP6	NC
MC68HC705B16	Not available in this package		
MC68HC705B16N	Contact Sales		
MC68HC705B32	NU	VPP6	VPP1

NC = Not connected

NU = Non-user pin (Should be tied to V_{SS} in an electrically noisy environment)

Figure 12-3 56-pin SDIP pinout for the MC68HC05B6

C
MC68HC705B5

The MC68HC705B5 is a device similar to the MC68HC05B6, but with the 6 kbytes ROM and 256 bytes EEPROM replaced by a single EPROM array. In addition, the self-check routines available on the MC68HC05B6 are replaced by bootstrap firmware. The MC68HC705B5 is intended to operate as a one time programmable (OTP) version of the MC68HC05B6 without EEPROM or the MC68HC05B4, meaning that the application program can never be erased once it has been loaded into the EPROM. The entire MC68HC05B6 data sheet applies to the MC68HC705B5, with the exceptions outlined in this appendix.

C.1 Features

- 6206 bytes EPROM (including 14 bytes User vectors)
- No EEPROM
- Bootstrap firmware
- Simultaneous programming of up to 4 bytes
- Data protection for program code
- Optional pull-down resistors on port B and port C
- MC68HC05B6 mask options are programmable using control bits held in the options register
- 52-pin PLCC and 56-pin SDIP packages
- High speed version not available

C.2 EPROM

The MC68HC705B5 has a total of 6206 bytes of EPROM, 256 bytes being reserved for the EPROM1 array (see Figure C-2). The EPP bit (EPROM protect) is not operative on the EPROM1 array, making it possible to program it after the main EPROM has been programmed and protected. The reset and interrupt vectors are located at $1FF2-$1FFF and the EPROM control register described in Section C.3.1 is located at address $0007.

The EPROM array is supplied by the VPP6 pin in both read and programming modes. Typically the user's software will be loaded in a programming board where VPP6 is controlled by one of the bootstrap loader routines (bootloader mode). It will then be placed in an application where no programming occurs (user mode). In this case the VPP6 pin should be hardwired to V_{DD}.

An erased EPROM byte reads as $00.

Warning: A minimum V_{DD} voltage must be applied to the VPP6 pin at all times, including power-on, as a lower voltage could damage the device. Unless otherwise stated, EPROM programming is guaranteed at ambient (25°C) temperature only

C.2.1 EPROM programming operation

The User program can be used to program some EPROM locations, provided the proper procedure is followed. In particular, the programming sequence must be running in RAM, as the EPROM will not be available for code execution while the ELAT bit is set. The VPP6 switching must occur externally, after the EPGM bit is set, for example, under the control of a signal generated on a pin by the programming routine.

Note: Unless the part has a window for reprogramming, only the cumulative programming of bits to logic 1 is possible if multiple programming is made on the same byte.

To allow simultaneous programming of up to 4 bytes, they must be in the same group of addresses which share the same most significant address bits; only the two LSBs can change.

C.4 Options register (OPTR)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Options (OPTR)(1)	$1EFE		EPP	0	RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) This register is implemented in EPROM, therefore reset has no effect on the state of the individual bits.

Note: This register can only be written to while the device is in bootloader mode.

Bit 7 — Factory use only

Warning: This bit is strictly for factory use only and will always read zero to avoid accidental damage to the device. Any attempt to write to this bit could result in physical damage.

EPP — EPROM protect

This bit protects the contents of the main EPROM against accidental modification; it has no effect on reading or executing code in the EPROM.

1 (set) – EPROM contents are protected.

0 (clear) – EPROM contents are not protected.

RTIM — Reset time

This bit can modify t_{PORL}, i.e. the time that the $\overline{\text{RESET}}$ pin is kept low following a power-on reset. This feature is handled in the ROM part via a mask option.

1 (set) – t_{PORL} = 16 cycles.

0 (clear) – t_{PORL} = 4064 cycles.

RWAT — Watchdog after reset

This bit can modify the status of the watchdog counter after reset.

1 (set) – The watchdog will be active immediately following power-on or external reset (except in bootstrap mode).

0 (clear) – The watchdog system will be disabled after power-on or external reset.

WWAT — Watchdog during WAIT mode

This bit can modify the status of the watchdog counter during WAIT mode.

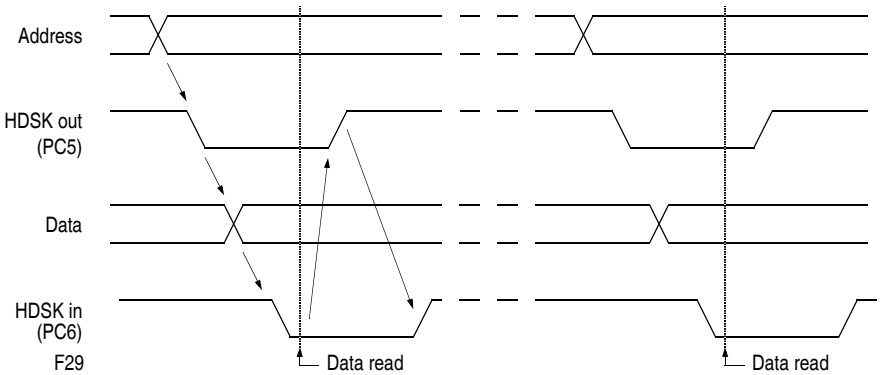
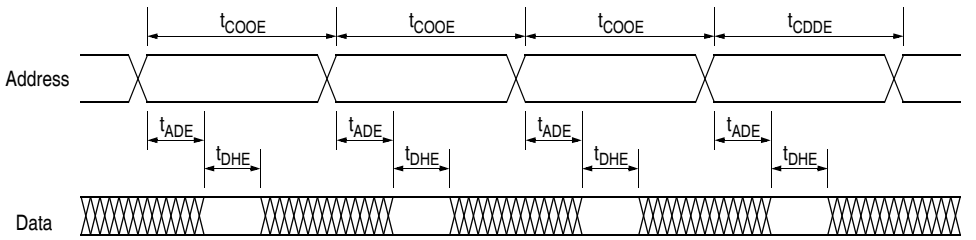


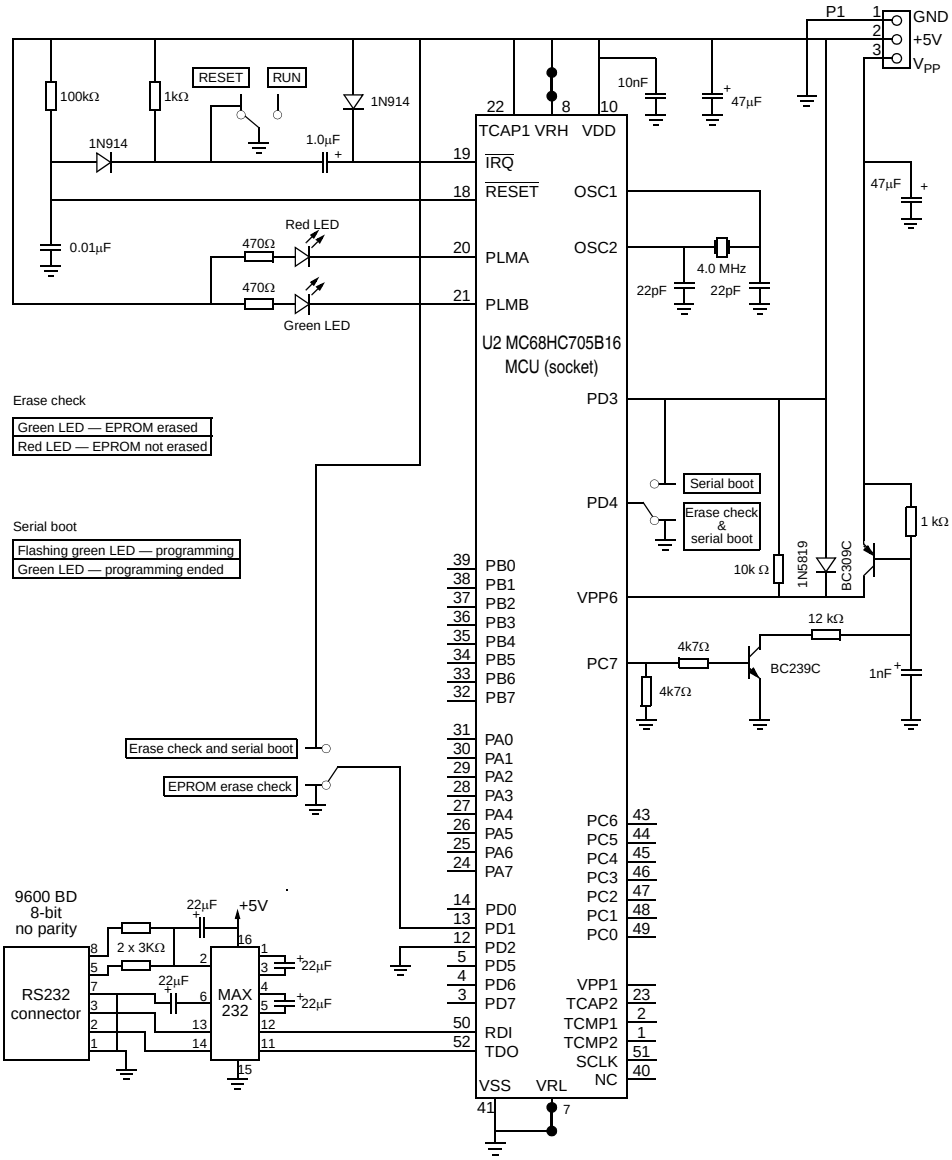
Figure E-5 Timing diagram with handshake



t_{ADE} max (address to data delay)	5 machine cycles
t_{DHA} min (data hold time)	14 machine cycles
t_{COOE} (load cycle time)	117 machine cycles < t_{COOE} < 150 machine cycles
t_{CDDE} (programming cycle time)	t_{COOE} + t_{PROG} (5 ms nominal for EPROM; 10ms for EEPROM1))

1 machine cycle = $1/(2f_0(Xtal))$

Figure E-6 Parallel EPROM loader timing diagram



Note: A minimum V_{DD} voltage must be applied to the VPP6 pin at all times, including power-on, as a lower voltage could damage the device. Unless otherwise stated, EPROM programming is guaranteed at ambient (25°C) temperature only

Figure E-8 RAM/EPROM/EEPROM serial bootstrap schematic diagram

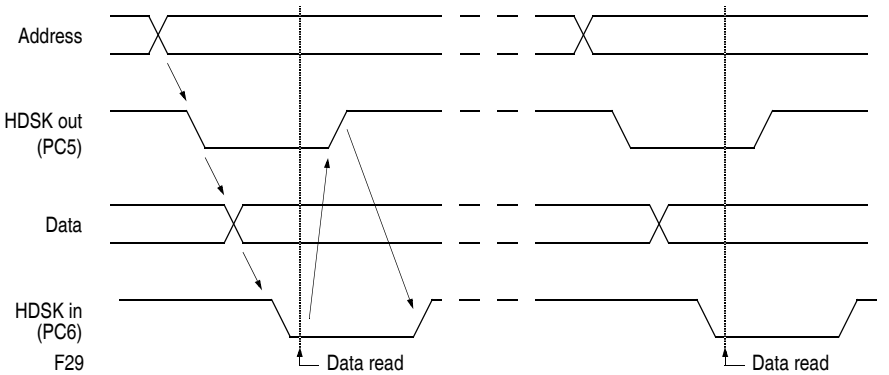
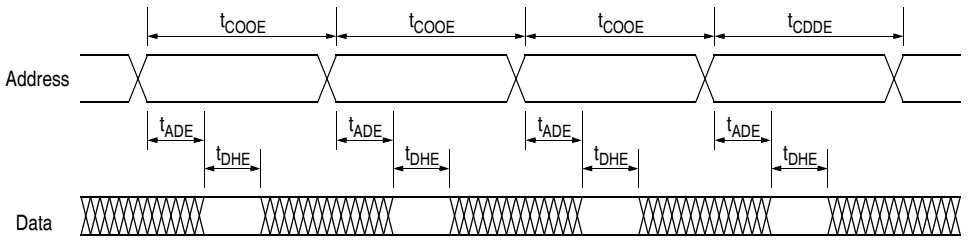


Figure F-5 Timing diagram with handshake



t_{ADE} max (address to data delay)	5 machine cycles
t_{DHA} min (data hold time)	14 machine cycles
t_{COOE} (load cycle time)	117 machine cycles < t_{COOE} < 150 machine cycles
t_{CDDE} (programming cycle time)	t_{COOE} + t_{PROG} (10 ms nominal for EPROM; 10ms for EEPROM1))

1 machine cycle = $1/(2f_0(Xtal))$

Figure F-6 Parallel EPROM loader timing diagram

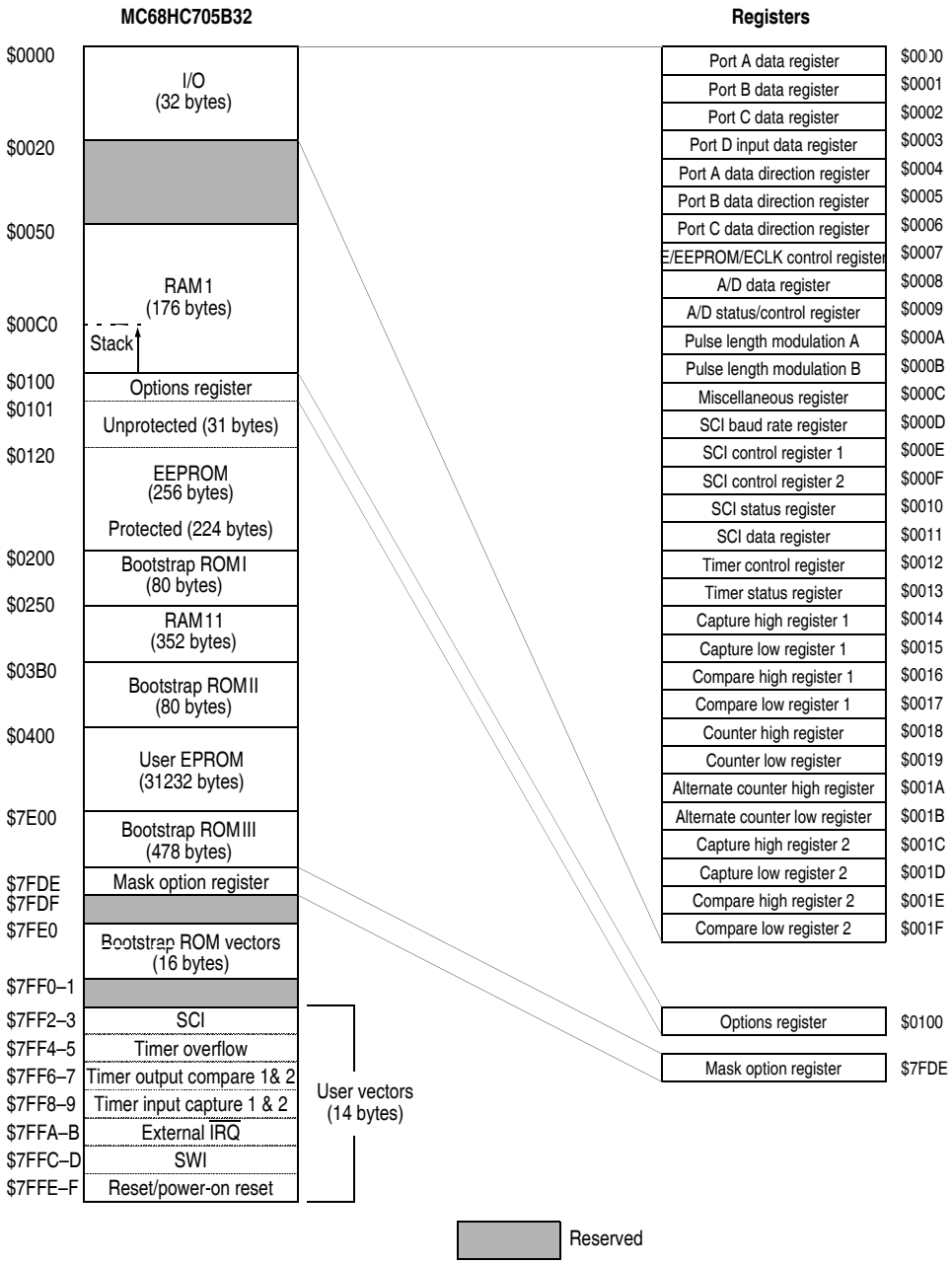


Figure H-2 Memory map of the MC68HC705B32

H.4.1 EPROM read operation

The execution of a program in the EPROM address range or a load from the EPROM are both read operations. The E6LAT bit in the EPROM/EEPROM control register should be cleared to ‘0’ which automatically resets the E6PGM bit. In this way the EPROM is read like a normal ROM. Reading the EPROM with the E6LAT bit set will give data that does not correspond to the actual memory content. As interrupt vectors are in EPROM, they will not be loaded when E6LAT is set. Similarly, the bootstrap ROM routines cannot be executed when E6LAT is set. In read mode, the VPP6 pin must be at the V_{DD} level. When entering the STOP mode, the EPROM is automatically set to the read mode.

Note: An erased byte reads as $00.

H.4.2 EPROM program operation

Typically, the EPROM will be programmed by the bootstrap routines resident in the on-chip ROM. However, the user program can be used to program some EPROM locations if the proper procedure is followed. In particular, the programming sequence must be running in RAM, as the EPROM will not be available for code execution while the E6LAT bit is set. The V_{PP6} switching must occur externally after EPGM is set, for example under control of a signal generated on a pin by the programming routine.

Note: Unless the part has a window for reprogramming, only the cumulative programming of bits to logic ‘1’ is possible if multiple programming is made on the same byte.

To allow simultaneous programming of up to sixteen bytes, these bytes must be in the same group of addresses which share the same most significant address bits; only the four LSBs can change.

H.4.3 EPROM/EEPROM control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EPROM/EEPROM/ECLK control	$0007		0	E6LAT	E6PGM	ECLK	E1ERA	E1LAT	E1PGM	u000 0000

E1LAT — EEPROM programming latch enable bit

1 (set) – Address and data can be latched into the EEPROM for further program or erase operations, providing the E1PGM bit is cleared.

0 (clear) – Data can be read from the EEPROM. The E1ERA bit and the E1PGM bit are reset to zero when E1LAT is ‘0’.

STOP, power-on and external reset clear the E1LAT bit.

Note: After the t_{ERA1} erase time or t_{PROG1} programming time, the E1LAT bit has to be reset to zero in order to clear the E1ERA bit and the E1PGM bit.

E1PGM — EEPROM charge pump enable/disable

1 (set) – Internal charge pump generator switched on.

0 (clear) – Internal charge pump generator switched off.

When the charge pump generator is on, the resulting high voltage is applied to the EEPROM array. This bit cannot be set before the data is selected, and once this bit has been set it can only be cleared by clearing the E1LAT bit.

A summary of the effects of setting/clearing bits 0, 1 and 2 of the control register are given in Table H-3.

Table H-3 EEPROM control bits description

E1ERA	E1LAT	E1PGM	Description
0	0	0	Read condition
0	1	0	Ready to load address/data for program/erase
0	1	1	Byte programming in progress
1	1	0	Ready for byte erase (load address)
1	1	1	Byte erase in progress

Note: The E1PGM and E1ERA bits are cleared when the E1LAT bit is at zero.

Table H-10 A/D characteristics for 3.3V operation

(V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 to +85°C)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics (V_{RH} = V_{DD} and V_{RL} = 0V)	—	± 1	LSB
Quantization error	Uncertainty due to converter resolution	—	± 1	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	± 2	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
ΔV_R	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion Internal RC oscillator	—	32	µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when V_{IN} = V_{RL}	00	—	Hex
Full scale reading	Conversion result when V_{IN} = V_{RH}	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling Internal RC oscillator(1)	—	12	µs
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(2)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Source impedances greater than 10kΩ will adversely affect internal charging time during input sampling.

(2) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 8-2).