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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	15KB (15K x 8)
Program Memory Type	OTP
EEPROM Size	256 x 8
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	56-SDIP (0.600", 15.24mm)
Supplier Device Package	56-PSDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc705b16ncbe

2.3 ‘Jump to any address’

The ‘jump to any address’ mode is entered when the reset pin is released to V_{DD}, if the following conditions are satisfied:

- $\overline{IRQ}$ at 2xV_{DD}
- TCAP1 at V_{DD}
- PD3 at V_{DD} for at least 30 machine cycles after reset
- PD4 at V_{DD} for at least 30 machine cycles after reset

This function allows execution of programs previously loaded in RAM or EEPROM using the methods outlined in Section 2.2.

To execute the ‘jump to any address’ function, data input at port A has to be $CC and data input at port B and port C should represent the MSB and LSB respectively, of the address to jump to for execution of the user program. A schematic diagram of the circuit required is shown in Figure 2-2.

2.4.2 WAIT

The WAIT instruction places the MCU in a low power consumption mode, but WAIT mode consumes more power than STOP mode. All CPU action is suspended and the watchdog is disabled, but the timer, A/D and SCI systems remain active and operate as normal (see flowchart in Figure 2-3). All other memory and registers remain unaltered and all parallel input/output lines remain unchanged. The programming or erase mechanism of the EEPROM is also unaffected, as well as the charge pump high voltage generator.

During WAIT mode the I-bit in the CCR is cleared to enable all interrupts. The INTE bit in the miscellaneous register (Section 2.5) is not affected by WAIT mode. When any interrupt or reset is sensed, the program counter vectors to the locations containing the start address of the interrupt or reset service routine.

Any $\overline{\text{IRQ}}$, timer (overflow, input capture or output compare) or SCI interrupt (in addition to a logic low on the $\overline{\text{RESET}}$ pin) causes the processor to exit WAIT mode.

If a non-reset exit from WAIT mode is performed (i.e. timer overflow interrupt exit), the state of the remaining systems will be unchanged.

If a reset exit from WAIT mode is performed the entire system reverts to the disabled reset state.

Note: The stacking corresponding to an eventual interrupt to leave WAIT mode will only be executed when leaving WAIT mode.

The following list summarizes the effect of WAIT mode on the modules of the MC68HC05B6.

- The watchdog timer functions according to the mask option selected; refer to Section 9.1.4.2
- The EEPROM is not affected; refer to Section 3.7
- The SCI is not affected; refer to Section 6.14
- The timer is not affected; refer to Section 5.7
- The PLM is not affected; refer to Section 7.4
- The A/D converter is not affected; refer to Section 8.4
- The I-bit in the CCR is cleared

2.4.2.1 Power consumption during WAIT mode

Power consumption during WAIT mode depends on how many systems are active. The power consumption will be highest when all the systems (A/D, timer, EEPROM and SCI) are active, and lowest when the EEPROM erase and programming mechanism, SCI and A/D are disabled. The timer cannot be disabled in WAIT mode. It is important that before entering WAIT mode, the programmer sets the relevant control bits for the individual modules to reflect the desired functionality during WAIT mode.

Power consumption may be further reduced by the use of SLOW mode.

SFA — Slow or fast mode selection for PLMA (see Section 7.1)

This bit allows the user to select the slow or fast mode of the PLMA pulse length modulation output.

1 (set) – Slow mode PLMA (4096 x timer clock period).

0 (clear) – Fast mode PLMA (256 x timer clock period).

SFB — Slow or fast mode selection for PLMB (see Section 7.1)

This bit allows the user to select the slow or fast mode of the PLMB pulse length modulation output.

1 (set) – Slow mode PLMB (4096 x timer clock period).

0 (clear) – Fast mode PLMB (256 x timer clock period).

Note: The highest speed of the PLM system corresponds to the frequency of the TOF bit being set, multiplied by 256. The lowest speed of the PLM system corresponds to the frequency of the TOF bit being set, multiplied by 16.

Warning: Because the SFA bit and SFB bit are not double buffered, it is mandatory to set the SFA bit and SFB bit to the desired values before writing to the PLM registers; not doing so could temporarily give incorrect values at the PLM outputs.

SM — Slow mode (see Section 2.4.3)

1 (set) – The system runs at a bus speed 16 times lower than normal ($f_{OSC}/32$). SLOW mode affects all sections of the device, including SCI, A/D and timer.

0 (clear) – The system runs at normal bus speed ($f_{OSC}/2$).

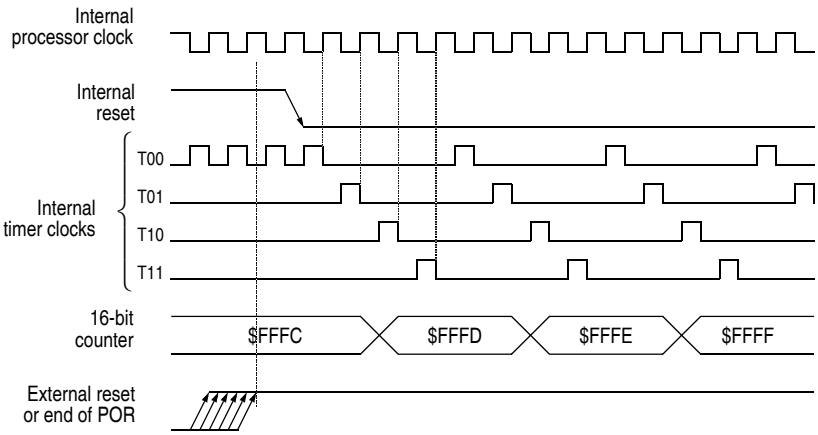
The SM bit is cleared by external or power-on reset. The SM bit is automatically cleared when entering STOP mode.

WDOG — Watchdog enable/disable (see Section 9.1.4)

The WDOG bit can be used to enable the watchdog timer previously disabled by a mask option. Following a watchdog reset the state of the WDOG bit is as defined by the mask option specified. Once the watchdog is enabled, the WDOG bit acts as a reset mechanism for the watchdog counter. Writing a'1' to this bit clears the counter to its initial value and prevents a watchdog timeout.

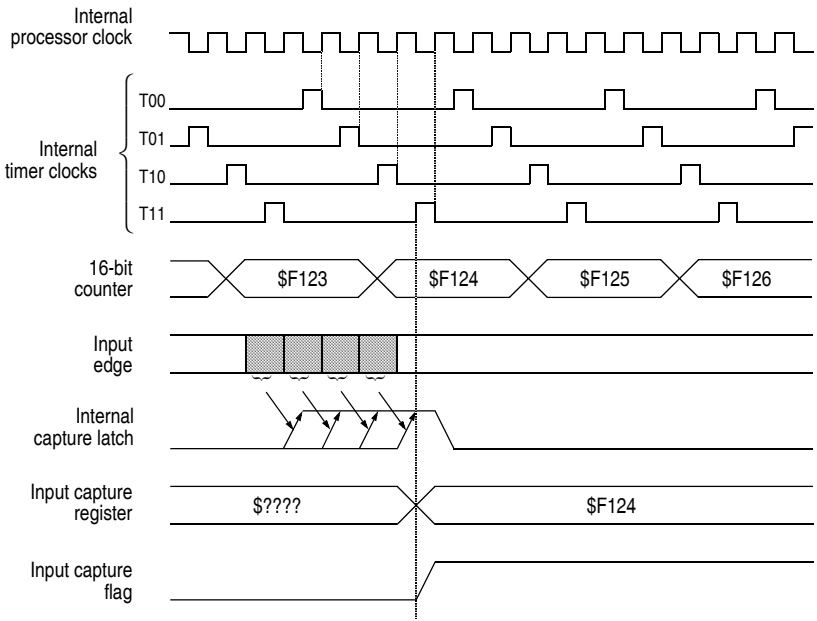
1 (set) – Watchdog counter cleared and enabled.

0 (clear) – The watchdog cannot be disabled by software; writing a zero to this bit has no effect.



Note: The counter and timer control registers are the only ones affected by power-on or external reset.

Figure 5-2 Timer state timing diagram for reset



Note: If the input edge occurs in the shaded area from one timer state T10 to the next timer state T10, then the input capture flag will be set during the next T11 state.

Figure 5-3 Timer state timing diagram for input capture

6.11.3 Serial communications control register 2 (SCCR2)

The SCI control register 2 (SCCR2) provides the control bits that enable/disable individual SCI functions.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
SCI control (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000

TIE — Transmit interrupt enable

1 (set) – TDRE interrupts enabled.

0 (clear) – TDRE interrupts disabled.

TCIE — Transmit complete interrupt enable

1 (set) – TC interrupts enabled.

0 (clear) – TC interrupts disabled.

RIE — Receiver interrupt enable

1 (set) – RDRF and OR interrupts enabled.

0 (clear) – RDRF and OR interrupts disabled.

ILIE — Idle line interrupt enable

1 (set) – IDLE interrupts enabled.

0 (clear) – IDLE interrupts disabled.

TE — Transmitter enable

When the transmit enable bit is set, the transmit shift register output is applied to the TDO line and the corresponding clocks are applied to the SCLK pin. Depending on the state of control bit M (SCCR1), a preamble of 10 (M = 0) or 11 (M = 1) consecutive ones is transmitted when software sets the TE bit from a cleared state.

If a transmission is in progress and a zero is written to TE, the transmitter will wait until after the present byte has been transmitted before placing the TDO and the SCLK pin in the idle, high impedance state.

If the TE bit has been written to a zero and then set to a one before the current byte is transmitted, the transmitter will wait for that byte to be transmitted and will then initiate transmission of a new preamble. After this latest transmission, and provided the TDRE bit is set (no new data to transmit), the line remains idle (driven high while TE = 1); otherwise, normal transmission occurs. This function allows the user to neatly terminate a transmission sequence.

6.13 SCI during STOP mode

When the MCU enters STOP mode, the baud rate generator driving the receiver and transmitter is shut down. This stops all SCI activity. Both the receiver and the transmitter are unable to operate.

If the STOP instruction is executed during a transmitter transfer, that transfer is halted. When STOP mode is exited as a result of an external interrupt, that particular transmission resumes.

If the receiver is receiving data when the STOP instruction is executed, received data sampling is stopped (baud generator stops) and the rest of the data is lost.

Warning: For the above reasons, all SCI transactions should be in the idle state when the STOP instruction is executed.

6.14 SCI during WAIT mode

The SCI system is not affected by WAIT mode and continues normal operation. Any valid SCI interrupt will wake-up the system. If required, the SCI system can be disabled prior to entering WAIT mode by writing a zero to the transmitter and receiver enable bits in the serial communication control register 2 at $000F. This action will result in a reduction of power consumption during WAIT mode.

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8
ANALOG TO DIGITAL CONVERTER

The analog to digital converter system consists of a single 8-bit successive approximation converter and a sixteen channel multiplexer. Eight of the channels are connected to the PD0/AN0 – PD7/AN7 pins of the MC68HC05B6 and the other eight channels are dedicated to internal reference points for test functions. The channel input pins do not have any internal output driver circuitry connected to them because such circuitry would load the analog input signals due to output buffer leakage current. There is one 8-bit result data register (address $08) and one 8-bit status/control register (address $09).

The A/D converter is ratiometric and two dedicated pins, VRH and VRL, are used to supply the reference voltage levels for all analog inputs. These pins are used in preference to the system power supply lines because any voltage drops in the bonding wires of the heavily loaded supply pins could degrade the accuracy of the A/D conversion. An input voltage equal to or greater than V_{RH} converts to $FF (full scale) with no overflow indication and an input voltage equal to V_{RL} converts to $00.

The A/D converter can operate from either the bus clock or an internal RC type oscillator. The internal RC type oscillator is activated by the ADRC bit in the A/D status/control register (ADSTAT) and can be used to give a sufficiently high clock rate to the A/D converter when the bus speed is too low to provide accurate results. When the A/D converter is not being used it can be disconnected, by clearing the ADON bit in the ADSTAT register, in order to save power (see Section 8.2.3).

For further information on A/D converter operation please refer to the M68HC11 Reference Manual — M68HC11RM/AD.

8.1 A/D converter operation

The A/D converter consists of an analog multiplexer, an 8-bit digital to analog converter capacitor array, a comparator and a successive approximation register (SAR) (see Figure 8-1).

There are eleven options that can be selected by the multiplexer; AN0–AN7, VRH, (VRH+VRL)/2 or VRL. Selection is done via the CHx bits in the ADSTAT register (see Section 8.2.3). AN0–AN7 are the only input points for A/D conversion operations; the others are reference points that can be used for test purposes.

8.2 A/D registers

8.2.1 Port D data register (PORTD)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined

Port D is an input-only port which routes the eight analog inputs to the A/D converter. When the A/D converter is disabled, the pins are configured as standard input-only port pins, which can be read via the port D data register.

Note: When the A/D function is enabled, pins PD0–PD7 will act as analog inputs. Using a pin or pins as A/D inputs does not affect the ability to read port D as static inputs; however, reading port D during an A/D conversion sequence may inject noise on the analog inputs and result in reduced accuracy of the A/D result.
Performing a digital read of port D with levels other than V_{DD} or V_{SS} on the pins will result in greater power dissipation during the read cycle, and may give unpredictable results on the corresponding port D pins.

8.2.2 A/D result data register (ADDATA)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
A/D data (ADDATA)	$0008									0000 0000

ADDATA is a read-only register which is used to store the results of A/D conversions. Each result is loaded into the register from the SAR and the conversion complete flag, COCO, in the ADSTAT register is set.

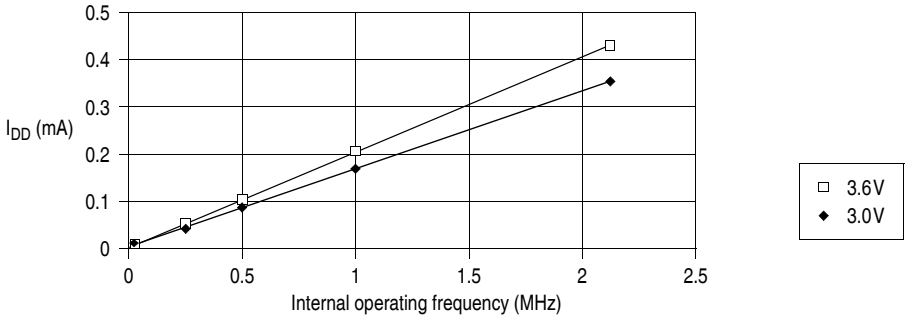


Figure 11-10 Wait I_{DD} (SM = 1) vs internal operating frequency (3V, 3.6V)

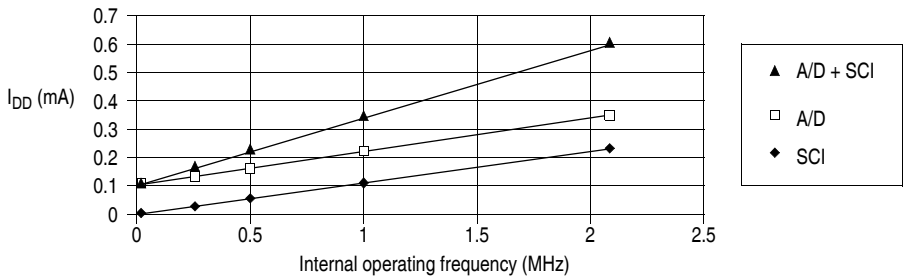


Figure 11-11 Increase in I_{DD} vs frequency for A/D, SCI systems active, V_{DD} = 3.6V

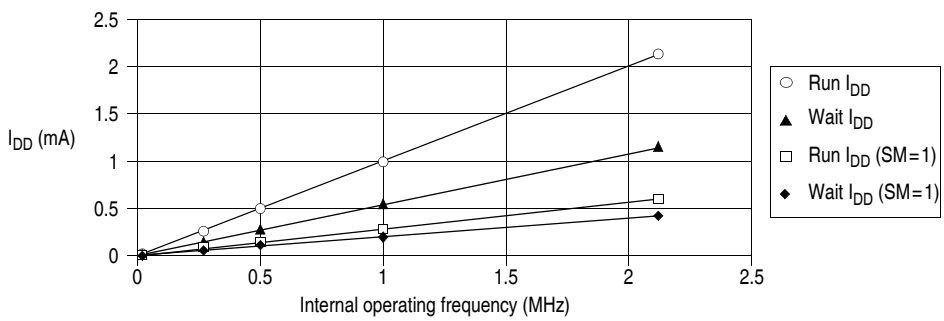
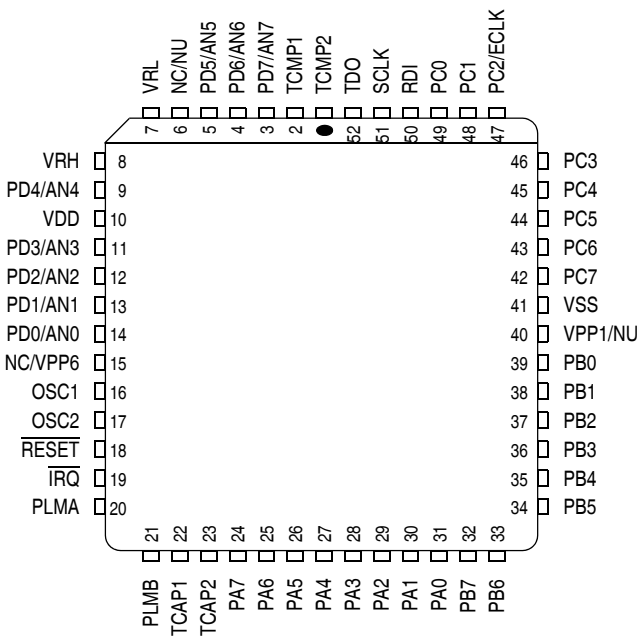


Figure 11-12 I_{DD} vs mode vs internal operating frequency, V_{DD} = 3.6V

12
MECHANICAL DATA

12.1 MC68HC05B family pin configurations

12.1.1 52-pin plastic leaded chip carrier (PLCC)



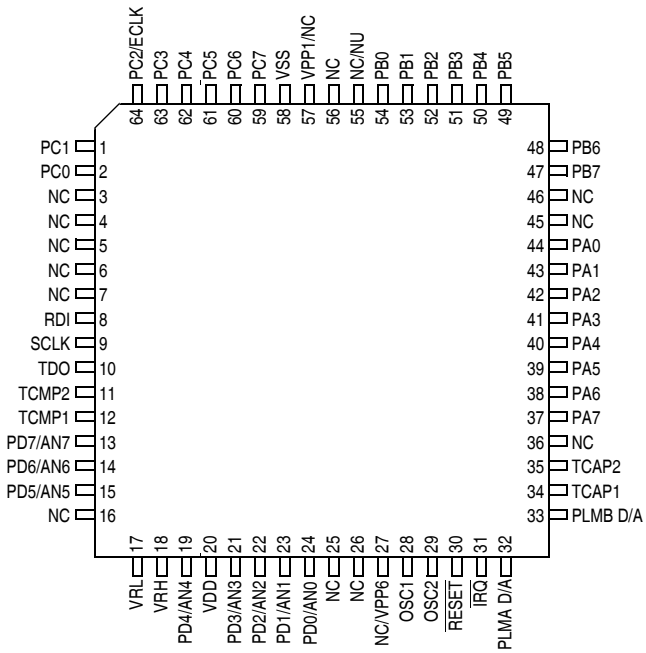
Device	Pin 6	Pin 15	Pin 40
MC68HC05B4	NC	NC	NU
MC68HC05B6	NC	NC	VPP1
MC68HC05B8	NC	NC	VPP1
MC68HC05B16	NC	NC	VPP1
MC68HC05B32	NC	NC	VPP1
MC68HC705B5	NC	VPP6	NU
MC68HC705B16	NU	VPP6	VPP1
MC68HC705B16N	NU	VPP6	VPP1
MC68HC705B32	NU	VPP6	VPP1

NC = Not connected

NU = Non-user pin (Should be tied to V_{SS} in an electrically noisy environment)

Figure 12-1 52-pin PLCC pinout for the MC68HC05B6

12.1.2 64-pin quad flat pack (QFP)



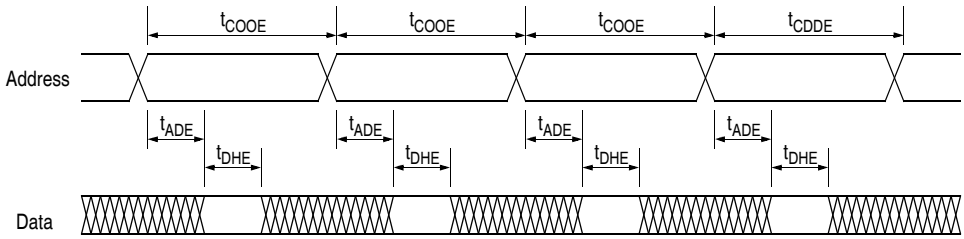
Device	Pin 27	Pin 55	Pin 57
MC68HC05B4	NC	NC	NC
MC68HC05B6 MC68HC05B8 MC68HC05B16 MC68HC05B32	NC	NC	VPP1
MC68HC705B5	Not available in this package		
MC68HC705B16	VPP6	NU	VPP1
MC68HC705B16N	VPP6	NU	VPP1
MC68HC705B32	VPP6	NC	VPP1

NC = Not connected

NU = Non-user pin (Should be tied to V_{SS} in an electrically noisy environment)

Figure 12-2 64-pin QFP pinout for the MC68HC05B6

C.5.5 Bootstrap loader timing diagrams



t_{ADE} max (address to data delay)	5 machine cycles
t_{DHA} min (data hold time)	14 machine cycles
t_{COOE} (load cycle time)	117 machine cycles < t_{COOE} < 150 machine cycles
t_{CDDE} (programming cycle time)	t_{COOE} + t_{PROG} (5 ms nominal)

1 machine cycle = $1/(2f_0(Xtal))$

Figure C-9 EPROM parallel bootstrap loader timing diagram

EPROM will not be available for code execution while the E6LAT bit is set. The V_{PP6} switching must occur externally after the E6PGM bit is set, for example under control of a signal generated on a pin by the programming routine.

Note: When the part becomes a PROM, only the cumulative programming of bits to logic ‘1’ is possible if multiple programming is made on the same byte.

To allow simultaneous programming of up to eight bytes, these bytes must be in the same group of addresses which share the same most significant address bits; only the three least significant bits can change.

E.3.3 EPROM/EEPROM/ECLK control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EPROM/EEPROM/ECLK control	$0007			E6LAT	E6PGM	ECLK	E1ERA	E1LAT	E1PGM	0000 0000

E6LAT — EPROM programming latch enable bit

1 (set) – Address and up to eight data bytes can be latched into the EPROM for further programming providing the E6PGM bit is cleared.

0 (clear) – Data can be read from the EPROM or firmware ROM; the E6PGM bit is reset to zero when E6LAT is ‘0’.

STOP, power-on and external reset clear the E6LAT bit.

Note: After the t_{ERA1} erase time or t_{PROG1} programming time, the E6LAT bit has to be reset to zero in order to clear the E6PGM bit.

E6PGM — EPROM program enable bit

This bit is the EPROM program enable bit. It can be set to ‘1’ to enable programming only after E6LAT is set and at least one byte is written to the EPROM. It is not possible to clear this bit using software but clearing E6LAT will always clear E6PGM.

Table E-2 EPROM control bits description

E6LAT	E6PGM	Description
0	0	Read/execute in EPROM
1	0	Ready to write address/data to EPROM
1	1	programming in progress

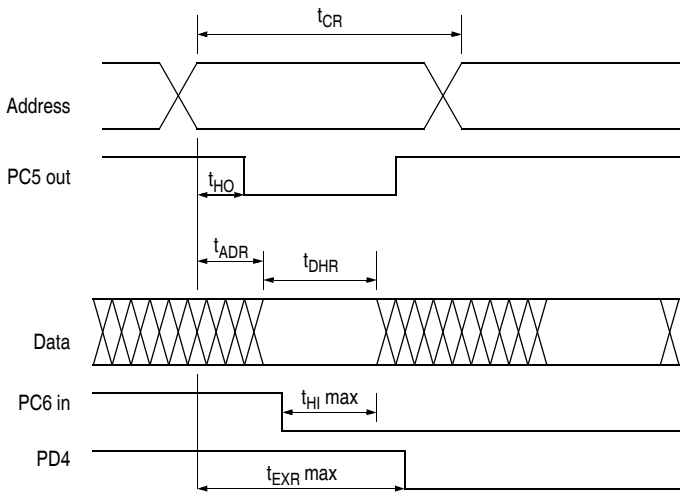
Note: The E6PGM bit can never be set while the E6LAT bit is at zero.

E.4.4 RAM parallel bootstrap

The program first checks the state of the security bit. If the SEC bit is active, i.e. ‘0’, the program will not enter the RAM bootstrap mode and the red LED will flash. Otherwise the RAM bootstrap program will start loading the RAM with external data (e.g. from a 2564 or 2764 EPROM). Before loading a new byte the state of the PD4/AN4 pin is checked. If this pin goes to level ‘0’, or if the RAM is full, then control is given to the loaded program at address $0050. See Figure E-3 and Figure E-4.

If the data is supplied by a parallel interface, handshaking will be provided by PC5 and PC6 according to Figure E-9. If the data comes from an external EPROM, the handshake can be disabled by connecting together PC5 and PC6.

Figure E-10 provides a schematic diagram of a circuit that can be used to load the RAM with short test programs. Up to 8 programs can be loaded in turn from the EPROM. Selection is accomplished by means of the switches connected to the EPROM higher address lines (A8 through A10). If the user program sets PC0 to level ‘1’, this will disable the external EPROM, thus rendering both port A output and port B input available. The EPROM parallel bootstrap loader schematic can also be used (Figure E-7), provided VPP is at V_{DD} level. The high order address lines will be at zero. The LEDs will stay off.



t_{ADR} max (address to data delay; PC6=PC5)	16 machine cycles
t_{DHR} min (data hold time)	4 machine cycles
t_{CR} (load cycle time; PC6=PC5)	49 machine cycles
t_{HO} (PC5 handshake out delay)	5 machine cycles
t_{HI} max (PC6 handshake in, data hold time)	10 machine cycles
t_{EXR} max (max delay for transition to be recognised during this cycle; PC6=PC5	30 machine cycles

1 machine cycle = $1/(2f_0(Xtal))$

Figure E-9 Parallel RAM loader timing diagram

E.5 Absolute maximum ratings

Table E-6 Absolute maximum ratings

Rating	Symbol	Value	Unit
Supply voltage(1)	V_{DD}	– 0.5 to +7.0	V
Input voltage (Except V_{PP1} and V_{PP6})	V_{IN}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input voltage – Self-check mode ($\overline{IRQ}$ pin only)	V_{IN}	V_{SS} – 0.5 to $2V_{DD}$ + 0.5	V
Operating temperature range – Standard (MC68HC705B16) – Extended (MC68HC705B16C) – Industrial (MC68HC705B16V) – Automotive (MC68HC705B16M)	T_A	T_L to T_H 0 to +70 –40 to +85 –40 to +105 –40 to +125	°C
Storage temperature range	T_{STG}	– 65 to +150	°C
Current drain per pin (excluding VDD and VSS)(2) – Source – Sink	 I_D I_S	 25 45	 mA mA

(1) All voltages are with respect to V_{SS}.

(2) Maximum current drain per pin is for one pin at a time, limited by an external resistor.

Note: This device contains circuitry designed to protect against damage due to high electrostatic voltages or electric fields. However, it is recommended that normal precautions be taken to avoid the application of any voltages higher than those given in the maximum ratings table to this high impedance circuit. For maximum reliability all unused inputs should be tied to either V_{SS} or V_{DD}.

F.6 Absolute maximum ratings

Table F-6 Absolute maximum ratings

Rating	Symbol	Value	Unit
Supply voltage(1)	V_{DD}	– 0.5 to +7.0	V
Input voltage (Except V_{PP1} and V_{PP6})	V_{IN}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input voltage – Self-check mode ($\overline{IRQ}$ pin only)	V_{IN}	V_{SS} – 0.5 to $2V_{DD}$ + 0.5	V
Operating temperature range – Standard (MC68HC705B16N) – Extended (MC68HC705B16NC) – Industrial (MC68HC705B16NV) – Automotive (MC68HC705B16NM)	T_A	T_L to T_H 0 to +70 –40 to +85 –40 to +105 –40 to +125	°C
Storage temperature range	T_{STG}	– 65 to +150	°C
Current drain per pin (excluding VDD and VSS)(2) – Source – Sink	 I_D I_S	 25 45	 mA mA

(1) All voltages are with respect to V_{SS}.

(2) Maximum current drain per pin is for one pin at a time, limited by an external resistor.

Note: This device contains circuitry designed to protect against damage due to high electrostatic voltages or electric fields. However, it is recommended that normal precautions be taken to avoid the application of any voltages higher than those given in the maximum ratings table to this high impedance circuit. For maximum reliability all unused inputs should be tied to either V_{SS} or V_{DD}.

F.7 DC electrical characteristics

Table F-7 DC electrical characteristics for 5V operation

(V_{DD} = 5 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage					
I_{LOAD} = – 10 µA	V_{OH}	V_{DD} – 0.1	—	—	V
I_{LOAD} = +10 µA	V_{OL}	—	—	0.1	
Output high voltage (I_{LOAD} = 0.8 mA)					
PA0–7, PB0–7, PC0–7, TCMP1, TCMP2	V_{OH}	V_{DD} – 0.8	V_{DD} – 0.4	—	V
Output high voltage (I_{LOAD} = 1.6 mA)					
TDO, SCLK, PLMA, PLMB	V_{OH}	V_{DD} – 0.8	V_{DD} – 0.4	—	
Output low voltage (I_{LOAD} = 1.6 mA)					
PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB	V_{OL}	—	0.1	0.4	V
Output low voltage (I_{LOAD} = 1.6 mA)					
$\overline{RESET}$	V_{OL}		0.4	1	
Input high voltage					
PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	$0.7V_{DD}$	—	V_{DD}	V
Input low voltage					
PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	$0.2V_{DD}$	V
Supply current[3]					
RUN (SM = 0) (See Figure 11-1)	I_{DD}	—	5.0	6	mA
RUN (SM = 1) (See Figure 11.2)	I_{DD}	—	1.0	1.5	mA
WAIT (SM = 0) (See Figure 11-3)	I_{DD}	—	1.5	2	mA
WAIT (SM = 1) (See Figure 11-4)	I_{DD}	—	0.9	1	mA
STOP					
0 to 70 (standard)	I_{DD}	—	2	10	µA
– 40 to 85 (extended)	I_{DD}	—	—	20	µA
– 40 to 105 (industrial)	I_{DD}	—	—	60	µA
– 40 to 125 (automotive)	I_{DD}	—	—	100	µA
High-Z leakage current					
PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	±0.2	±1	µA
Input current					
Port B and port C pull-down (V_{IN}=V_{IH})	I_{RPD}		80		µA
Input current (0 to 70)					
$\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	±0.2	±1	µA
Input current (– 40 to 125)					
$\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	—	±5	µA
Capacitance					
Ports (as input or output), $\overline{RESET}$, TDO, SCLK	C_{OUT}	—	—	12	pF
$\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI	C_{IN}	—	—	8	pF
PD0/AN0–PD7/AN7 (A/D off)	C_{IN}	—	12	—	pF
PD0/AN0–PD7/AN7 (A/D on)	C_{IN}	—	22	—	pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25°C only.

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 4.2MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and $V_{IH} = V_{DD} – 0.2$ V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

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