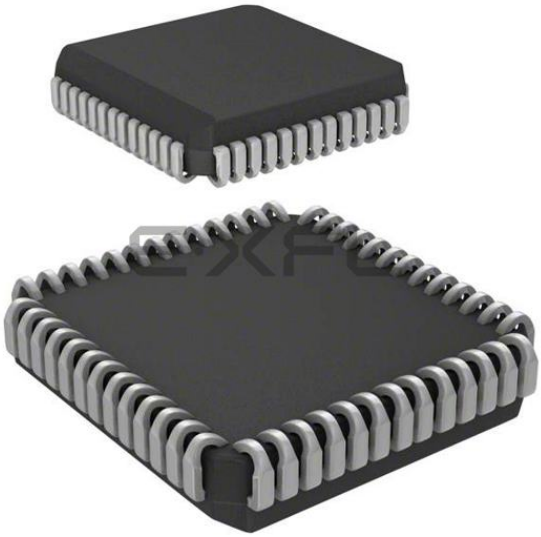

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	15KB (15K x 8)
Program Memory Type	OTP
EEPROM Size	256 x 8
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.1x19.1)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc705b16ncfner

Conventions

Where abbreviations are used in the text, an explanation can be found in the glossary, at the back of this manual. Register and bit mnemonics are defined in the paragraphs describing them.

An overbar is used to designate an active-low signal, eg: $\overline{\text{RESET}}$.

Unless otherwise stated, shaded cells in a register diagram indicate that the bit is either unused or reserved; ‘u’ is used to indicate an undefined state (on reset).

Unless otherwise stated, pins labelled “NU” should be tied to V_{SS} in an electrically noisy environment. Pins labelled “NC” can be left floating, since they are not bonded to any part of the device.

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CPU CORE AND INSTRUCTION SET

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INTRODUCTION

The MC68HC05B6 microcomputer (MCU) is a member of Freescale's MC68HC05 family of low-cost single chip microcomputers. This 8-bit MCU contains an on-chip oscillator, CPU, RAM, ROM, EEPROM, A/D converter, pulse length modulated outputs, I/O, serial communications interface, programmable timer system and watchdog. The fully static design allows operation at frequencies down to dc to further reduce the already low power consumption to a few micro-amps.

This data sheet is structured such that devices similar to the MC68HC05B6 are described in a set of appendices (see Table 1-1).

Table 1-1 Data sheet appendices

Device	Appendix	Differences from MC68HC05B6
MC68HC05B4	A	4K bytes ROM; no EEPROM
MC68HC05B8	B	7.25K bytes ROM
MC68HC705B5	C	6K bytes EPROM; self-check replaced by bootstrap firmware; no EEPROM
MC68HC05B16	D	16K bytes ROM; increased RAM and self-check ROM
MC68HC705B16	E	16K bytes EPROM; increased RAM; self-check replaced by bootstrap firmware; modified power-on reset routine
MC68HC705B16N	F	16K bytes EPROM; increased RAM; self-check replaced by bootstrap firmware; modified power-on reset routine
MC68HC05B32	G	32K bytes ROM; no page zero ROM; increased RAM
MC68HC705B32	H	32K bytes EPROM; no page zero ROM; increased RAM; self-check mode replaced by bootstrap firmware

2.5 Pin descriptions

2.5.1 VDD and VSS

Power is supplied to the microcontroller using these two pins. VDD is the positive supply and VSS is ground.

It is in the nature of CMOS designs that very fast signal transitions occur on the MCU pins. These short rise and fall times place very high short-duration current demands on the power supply. To prevent noise problems, special care must be taken to provide good power supply by-passing at the MCU. By-pass capacitors should have good high-frequency characteristics and be as close to the MCU as possible. Bypassing requirements vary, depending on how heavily the MCU pins are loaded.

2.5.2 $\overline{\text{IRQ}}$

This is an input-only pin for external interrupt sources. Interrupt triggering is selected using the INTP and INTN bits in the miscellaneous register, to be one of four options detailed in Table 9-3. In addition, the external interrupt facility ($\overline{\text{IRQ}}$) can be disabled using the INTE bit in the miscellaneous register (see Section 3.8). It is only possible to change the interrupt option bits in the miscellaneous register while the I-bit is set. Selecting a different interrupt option will automatically clear any pending interrupts. Further details of the external interrupt procedure can be found in Section 9.2.3.1.

The $\overline{\text{IRQ}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity.

2.5.3 $\overline{\text{RESET}}$

This active low I/O pin is used to reset the MCU. Applying a logic zero to this pin forces the device to a known start-up state. An external RC-circuit can be connected to this pin to generate a power-on-reset (POR) if required. In this case, the time constant must be great enough to allow the oscillator circuit to stabilize. This input has an internal Schmitt trigger to improve noise immunity. When a reset condition occurs internally, i.e. from the COP watchdog, the $\overline{\text{RESET}}$ pin provides an active-low open drain output signal that may be used to reset external hardware.

2.5.4 TCAP1

The TCAP1 input controls the input capture 1 function of the on-chip programmable timer system.

5.2 Timer control and status

The various functions of the timer are monitored and controlled using the timer control and status registers described below.

5.2.1 Timer control register (TCR)

The timer control register ($0012) is used to enable the input captures (ICIE), output compares (OCIE), and timer overflow (TOIE) functions as well as forcing output compares (FOLV1 and FOLV2), selecting input edge sensitivity (IEDG1) and levels of output polarity (OLV1 and OLV2).

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0

ICIE — Input captures interrupt enable

If this bit is set, a timer interrupt is enabled whenever the ICF1 or ICF2 status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

OCIE — Output compares interrupt enable

If this bit is set, a timer interrupt is enabled whenever the OCF1 or OCF2 status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

TOIE — Timer overflow interrupt enable

If this bit is set, a timer interrupt is enabled whenever the TOF status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

5.4 Output compare

'Output compare' is a technique which may be used, for example, to generate an output waveform, or to signal when a specific time period has elapsed, by presetting the output compare register to the appropriate value.

There are two output compare registers: output compare register 1 (OCR1) and output compare register 2 (OCR2), both of which are read or write registers.

Note: The same output compare interrupt enable bit (OCIE) is used for the two output compares.

5.4.1 Output compare register 1 (OCR1)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined

The 16-bit output compare register 1 is made up of two 8-bit registers at locations $16 (MSB) and $17 (LSB). The contents of the output compare register 1 are compared with the contents of the free-running counter continually and, if a match is found, the corresponding output compare flag (OCF1) in the timer status register is set and the output level (OLVL1) is transferred to pin TCMP1. The output compare register 1 values and the output level bit should be changed after each successful comparison to establish a new elapsed timeout. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit (OCIE) is set. (The free-running counter is updated every four internal bus clock cycles.)

After a processor write cycle to the output compare register 1 containing the MSB ($16), the output compare function is inhibited until the LSB ($17) is also written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($17) will not inhibit the compare 1 function. The processor can write to either byte of the output compare register 1 without affecting the other byte. The output level (OLVL1) bit is clocked to the output level register and hence to the TCMP1 pin whether the output compare flag 1 (OCF1) is set or clear. The minimum time required to update the output compare register 1 is a function of the program rather than the internal hardware. Because the output compare flag 1 and the output compare register 1 are not defined at power on, and not affected by reset, care must be taken when initializing output compare functions with software. The following procedure is recommended:

- Write to output compare high 1 to inhibit further compares;
- Read the timer status register to clear OCF1 (if set);
- Write to output compare low 1 to enable the output compare 1 function.

6.6.1 Idle line wake-up

In idle line wake-up mode, a dormant receiver wakes up as soon as the RDI line becomes idle. Idle is defined as a continuous logic high level on the RDI line for ten (or eleven) full bit times. Systems using this type of wake-up must provide at least one character time of idle between messages to wake up sleeping receivers, but must not allow any idle time between characters within a message.

6.6.2 Address mark wake-up

In address mark wake-up, the most significant bit (MSB) in a character is used to indicate whether it is an address (1) or data (0) character. Sleeping receivers will wake up whenever an address character is received. Systems using this method for wake-up would set the MSB of the first character of each message and leave it clear for all other characters in the message. Idle periods may be present within messages and no idle time is required between messages for this wake-up method.

6.7 Receive data in (RDI)

Receive data is the serial data that is applied through the input line and the SCI to the internal bus. The receiver circuitry clocks the input at a rate equal to 16 times the baud rate. This time is referred to as the RT rate in Figure 6-4 and as the receiver clock in Figure 6-2.

The receiver clock generator is controlled by the baud rate register, as shown in Figure 6-1 and Figure 6-2; however, the SCI is synchronized by the start bit, independent of the transmitter.

Once a valid start bit is detected, the start bit, each data bit and the stop bit are sampled three times at RT intervals 8 RT, 9 RT and 10 RT (1 RT is the position where the bit is expected to start), as shown in Figure 6-5. The value of the bit is determined by voting logic which takes the value of the majority of the samples. A noise flag is set when all three samples on a valid start bit or data bit or the stop bit do not agree.

6.8 Start bit detection

When the input (idle) line is detected low, it is tested for three more sample times (referred to as the start edge verification samples in Figure 6-4). If at least two of these three verification samples detect a logic zero, a valid start bit has been detected, otherwise the line is assumed to be idle. A noise flag is set if one of the three verification samples detect a logic one, thus a valid start bit could be assumed with a set noise flag present.

6.10 SCI synchronous transmission

The SCI transmitter allows the user to control a one way synchronous serial transmission. The SCLK pin is the clock output of the SCI transmitter. No clocks are sent to that pin during start bit and stop bit. Depending on the state of the LBCL bit (bit 0 of SCCR1), clocks will or will not be activated during the last valid data bit (address mark). The CPOL bit (bit 2 of SCCR1) allows the user to select the clock polarity, and the CPHA bit (bit 1 of SCCR1) allows the user to select the phase of the external clock (see Figure 6-8, Figure 6-9 and Figure 6-10).

During idle, preamble and send break, the external SCLK clock is not activated.

These options allow the user to serially control peripherals which consist of shift registers, without losing any functions of the SCI transmitter which can still talk to other SCI receivers. These options do not affect the SCI receiver which is independent of the transmitter.

The SCLK pin works in conjunction with the TDO pin. When the SCI transmitter is disabled (TE = 0), the SCLK and TDO pins go to the high impedance state.

Note: The LBCL, CPOL and CPHA bits have to be selected before enabling the transmitter to ensure that the clocks function correctly. These bits should not be changed while the transmitter is enabled.

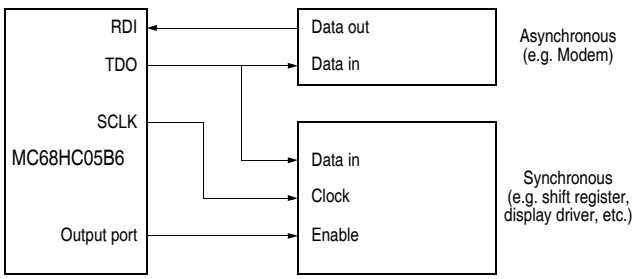


Figure 6-8 SCI example of synchronous and asynchronous transmission

The D/A converter has two data registers associated with it, PLMA and PLMB.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000

This is a dual 8-bit resolution D/A converter associated with two output pins (PLMA and PLMB). The outputs are pulse length modulated signals whose duty cycle ratio may be modified. These signals can be used directly as PLMs, or the filtered average may be used as general purpose analog outputs.

The longest repetition period is 4096 times the programmable timer clock period (CPU clock multiplied by four), and the shortest repetition period is 256 times the programmable timer clock period (the repetition rate frequencies for a 4 MHz crystal are 122 Hz and 1953 Hz respectively). Registers PLMA ($0A) and PLMB ($0B) are associated with the pulse length values of the two counters. A value of $00 loaded into these registers results in a continuously low output on the corresponding D/A output pin. A value of $80 results in a 50% duty cycle output, and so on, to the maximum value $FF corresponding to an output which is at ‘1’ for 255/256 of the cycle. When the MCU makes a write to register PLMA or PLMB the new value will only be picked up by the D/A converters at the end of a complete cycle of conversion. This results in a monotonic change of the DC component at the output without overshoots or vicious starts (a vicious start is an output which gives totally erroneous PLM during the period immediately following an update of the PLM D/A registers). This feature is achieved by double buffering of the PLM D/A registers. Examples of PWM output waveforms are shown in Figure 7-2.

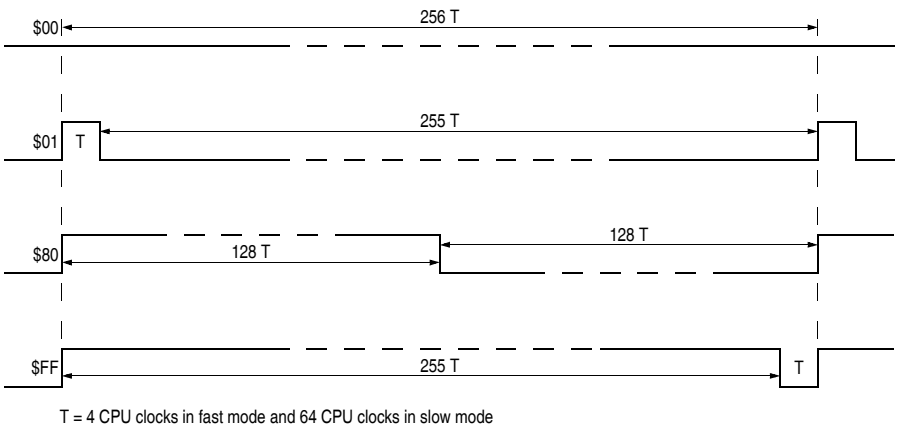


Figure 7-2 PLM output waveform examples

Table 11-7 Control timing for 3.3V operation

(V_{DD} = 3.3Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	2.0	MHz
External clock option	f_{OSC}	dc	2.0	MHz
Internal operating frequency (f_{OSC}/2)				
Using crystal	f_{OP}	—	1.0	MHz
Using external clock	f_{OP}	dc	1.0	MHz
Cycle time (see Figure 9-1)	t_{CYC}	1000	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		5	µs
A/D converter stabilization time	t_{ADON}		500	µs
External $\overline{\text{RESET}}$ input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on $\overline{\text{RESET}}$ output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog $\overline{\text{RESET}}$ output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	30	—	ms
– 40 to 85 (extended)	t_{ERA}	30	—	ms
– 40 to 125 (automotive)	t_{ERA}	30	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	30	—	ms
– 40 to 85 (extended)	t_{PROG}	30	—	ms
– 40 to 125 (automotive)	t_{PROG}	30	—	ms
Timer (see Figure 11-13)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	250	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	250	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width(5)	t_{OH}, t_{OL}	200	—	ns
Write/Erase endurance(6)(7)	—	10000		cycles
Data retention(6)(7)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{CYC}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

(5) t_{OH} and t_{OL} should not total less than 500ns.

(6) At a temperature of 85°C

(7) Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

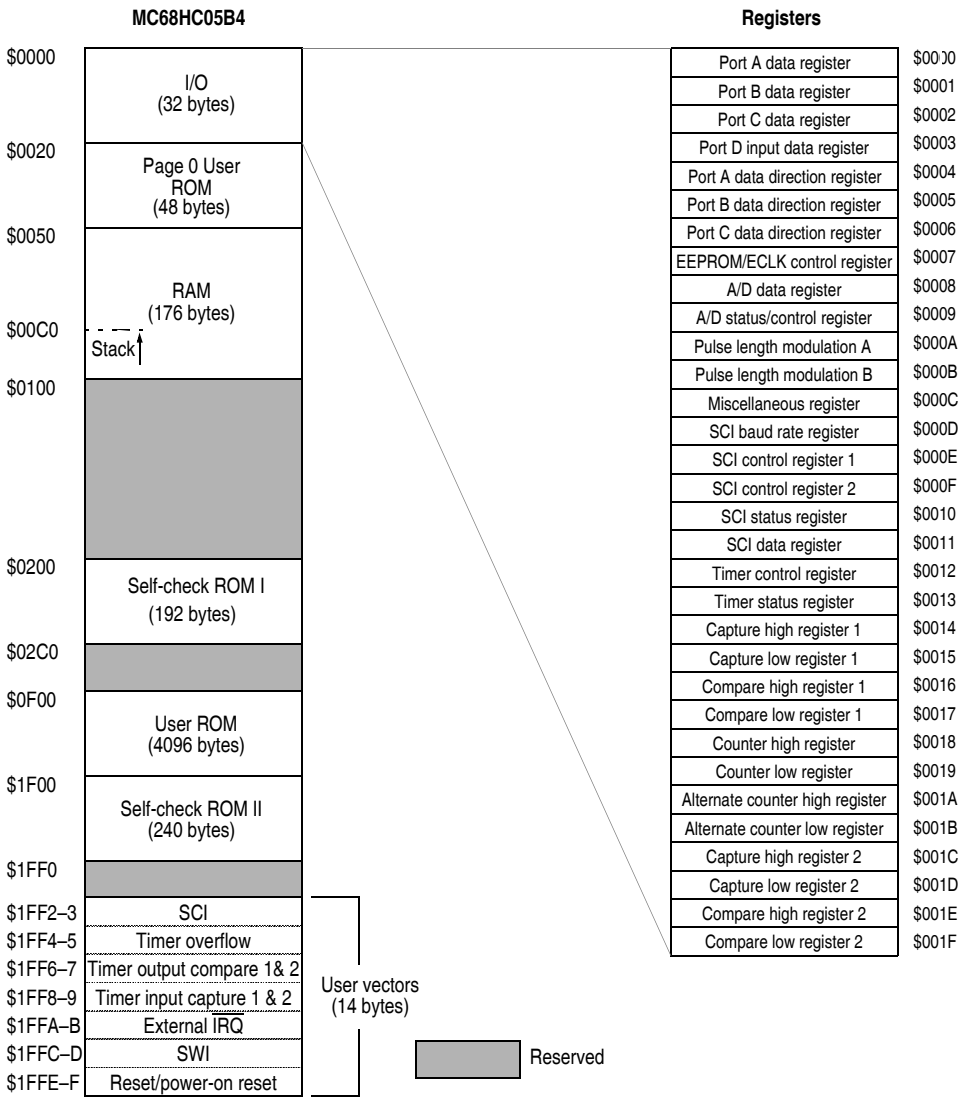
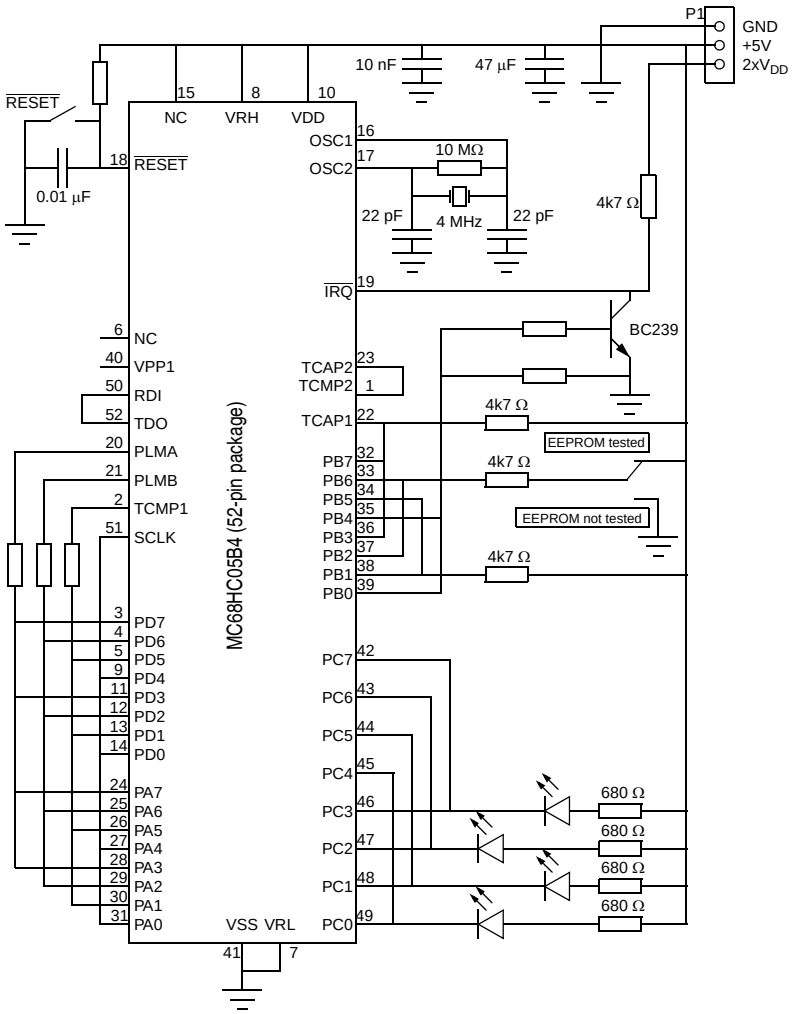


Figure A-2 Memory map of the MC68HC05B4

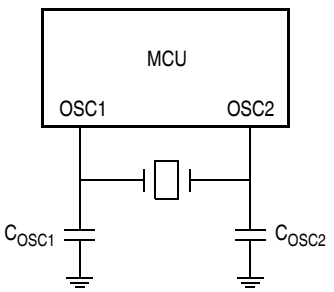


Note: For the MC68HC05B4, switches on PB5 and PB6 have no effect
All resistors are 10 kΩ, unless otherwise stated.

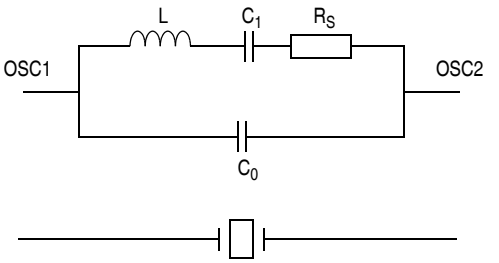
Figure A-3 MC68HC05B4 self-check schematic diagram

D.3 External clock

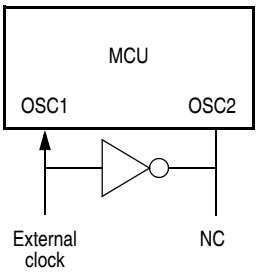
When using an external clock the OSC1 and OSC2 pins should be driven in antiphase, as shown in Figure D-2. The t_{OXOV} or t_{ILCH} specifications (see Section 11.4) do not apply when using an external clock input. The equivalent specification of the external clock source should be used in lieu of t_{OXOV} or t_{ILCH}.



(a) Crystal/ceramic resonator oscillator connections



(b) Crystal equivalent circuit



(c) External clock source connections

Crystal

	2 MHz	4 MHz	Unit
R_S(max)	400	75	Ω
C_0	5	7	pF
C_1	8	12	*f*F
C_{OSC1}	15 – 40	15 – 30	pF
C_{OSC2}	15 – 30	15 – 25	pF
R_P	10	10	MΩ
Q	30 000	40 000	—

Ceramic resonator

	2 – 4 MHz	Unit
R_S(typ)	10	Ω
C_0	40	pF
C_1	4.3	pF
C_{OSC1}	30	pF
C_{OSC2}	30	pF
R_P	1 – 10	MΩ
Q	1250	—

(d) Typical crystal and ceramic resonator parameters

Figure D-2 Oscillator connections

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 2.0 MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and $V_{IH} = V_{DD} - 0.2$ V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

F.5 Bootstrap mode

Oscillator divide-by-two is forced in bootstrap mode.

The 432 bytes of self-check firmware on the MC68HC05B6 are replaced by 576 bytes of bootstrap firmware. A detailed description of the modes of operation within bootstrap mode is given below.

The bootstrap program in mask ROM address locations $0200 to $024F and $3E00 to $3FEF can be used to program the EPROM and the EEPROM, to check if the EPROM is erased or to load and execute data in RAM.

After reset, while going to the bootstrap mode, the vector located at address $3FEE and $3FEF ($\overline{\text{RESET}}$) is fetched to start execution of the bootstrap program. To place the part in bootstrap mode, the $\overline{\text{IRQ}}$ pin should be at $2xV_{DD}$ with the TCAP1 pin 'high' during transition of the $\overline{\text{RESET}}$ pin from low to high. The hold time on the $\overline{\text{IRQ}}$ and TCAP1 pins is two clock cycles after the external $\overline{\text{RESET}}$ pin is brought high.

When the MC68HC705B16N is placed in the bootstrap mode, the bootstrap reset vector will be fetched and the bootstrap firmware will start to execute. Table F-4 shows the conditions required to enter each level of bootstrap mode on the rising edge of $\overline{\text{RESET}}$.

Table F-4 Mode of operation selection

$\overline{\text{IRQ}}$ pin	TCAP1 pin	PD1	PD2	PD3	PD4	Mode
V_{SS} to V_{DD}	V_{SS} to V_{DD}	x	x	x	x	Single chip
$2xV_{DD}$	V_{DD}	0	0	0	0	Erased EPROM verification
$2xV_{DD}$	V_{DD}	0	0	1	0	EPROM verification;
$2xV_{DD}$	V_{DD}	1	0	0	0	EPROM verification; erase EEPROM; EPROM/EEPROM parallel program/verify
$2xV_{DD}$	V_{DD}	1	0	1	0	Erased EPROM verification; erase EEPROM; EPROM parallel program/verify (no E^2)
$2xV_{DD}$	V_{DD}	1	0	0	1	Jump to start of RAM ($0051); SEC bit = NON ACTIVE
$2xV_{DD}$	V_{DD}	x	0	1	1	Serial RAM load/execute – similar to MC68HC05B6 but can fill RAM I and II

x = Don't care

The bootstrap program will first copy part of itself in RAM (except 'RAM parallel load'), as the program cannot be executed in ROM during verification/programming of the EPROM. It will then set the TCMP1 output to a logic high level, unlike the MC68HC05B6 which keeps TCMP1 low. This can be used to distinguish between the two circuits and, in particular, for selection of the VPP level and current capability.

Table G-1 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EEPROM/ECLK control	$0007	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(3)	$0100							EE1P	SEC	Not affected
Mask option register (MOR)(4)	$7FDE				RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) This bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent upon the mask option selected; 1 = watchdog enabled, 0 = watchdog disabled.

(3) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

(4) This register is implemented in ROM; therefore reset has no effect on the individual bits.

H

MC68HC705B32

Maskset errata

This errata section outlines the differences between two previously available masksets (D59J and D40J) and all other masksets. Unless otherwise stated, the main body of Appendix G refers to all these other masksets with any differences being noted in this errata section.

- For the D59J and D40J masksets, the MCU only requires that a logic zero is applied to the $\overline{\text{RESET}}$ input for 1.5 t_{CYC}.
- For D59J, 16 cycle POR delay option (t_{PORL}) is not available
- For the D59J maskset, oscillator divide ratio DIV10 is forced in Bootstrap mode. On all other revisions DIV2 is forced.

For the D59J:

The STOP Idd is greater than the expected value of 120μA at 5 volts Vdd at a temperature of 20°C with the CAN module enabled and in SLEEP mode. Typically the STOP Idd is in the region of 2.0 milliamps at 20°C.

The fault lies with the design of the EPROM array. When the STOP instruction is executed, the next opcode in memory is present on the data bus. A fault in the EPROM write data latch circuitry causes a latch to be driven to logic 0 on both sides when the data bus for that bit is logic 1. This results in increasing STOP Idd of 450μA per data bus bit set to a logic 1. If all data bus bits are set to logic 1 (i.e. next opcode is $FF, STX 0,X) the STOP Idd shall be in the region of 3.6mA.

The minimum STOP Idd is achieved by ensuring the opcode immediately following the STOP instruction is data $00. This corresponds to BRSET 0,ADDRESS,LABEL. If the label points to the next sequential instruction in memory then this has the effect of a 5 cycle NOP but note that the carry bit in the condition code register may be altered by the BRSET instruction.

H.4.4 Mask option register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Mask option register (MOR)(1)	$7FDE				RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) Because this register is implemented in EPROM, reset has no effect on the individual bits.

RTIM

This bit can modify the time t_{PORL}, where the $\overline{\text{RESET}}$ pin is kept low after a power-on reset.

1 (set) – t_{PORL} = 16 cycles.

0 (clear) – t_{PORL} = 4064 cycles.

RWAT

This bit can modify the status of the watchdog counter after reset. Usually, the watchdog system is disabled after power-on or external reset but when this bit is set, it will be active immediately after the following resets (except in bootstrap mode).

WWAT

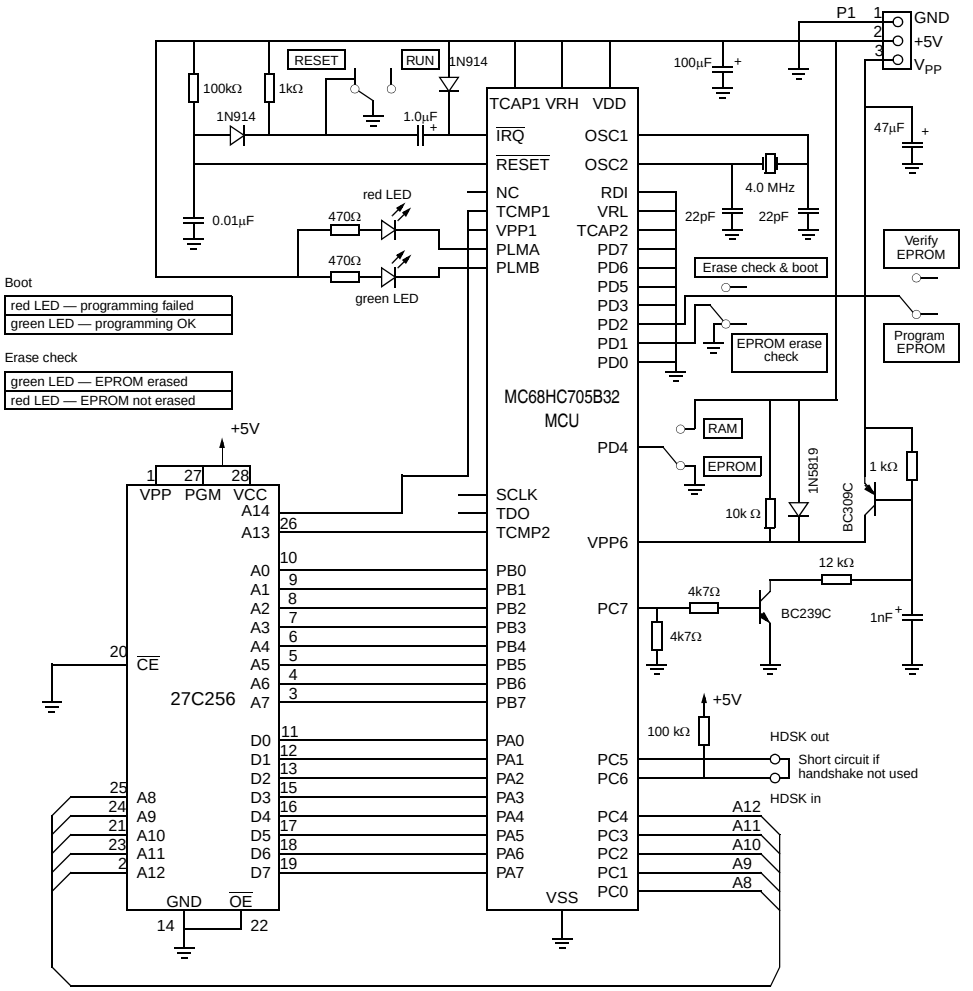
This bit can modify the status of the watchdog counter in WAIT mode. Normally, the watchdog system is disabled in WAIT mode but when this bit is set, the watchdog will be active in WAIT mode.

PBPD

This bit, when programmed, connects a resistive pull-down on all 8 pins of port B. This pull-down, R_{PD}, is active on a given pin only while it is an input.

PCPD

This bit, when programmed, connects a resistive pull-down on all 8 pins of port C. This pull-down, R_{PD}, is active on a given pin only while it is an input.



Note: This circuit is recommended for programming only at 25°C and not for use in the end application, or at temperatures other than 25°C. If used in the end application, VPP6 should be tied to VDD to avoid damaging the device.

Figure H-7 EPROM parallel bootstrap schematic diagram

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