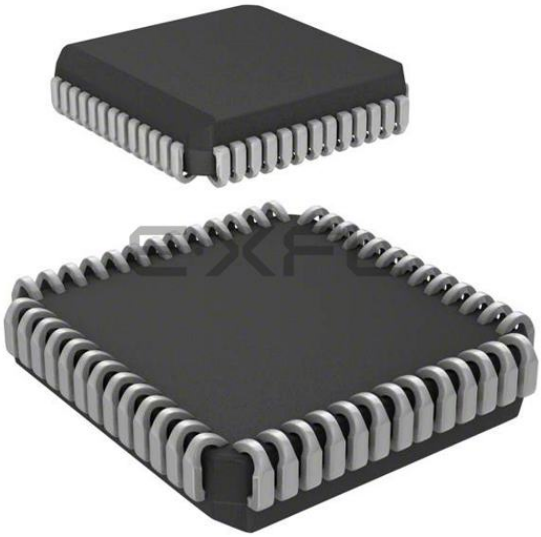

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Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	15KB (15K x 8)
Program Memory Type	OTP
EEPROM Size	256 x 8
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.1x19.1)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc705b16ncfne

MC68HC05B6

High-density Complementary Metal Oxide Semiconductor (HCMOS) Microcomputer Unit

2.2 Serial RAM loader

The ‘load program in RAM and execute’ mode is entered if the following conditions are satisfied when the reset pin is released to V_{DD}. The format used is identical to the format used for the MC68HC805C4. The SEC bit in the options register must be inactive, i.e. set to ‘1’.

- $\overline{IRQ}$ at $2xV_{DD}$
- TCAP1 at V_{DD}
- PD3 at V_{DD} for at least 30 machine cycles after reset
- PD4 at V_{SS} for at least 30 machine cycles after reset

In the ‘load program in RAM and execute’ routine, user programs are loaded into MCU RAM via the SCI port and then executed. Data is loaded sequentially, starting at RAM location $0050, until the last byte is loaded. Program control is then transferred to the RAM program starting at location $0051. The first byte loaded is the count of the total number of bytes in the program plus the count byte. The program starts at the second byte in RAM. During the firmware initialization stage, the SCI is configured for the NRZ data format (idle line, start bit, eight data bits and stop bit). The baud rate is 9600 with a 4 MHz crystal. A program to convert ASCII S-records to the format required by the RAM loader is available from Freescale.

If immediate execution is not desired after loading the RAM program, it is possible to hold off execution. This is accomplished by setting the byte count to a value that is greater than the overall length of the loaded data. When the last byte is loaded, the firmware will halt operation expecting additional data to arrive. At this point, the reset switch is placed in the reset position which will reset the MCU, but keep the RAM program intact. All routines can now be entered from this state, including the one which will execute the program in RAM (see Section 2.3).

To load a program in the EEPROM, the ‘load program in RAM and execute’ function is also used. In this instance the process involves two distinct steps. Firstly, the RAM is loaded with a program which will control the loading of the EEPROM, and when the RAM contents are executed, the MCU is instructed to load the EEPROM.

The erased state of the EEPROM is $FF.

Figure 2-1 shows the schematic diagram of the circuit required for the serial RAM loader.

2.5.5 TCAP2

The TCAP2 input controls the input capture 2 function of the on-chip programmable timer system.

2.5.6 TCMP1

The TCMP1 pin is the output of the output compare 1 function of the timer system.

2.5.7 TCMP2

The TCMP2 pin is the output of the output compare 2 function of the timer system.

2.5.8 OSC1, OSC2

These pins provide control input for an on-chip oscillator circuit. A crystal, ceramic resonator or external clock signal connected to these pins supplies the oscillator clock. The oscillator frequency (f_{OSC}) is divided by two to give the internal bus frequency (f_{OP}). There is also a software option which introduces an additional divide by 16 into the oscillator clock, giving an internal bus frequency of $f_{OSC}/32$.

2.5.8.1 Crystal

The circuit shown in Figure 2-5(a) is recommended when using either a crystal or a ceramic resonator. Figure 2-5(d) lists the recommended capacitance and feedback resistance values. The internal oscillator is designed to interface with an AT-cut parallel-resonant quartz crystal resonator in the frequency range specified for f_{OSC} (see Section 11.4). Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and associated components should be mounted as close as possible to the input pins to minimise output distortion and start-up stabilisation time. The manufacturer of the particular crystal being considered should be consulted for specific information.

2.5.8.2 Ceramic resonator

A ceramic resonator may be used instead of a crystal in cost sensitive applications. The circuit shown in Figure 2-5(a) is recommended when using either a crystal or a ceramic resonator. Figure 2-5(d) lists the recommended capacitance and feedback resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

FOLV2 — Force output compare 2

This bit always reads as zero, hence writing a zero to this bit has no effect. Writing a one at this position will force the OLV2 bit to the corresponding output level latch, thus appearing at the TCMP2 pin. Note that this bit does not affect the OCF2 bit of the status register (see Section 5.4.3).

1 (set) – OLV2 bit forced to output level latch.

0 (clear) – No effect.

FOLV1 — Force output compare 1

This bit always reads as zero, hence writing a zero to this bit has no effect. Writing a one at this position will force the OLV1 bit to the corresponding output level latch, thus appearing at the TCMP1 pin. Note that this bit does not affect the OCF1 bit of the status register (see Section 5.4.3).

1 (set) – OLV1 bit forced to output level latch.

0 (clear) – No effect.

OLV2 — Output level 2

When OLV2 is set a high output level will be clocked into the output level register by the next successful output compare, and will appear on the TCMP2 pin. When clear, it will be a low level which will appear on the TCMP2 pin.

1 (set) – A high output level will appear on the TCMP2 pin.

0 (clear) – A low output level will appear on the TCMP2 pin.

IEDG1 — Input edge 1

When IEDG1 is set, a positive-going edge on the TCAP1 pin will trigger a transfer of the free-running counter value to the input capture register 1. When clear, a negative-going edge triggers the transfer.

1 (set) – TCAP1 is positive-going edge sensitive.

0 (clear) – TCAP1 is negative-going edge sensitive.

Note: There is no need for an equivalent bit for the input capture register 2 as TCAP2 is negative-going edge sensitive only.

OLV1 — Output level 1

When OLV1 is set a high output level will be clocked into the output level register by the next successful output compare, and will appear on the TCMP1 pin. When clear, it will be a low level which will appear on the TCMP1 pin.

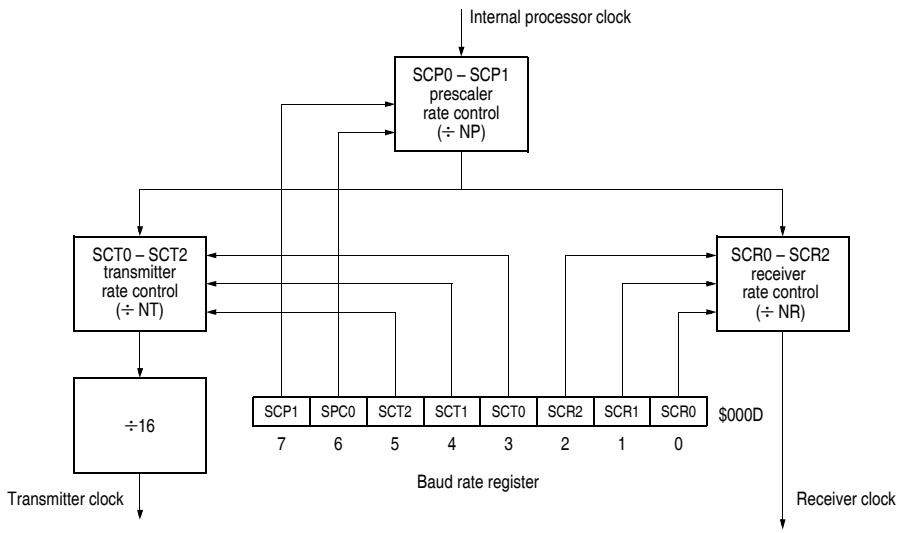
1 (set) – A high output level will appear on the TCMP1 pin.

0 (clear) – A low output level will appear on the TCMP1 pin.

When SCDR is read, it contains the last data byte received, provided that the receiver is enabled. The receive data register full flag bit (RDRF) in the SCSR is set to indicate that a data byte has been transferred from the input serial shift register to the SCDR; this will cause an interrupt if the receiver interrupt is enabled. The data transfer from the input serial shift register to the SCDR is synchronized by the receiver bit rate clock. The OR (overrun), NF (noise), or FE (framing) error flags in the SCSR may be set if data reception errors occurred.

An idle line interrupt is generated if the idle line interrupt is enabled and the IDLE bit (which detects idle line transmission) in SCSR is set. This allows a receiver that is not in the wake-up mode to detect the end of a message or the preamble of a new message, or to resynchronize with the transmitter. A valid character must be received before the idle line condition or the IDLE bit will not be set and idle line interrupt will not be generated.

The SCP0 and SCP1 bits function as a prescaler for SCR0–SCR2 to generate the receiver baud rate and for SCT0–SCT2 to generate the transmitter baud rate. Together, these eight bits provide multiple transmitter/receiver rate combinations for a given crystal frequency (see Figure 6-2). This register should only be written to while both the transmitter and receiver are disabled (TE=0, RE=0).



Note: There is a fixed rate divide-by-16 before the transmitter to compensate for the inherent divide-by-16 of the receiver (sampling). This means that by loading the same value for both the transmitter and receiver baud rate selector, the same baud rates can be obtained.

Figure 6-2 SCI rate generator division

8.2.3 A/D status/control register (ADSTAT)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000

COCO — Conversion complete flag

1 (set) – COCO is set each time a conversion is complete, allowing the new result to be read from the A/D result data register ($08). The converter then starts a new conversion.

0 (clear) – COCO is cleared by reading the result data register or writing to the status/control register.

Reset clears the COCO flag.

ADRC — A/D RC oscillator control

The ADRC bit allows the user to control the A/D RC oscillator, which is used to provide a sufficiently high clock rate to the A/D to ensure accuracy when the chip is running at low speeds.

1 (set) – When the ADRC bit is set, the A/D RC oscillator is turned on and, if ADON is set, the A/D runs from the RC oscillator clock. See Table 8-1.

0 (clear) – When the ADRC bit is cleared, the A/D RC oscillator is turned-off and, if ADON is set, the A/D runs from the CPU clock.

When the A/D RC oscillator is turned on, it takes a time t_{ADRC} to stabilize (see Table 11-6 and Table 11-7). During this time A/D conversion results may be inaccurate.

Note: If the MCU bus clock falls below 1 MHz, the A/D RC oscillator should be switched on.

Power-on or external reset clears the ADRC bit.

Table 8-1 A/D clock selection

ADRC	ADON	RC oscillator	A/D converter	Comments
0	0	OFF	OFF	A/D switched off.
0	1	OFF	ON	A/D using CPU clock.
1	0	ON	OFF	Allows the RC oscillator to stabilize.
1	1	ON	ON	A/D using RC oscillator clock.

Table 10-3 Branch instructions

		Relative addressing mode		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**
Branch always	BRA	20	2	3
Branch never	BRN	21	2	3
Branch if higher	BHI	22	2	3
Branch if lower or same	BLS	23	2	3
Branch if carry clear	BCC	24	2	3
(Branch if higher or same)	(BHS)	24	2	3
Branch if carry set	BCS	25	2	3
(Branch if lower)	(BLO)	25	2	3
Branch if not equal	BNE	26	2	3
Branch if equal	BEQ	27	2	3
Branch if half carry clear	BHCC	28	2	3
Branch if half carry set	BHCS	29	2	3
Branch if plus	BPL	2A	2	3
Branch if minus	BMI	2B	2	3
Branch if interrupt mask bit is clear	BMC	2C	2	3
Branch if interrupt mask bit is set	BMS	2D	2	3
Branch if interrupt line is low	BIL	2E	2	3
Branch if interrupt line is high	BIH	2F	2	3
Branch to subroutine	BSR	AD	2	6

Table 10-4 Bit manipulation instructions

		Addressing Modes					
		Bit set/clear			Bit test and branch		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**
Branch if bit n is set	BRSET n (n=0–7)				2•n	3	5
Branch if bit n is clear	BRCLR n (n=0–7)				01+2•n	3	5
Set bit n	BSET n (n=0–7)	10+2•n	2	5			
Clear bit n	BCLR n (n=0–7)	11+2•n	2	5			

11.2.2 I_{DD} trends for 3.3V operation

For the examples below, typical values are at the mid-point of the voltage range and at a temperature of 25°C only.

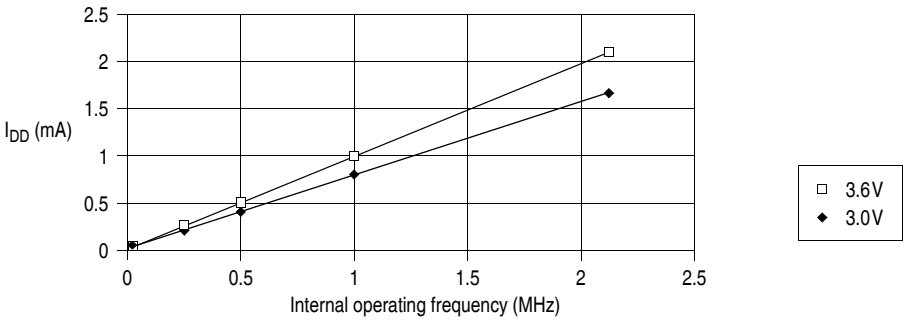


Figure 11-7 Run I_{DD} vs internal operating frequency (3 V, 3.6 V)

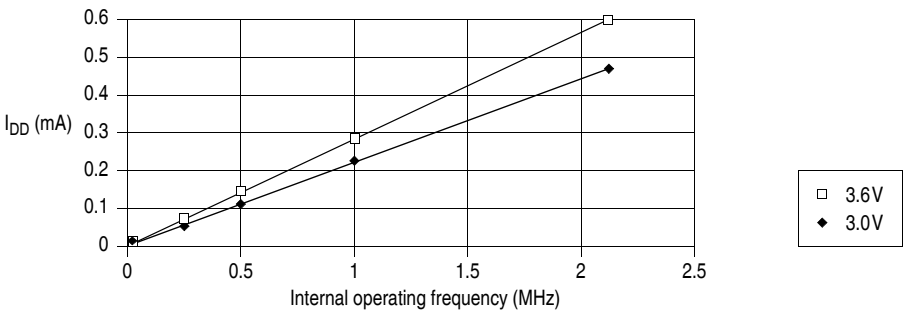


Figure 11-8 Run I_{DD} (SM = 1) vs internal operating frequency (3V,3.6V)

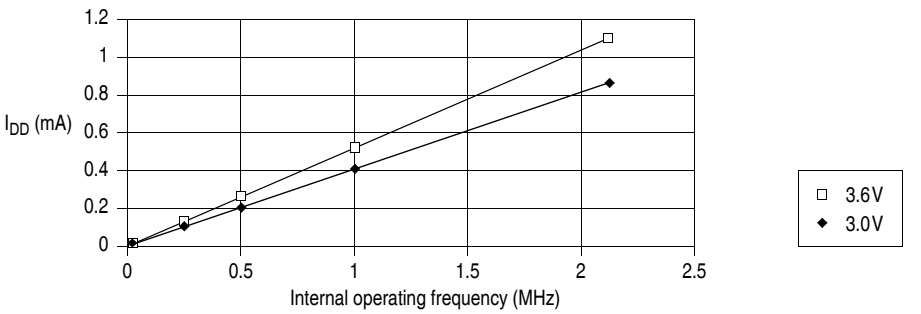


Figure 11-9 Wait I_{DD} vs internal operating frequency (3V, 3.6V)

E.3.5 EEPROM options register (OPTR)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Options (OPTR)(1)	$0100							EE1P	SEC	Not affected

(1) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

EE1P – EEPROM protect bit

In order to achieve a higher degree of protection, the EEPROM is effectively split into two parts, both working from the VPP1 charge pump. Part 1 of the EEPROM array (32 bytes from $0100 to $011F) cannot be protected; part 2 (224 bytes from $0120 to $01FF) is protected by the EE1P bit in the options register.

1 (set) – Part 2 of the EEPROM array is not protected; all 256 bytes of EEPROM can be accessed for any read, erase or programming operations.

0 (clear) – Part 2 of the EEPROM array is protected; any attempt to erase or program a location will be unsuccessful.

When this bit is set to 1 (erased), the protection will remain until the next power-on or external reset. EE1P can only be written to ‘0’ when the E1LAT bit in the EEPROM control register is set.

Note: The EEPROM1 protect function is disabled while in bootstrap mode.

SEC — Secure bit

This bit allows the EPROM and EEPROM1 to be secured from external access. When this bit is in the erased state (set), the EPROM and EEPROM1 content is not secured and the device may be used in non user mode. When the SEC bit is programmed to ‘zero’, the EPROM and EEPROM1 content is secured by prohibiting entry to the non user mode. To deactivate the secure bit, the EPROM has to be erased by exposure to a high density ultraviolet light, and the device has to be entered into the EPROM erase verification mode with PD1 set. When the SEC bit is changed, its new value will have no effect until the next power-on or external reset.

1 (set) – EEPROM/EPROM not protected.

0 (clear) – EEPROM/EPROM protected.

4) The exchange of data continues until the MC68HC705B16 has sent the four data bytes and the host has sent the 2 address data bytes and 4 data bytes.
5) If the data is different from $00 for EPROM or $FF for EEPROM, it is programmed at the address provided, while the next address and bytes are received and the previous data is echoed.
6) Loop to 1.

After reset, the MC68HC705B16 serial bootstrap routine will first echo two blocks of four bytes at $00, as no data is programmed yet.

If the data received is $00 for EPROM locations or $FF for EEPROM locations, no programming in the EPROM and EEPROM1 takes place, and the contents of the accessed location are returned as a prompt. The entire EPROM/EEPROM memory can be read in this fashion (serial dump).

Warning: When using this function with a programmed device, the device must be placed into RAM/EPROM/EEPROM serial bootstrap mode without EPROM erase check (PD4 = 1).

Serial RAM loading and execute can be accomplished in this mode. A RAM byte will be written if the address sent by the host in the serial protocol points to the RAM.

RAM bytes $008B–$00E3 and $0250–$02ED are available for user test programs. A 10-byte stack resides at the top of RAM1, allowing, for example, one interrupt and two sub-routine levels. The RAM addresses between $0050 and $008A are used by the loader and are therefore not available to the user during serial loading/executing.

If the SEC bit is at ‘1’, program execution is triggered by sending a negative (bit 7 set) high address; execution starts at address XADR ($008B).

In the RAM bootloader mode, all interrupt vectors are mapped to pseudo-vectors in RAM (see Table E-5). This allows programmers to use their own service-routine addresses. Each pseudo-vector is allowed three bytes of space rather than the two bytes for normal vectors, because an explicit jump (JMP) opcode is needed to cause the desired jump to the user’s service routine address.

Table E-5 Bootstrap vector targets in RAM

Vector targets in RAM	
SCI interrupt	$02EE
Timer overflow	$02F1
Timer output compare	$02F4
Timer input capture	$02F7
$\overline{\text{IRQ}}$	$02FA
SWI	$02FD

E.8 Control timing

Table E-11 Control timing for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	4.2	MHz
External clock option	f_{OSC}	dc	4.2	MHz
Internal operating frequency (f_{OSC}/2)				
Using crystal	f_{OP}	dc	2.1	MHz
Using external clock	f_{OP}	dc	2.1	MHz
Cycle time (see Figure 9-1)	t_{CYC}	480	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		5	µs
A/D converter stabilization time	t_{ADON}		500	µs
External RESET input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on RESET output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	10	—	ms
– 40 to 85 (extended)	t_{ERA}	10	—	ms
– 40 to 105 (industrial)	t_{ERA}	10	—	ms
– 40 to 125 (automotive)	t_{ERA}	10	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	10	—	ms
– 40 to 85 (extended)	t_{PROG}	10	—	ms
– 40 to 105 (industrial)	t_{PROG}	15	—	ms
– 40 to 125 (automotive)	t_{PROG}	20	—	ms
Timer (see Figure E-11)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	125	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width(5)	t_{OH}, t_{OL}	90	—	ns
Write/Erase endurance(6)(7)	—	10000		cycles
Data retention(6)(7)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.
(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{CYC}), this is the limiting factor in determining the timer resolution.
(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.
(5) t_{OH} and t_{OL} should not total less than 238ns.
(6) At a temperature of 85°C
(7) Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

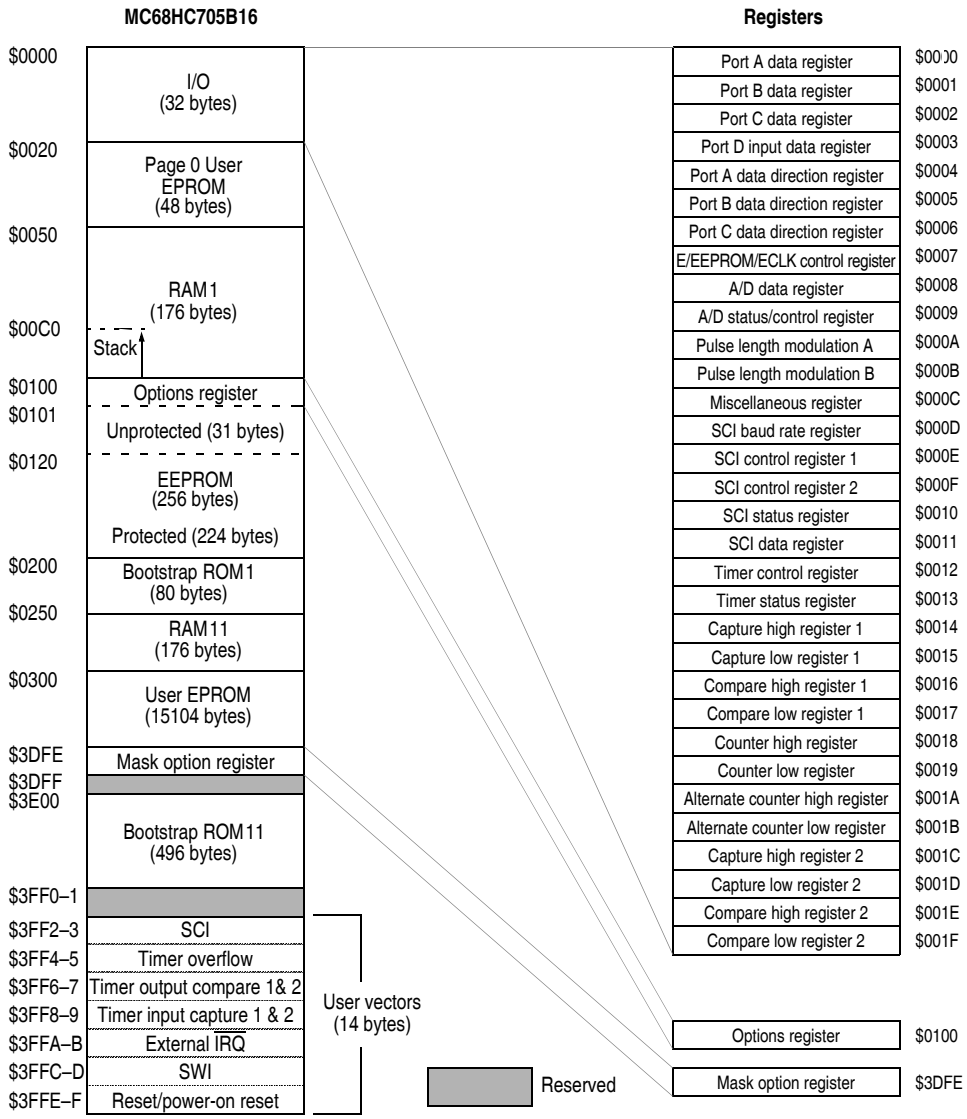


Figure F-2 Memory map of the MC68HC705B16N

Table F-10 A/D characteristics for 3.3V operation

(V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics ($V_{RH} = V_{DD}$ and V_{RL} = 0V)	—	± 1	LSB
Quantization error	Uncertainty due to converter resolution	—	± 1	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	± 2	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
ΔV_R	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion Internal RC oscillator	—	32	µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when $V_{IN} = V_{RL}$	00	—	Hex
Full scale reading	Conversion result when $V_{IN} = V_{RH}$	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling Internal RC oscillator(1)	—	12	µs
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(2)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Source impedances greater than 10kΩ will adversely affect internal charging time during input sampling.

(2) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 8-2).

Example

STOP

BRSET 0,$00,NEXT

NEXT any CPU instruction

The address compared may be any address in the page zero memory and the only restriction is that it should not be a register with flags cleared by reading the register. The example shows the address compared to be port A data register and this should not cause any problems in any applications.

High STOP Idd will be variable dependant upon the opcode following the STOP instruction. The more bits set in the following opcode, the higher the STOP Idd. The work around described above may be used on any 68HC05B32 or corrected version of the 68HC705B32 without problem. It simply adds a 5 cycle delay to the recovery from STOP and 3 bytes of additional code per STOP instruction but may alter the state of the carry bit in the CCR.

Also for the D59J:

The EEPROM programming circuit only fully supports 16-byte simultaneous programming mode and does not support single byte programming correctly.

The fault lies with the design of the EPROM array. A fault in the EPROM write data latch circuitry causes a latch to be driven to logic 0 on both sides when the data bus for that bit is logic 1. When the ELAT signal is removed, there is a race condition with the EPBS signal which results in the data bus value being copied to all the EPROM latches.

Since 16-byte simultaneous programming functions correctly, it is a relatively simple matter to emulate single byte programming by first initialising all 16 data latches to $00 and then writing the data to be written to the appropriate address.

This problem does not affect user application software in normally circumstances since it only applies to programming the EPROM array. The serial programming software should always simulate 16-byte programming. The Freescale software for programming the 705B32 from an IBM compatible PC functions in 16 byte programming mode. This program therefore correctly programs the EPROM.

In normal circumstances this errata does not affect the user application software. This only affects software that programs the EPROM array. The parallel programming bootloader software within the 705B32 ROM performs 16-byte programming and so functions correctly.

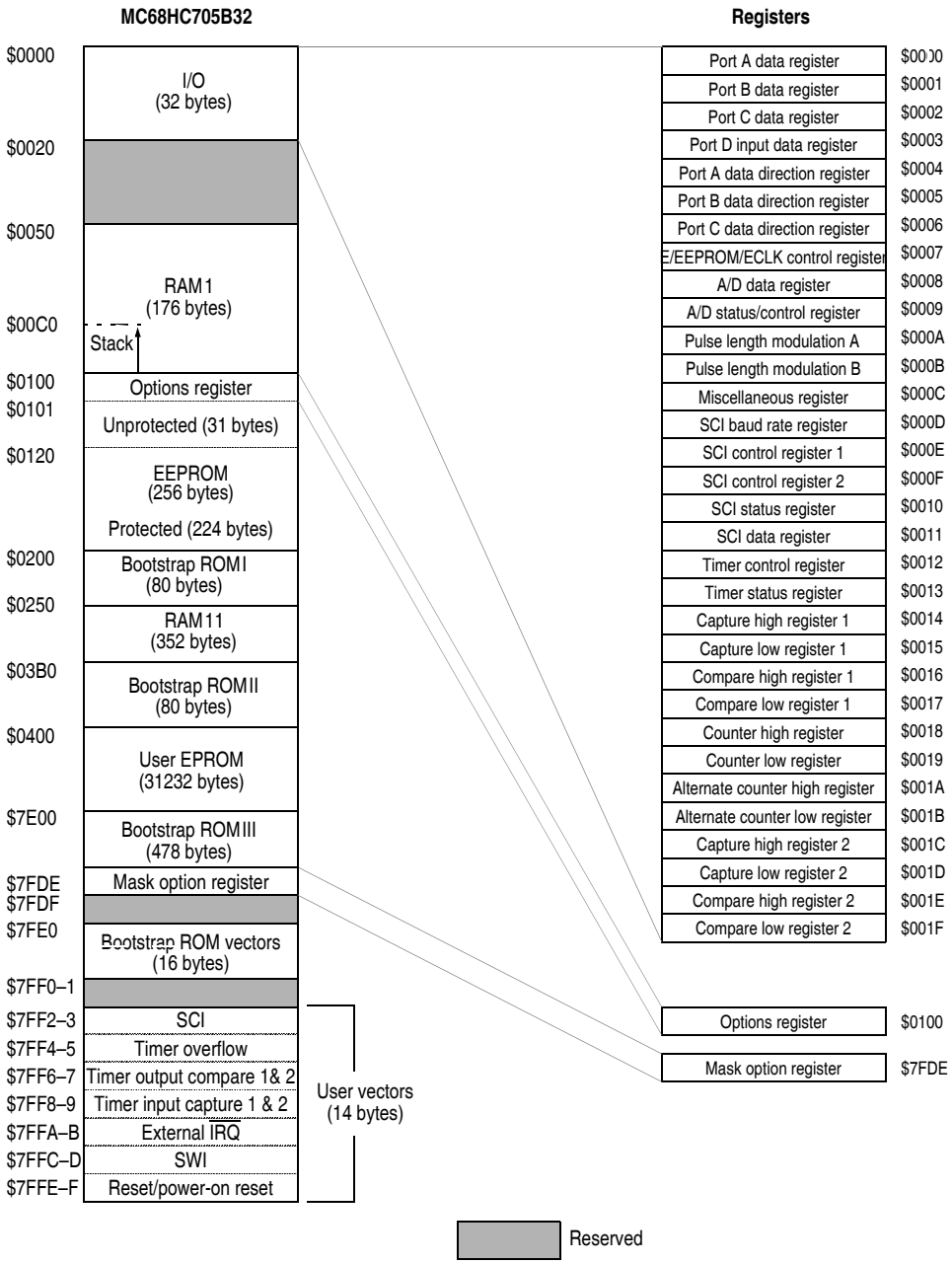


Figure H-2 Memory map of the MC68HC705B32

H.7 DC electrical characteristics

Table H-7 DC electrical characteristics for 5V operation

(V_{DD} = 5 Vdc ± 10%, V_{SS} = 0 Vdc, –40 to +85°C)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{LOAD} = – 10 µA I_{LOAD} = +10 µA	 V_{OH} V_{OL}	 V_{DD} – 0.1 —	 — —	 — 0.1	V
Output high voltage (I_{LOAD} = 0.8mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2 Output high voltage (I_{LOAD} = 1.6mA) TDO, SCLK, PLMA, PLMB Output high voltage (I_{LOAD} = -300µA) OSC2	 V_{OH} V_{OH} V_{OH}	 V_{DD} – 0.8 V_{DD} – 0.8 V_{DD} – 0.8	 V_{DD} – 0.4 V_{DD} – 0.4 V_{DD} – 0.3	 — — —	V
Output low voltage (I_{LOAD} = 1.6mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB Output low voltage (I_{LOAD} = 1.6mA) $\overline{RESET}$ Output low voltage (I_{LOAD} = -100µA) OSC2	 V_{OL} V_{OL} V_{OL}	 — — —	 0.1 0.4 TBD	 0.4 1 —	V
Input high voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage PA0–7, PB0–7, PC0–7, PD0–7,OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Supply current[3] (For Guidance Only) RUN (SM = 0) (See Figure 11-1) RUN (SM = 1) (See Figure 11-2) WAIT (SM = 0) (See Figure 11-3) WAIT (SM = 1) (See Figure 11-4) STOP 0 to 70 (standard) – 40 to 85 (extended)	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — —	 6 1.5 2 1 10 10	 TBD TBD TBD TBD TBD TBD	 mA mA mA mA µA µA
High-Z leakage current PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	±0.2	±1	µA
Input current Port B and port C pull-down (V_{IN}=V_{IH})	I_{RPD}		80		µA
Input current (0 to 70) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	±0.2	±1	µA
Input current (– 40 to 85) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	—	±5	µA
Capacitance Ports (as input or output), $\overline{RESET}$, TDO, SCLK $\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI PD0/AN0–PD7/AN7 (A/D off) PD0/AN0–PD7/AN7 (A/D on)	 C_{OUT} C_{OUT} C_{IN} C_{IN}	 — — — —	 — — 12 22	 12 8 — —	 pF pF pF pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25°C only.

H.9 Control timing

Table H-11 Control timing for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 to +85°C)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation Crystal option External clock option	 f_{OSC} f_{OSC}	 — dc	 4.2 4.2	 MHz MHz
Internal operating frequency (f_{OSC}/2) Using crystal Using external clock	 f_{OP} f_{OP}	 — dc	 2.1 2.1	 MHz MHz
Cycle time (see Figure 9-1)	t_{CYC}	476	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		5	µs
A/D converter stabilization time	t_{ADON}		500	µs
External RESET input pulse width	t_{RL}	3.0	—	t_{CYC}
Power-on RESET output pulse width 4064 cycle 16 cycle	 t_{PORL} t_{PORL}	 4064 16	 — —	 t_{CYC} t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time 0 to 70 (standard) – 40 to 85 (extended)	 t_{ERA} t_{ERA}	 10 10	 — —	 ms ms
EEPROM byte program time(1) 0 to 70 (standard) – 40 to 85 (extended)	 t_{PROG} t_{PROG}	 10 10	 — —	 ms ms
Timer (see Figure H-10) Resolution(2) Input capture pulse width Input capture pulse period	 t_{RESL} t_{TH}, t_{TL} t_{TLTL}	 4 125 —(3)	 — — —	 t_{CYC} ns t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width(5)	t_{OH}, t_{OL}	90	—	ns
Write/Erase endurance(6)(7)	—	10000		cycles
Data retention(6)(7)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{CYC}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

(5) t_{OH} and t_{OL} should not total less than 238ns.

(6) At a temperature of 85°C

(7) Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

I.1 DC electrical characteristics

Table I-2 DC electrical characteristics for 5V operation

(V_{DD} = 5 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 to +85°C)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{LOAD} = – 10 µA I_{LOAD} = +10 µA	 V_{OH} V_{OL}	 V_{DD} – 0.1 —	 — —	 — 0.1	V
Output high voltage (I_{LOAD} = 0.8 mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2 Output high voltage (I_{LOAD} = 1.6 mA) TDO, SCLK, PLMA, PLMB	 V_{OH} V_{OH}	 V_{DD} – 0.8 V_{DD} – 0.8	 — — —	 — —	V
Output low voltage (I_{LOAD} = 1.6 mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB Output low voltage (I_{LOAD} = 1.6 mA) $\overline{RESET}$	 V_{OL} V_{OL}	 — — —	 — — —	 0.4 1	V
Input high voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Supply current[3] RUN (SM = 0) (See Figure 11-1) RUN (SM = 1) (See Figure 11-2) WAIT (SM = 0) (See Figure 11-3) WAIT (SM = 1) (See Figure 11-4) STOP 0 to 70 (standard) – 40 to 85 (extended)	 I_{DD} 	 — — — — — —	 — — — — — —	 12 3 4 2 10 20	 mA mA mA mA µA µA
High-Z leakage current PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	—	±1	µA
Input current (0 to 70) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	— —	±5 ±1	µA
Capacitance Ports (as input or output), $\overline{RESET}$, TDO, SCLK $\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI PD0/AN0–PD7/AN7 (A/D off) PD0/AN0–PD7/AN7 (A/D on)	 C_{OUT} C_{IN} C_{IN} C_{IN}	 — — — —	 — — 12 22	 12 8 — —	 pF pF pF pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25°C only.

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 8.0MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and V_{IH} = V_{DD} – 0.2 V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

GLOSSARY

This section contains abbreviations and specialist words used in this data sheet and throughout the industry. Further information on many of the terms may be gleaned from Freescale's ***M68HC11 Reference Manual, M68HC11RM/AD***, or from a variety of standard electronics text books.

$xxxx	The digits following the '$' are in hexadecimal format.
%xxxx	The digits following the '%' are in binary format.
A/D, **ADC**	Analog-to-digital (converter).
Bootstrap mode	In this mode the device automatically loads its internal memory from an external source on reset and then allows this program to be executed.
Byte	Eight bits.
CCR	Condition codes register; an integral part of the CPU.
CERQUAD	A ceramic package type, principally used for EPROM and high temperature devices.
Clear	'0' — the logic zero state; the opposite of 'set'.
CMOS	Complementary metal oxide semiconductor. A semiconductor technology chosen for its low power consumption and good noise immunity.
COP	Computer operating properly. *aka* 'watchdog'. This circuit is used to detect device runaway and provide a means for restoring correct operation.
CPU	Central processing unit.
D/A, DAC	Digital-to-analog (converter).
EEPROM	Electrically erasable programmable read only memory. *aka* 'EEROM'.
EPROM	Erasable programmable read only memory. This type of memory requires exposure to ultra-violet wavelengths in order to erase previous data. *aka* 'PROM'.
ESD	Electrostatic discharge.
Expanded mode	In this mode the internal address and data bus lines are connected to external pins. This enables the device to be used in much more complex systems, where there is a need for external memory for example.